TI Designs：TIDA-010016
八端口 IO-Link® 主站参考设计

说明

需要快时序和快速周期时间的 PLC 应用 现已可利用此八端口 IO-Link®主站参考设计加以实现。它可用于构建远程 IO 网关以连接 OPC UA、Profinet、EtherCAT 或以太网 IP。基于 PRU 的帧处理程序可实现非常灵活的时序和时间同步方式。此设计有助于构建通用、可扩展的 IO-Link 主站。

资源

TIDA-010016	设计文件夹
TIOL111	产品文件夹
INA253	产品文件夹
TLC59282	产品文件夹
LM5165	产品文件夹
TPS4H160-Q1	产品文件夹

TI E2E™ Community

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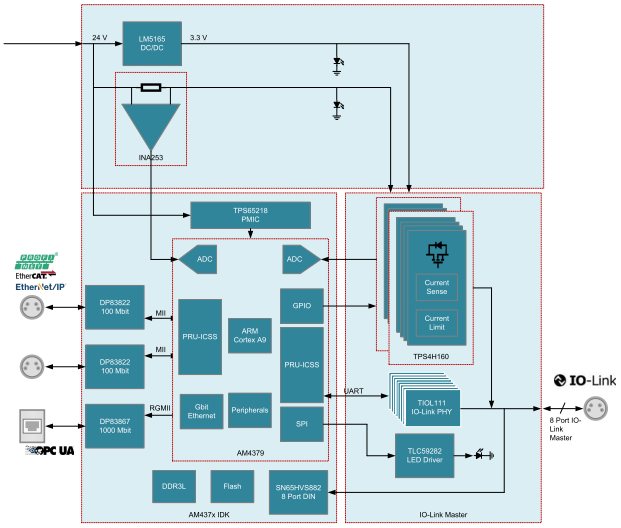
特性

- 八个 IO-Link 端口
- 支持 COM1、COM2、COM3
- 支持 400µs 周期时间
- 每端口的电流为 500mA
- 所有端口均具有过流保护和过流限制
- PRU 帧处理程序可实现灵活时序

应用

- 独立远程 IO
- 通信模块



1 System Description

Sensors and actuators are the most basic units of automation, feeding information into and acting on instructions from networked systems. Traditionally, these devices connect to control units through interfaces that provide little intelligence, and thus exchange little or no configuration and diagnostic information. Installing a new device requires configuration by hand at the point of use, and without diagnostics it is impossible to perform just-in-time preventive maintenance.

IO-Link (International Electrotechnical Commission [IEC] 61131-9) is an open standards protocol that addresses the need for intelligent control of small devices such as sensors and actuators. This standard provides low-speed point-to-point serial communication between a device and a master that normally serves as a gateway to a fieldbus and PLC. The intelligent link established enables ease of communication for data exchange, configuration, and diagnostics.

An unshielded three-wire cable as long as 20 meters, normally equipped with M12 connectors, establishes an IO-Link connection. Data rates range up to 230 kbps with a nonsynchronous minimum cycle time of 400 µs, +10%. Four operating modes support bidirectional input/output (I/O), digital input, digital output and deactivation. Security mechanisms and deterministic data delivery are not specified. A profile known as the IO Device Description (IODD) contains communication properties; device parameters; identification, process and diagnostic data; and information specifically about the device and manufacturer.

The many advantages of an IO-Link system include standardized wiring, increased data availability, remote monitoring and configuration, simple replacement of devices and advanced diagnostics. IO-Link permits factory managers to receive sensor updates and plan for upcoming maintenance or replacement. Swapping out a sensing or actuation unit that needs replacement and configuring a new one from the PLC through the IO-Link master eliminates manual setup and reduces downtime. Switching production remotely from one configuration to another without visiting the factory floor facilitates easier product customization. Factories can upgrade production lines readily to IO-Link, since it is backwards-compatible with existing standard I/O installations and cabling. Altogether, these capabilities result in reduced overall costs, more efficient processes, and greater machine availability.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage	External 24-V power supply	节 2.3.4
Input current	Depending on connected load (5 A recommended)	节 2.3.4
Output voltage	24 V	节 2.3.3
Output current per port	500 mA	节 2.3.3
Total output current	4 A	节 2.3.3
Number of IO-Link master ports	8	
Number of Ethernet ports	2	
Supported IO-Link data rates	COM1, COM2, COM3	
Supported IO-Link cycle time	400 µs	
Frame handler		节 2.4.1
Oversampling factor	8 times	
Sampling frequency	Up to 1.8432 MSPS per channel (COM3)	
Supported IO-Link transmission rates	COM3, COM2, COM1	

表 1. Key System Specifications (continued)

PARAMETER	SPECIFICATIONS	DETAILS
Equivalent Baud-rate	230.4 kbaud, 38.4 kbaud, 4.8 kbaud	
RX buffer size	128 bytes	
TX buffer size	2 x 128 bytes (double send buffer)	
Start bit and bit filter	Based on look-up table (can be adjusted)	
Parity check	Supported	
T1 time (UART frame transmission delay, master)	0 Tbit	
T2 time check (UART frame transmission delay, device)	Supported, hard coded to 5	
Ta time check (maximum response time)	Supported and user adjustable by register	

2 System Overview

2.1 Block Diagram

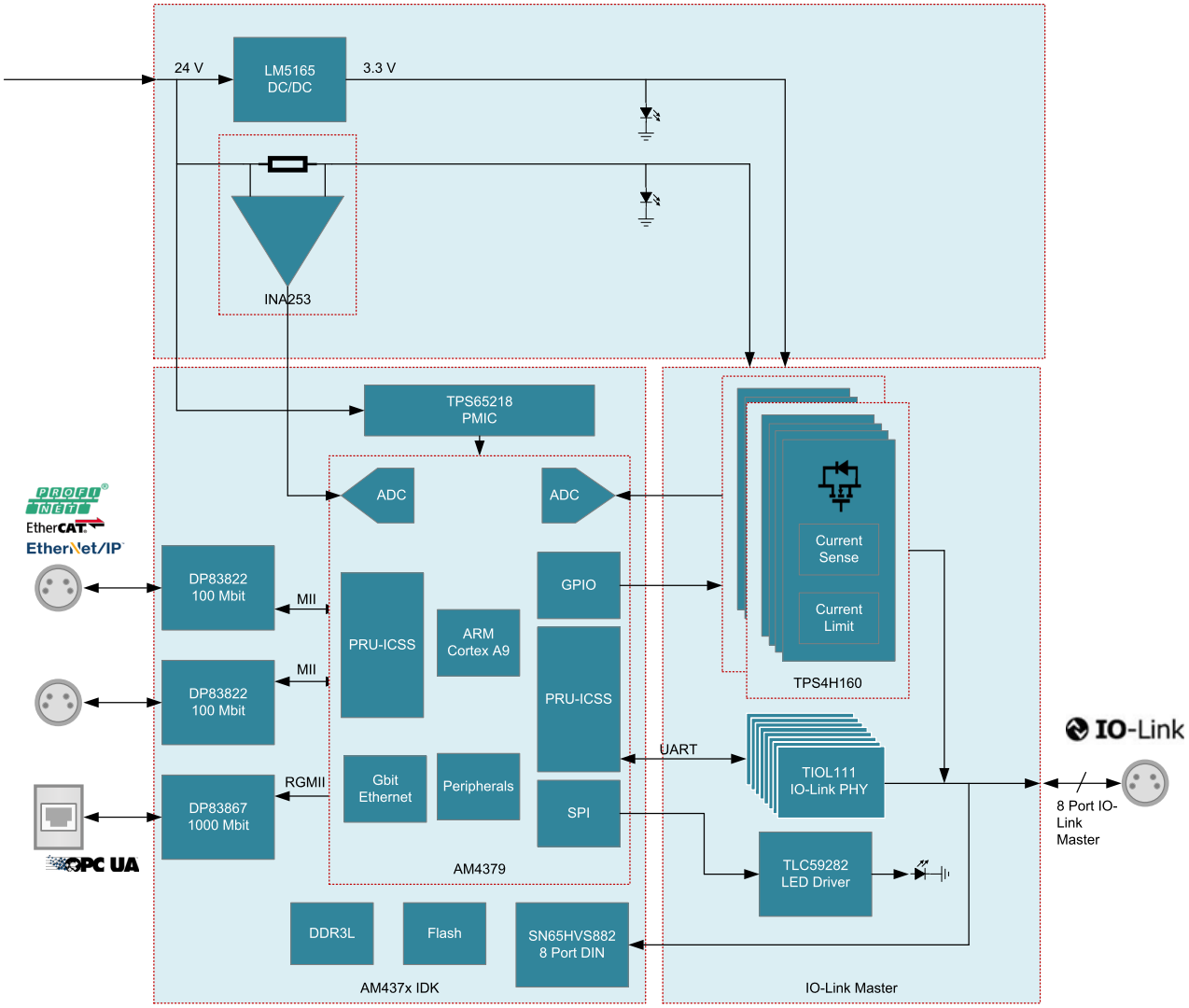


图 1. TIDA-010016 Block Diagram

2.2 Highlighted Products

This reference design uses TIOL111, TPS4H160, and TLC59282 on the one PCB for handling the main IO-Link master functionality. LM5165 and INA253 are used and the IDK adapter board for power supply and current monitoring.

2.2.1 LM5165

The LM5165 converter is an easy-to-use synchronous buck DC-DC regulator that operates from a 3-V to 65-V supply voltage. The device is intended for step-down conversions from 3.3-V, 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated and fully-regulated supply rails. With integrated high-side and low-side power MOSFETs, the LM5165 delivers up to 150-mA DC load current with high efficiency and ultra-low input quiescent current in a very small solution size. Designed for simple implementation, a choice of operating modes offers flexibility to optimize its usage according to the target application. In constant on-time (COT) mode of operation, ideal for low-noise, high current, fast load transient requirements, the device operates with predictive on-time switching pulse. A quasi-fixed switching frequency over the input voltage range is achieved by using an input voltage feedforward to set the on-time. Alternatively, pulse frequency modulation (PFM) mode, complemented by an adjustable peak current limit, achieves exceptional light-load efficiency performance. Control-loop compensation is not required with either operating mode, reducing design time and external component count.

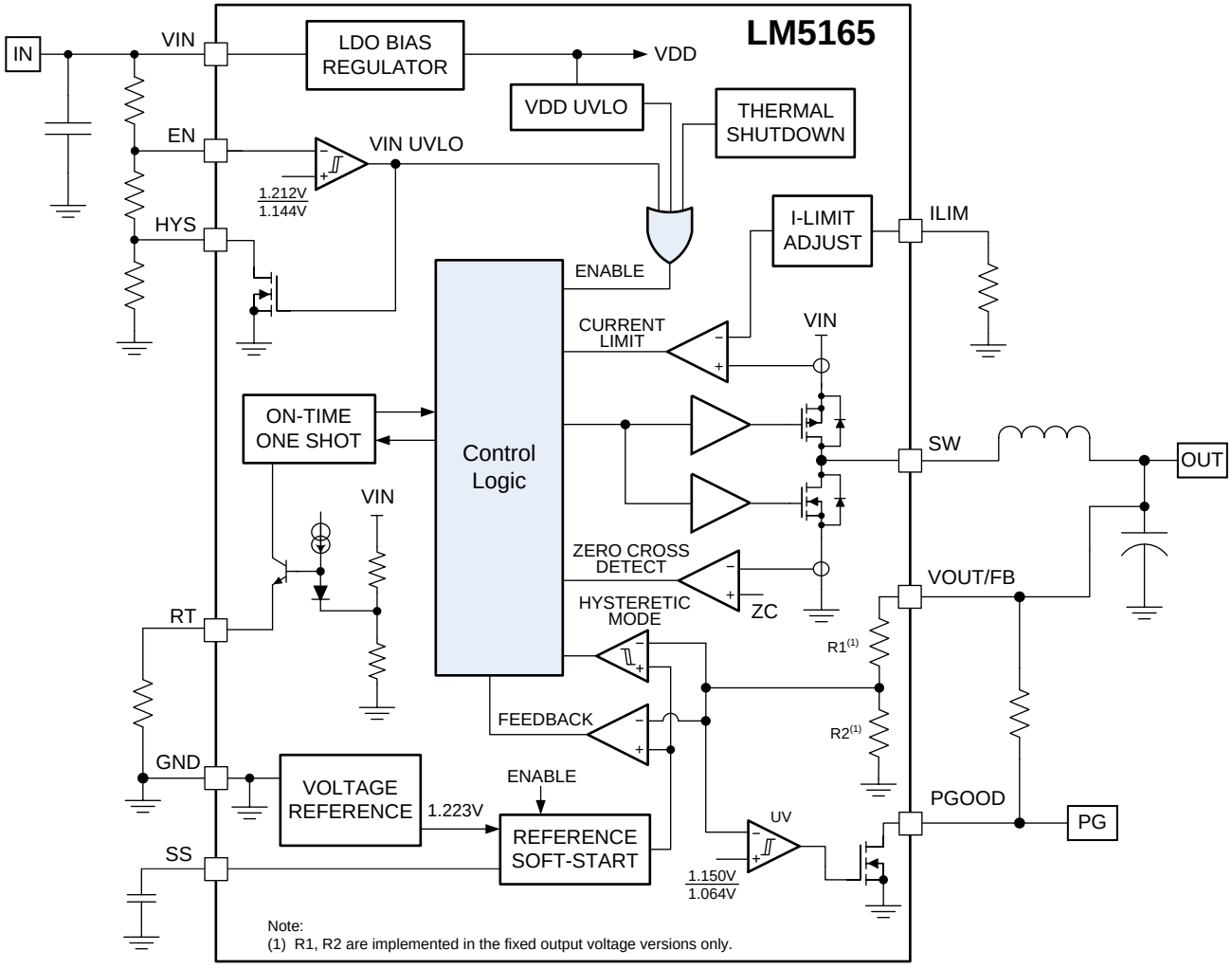


图 2. LM5165 Block Diagram

Key features relevant for this design are:

- Wide input voltage range of 3 V to 65 V
- Fixed 3.3-V output voltages

- 150-mA synchronous buck converter
- Integrated 2-Ω PMOS buck switch
- Integrated 1-Ω NMOS synchronous rectifier
  - Eliminates external rectifier diode
- Selectable PFM or COT mode operation
- No loop compensation or bootstrap components

This device allows to easily implement a small power supply solution with a wide input-voltage range.

2.2.2 TLC59282

The TLC59282 is a 16-channel, constant-current sink LED driver. Each channel can be turned on and off by writing serial data to an internal register. The constant-current value of all 16 channels is set by a single external resistor.

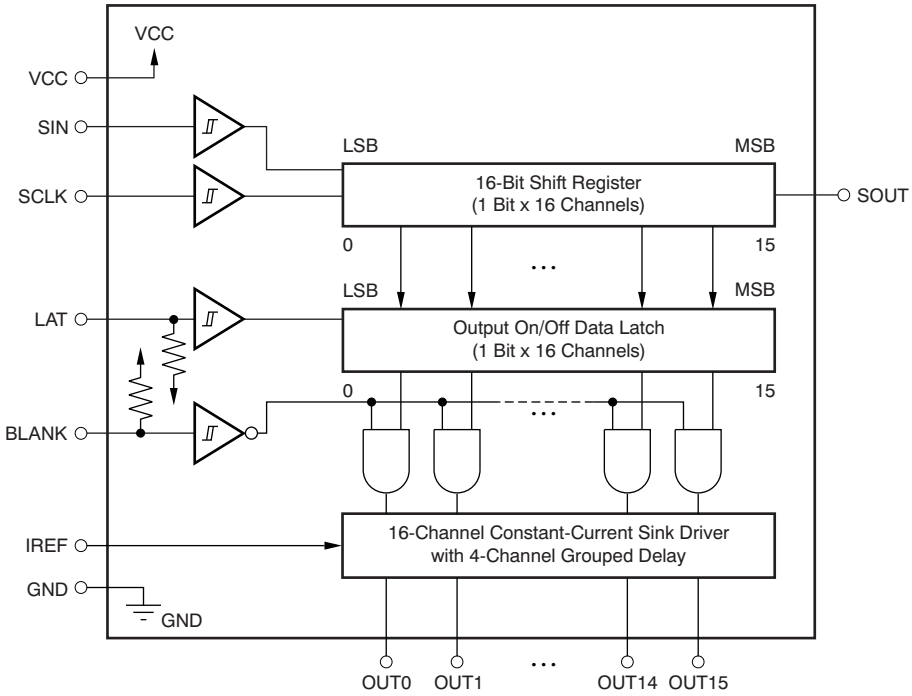


图 3. TLC59282 Block Diagram

Key features relevant for this design:

- 16 channels, constant-current sink output with on and off control
- 35-mA capability (constant-current sink)
- VCC = 3.0 V to 5.5 V
- Serial Peripheral Interface (SPI)

2.2.3 TPS4H160-Q1

The TPS4H160-Q1 device is a smart high-side switch, with internal charge pump and quad-channel integrated NMOS power FETs. Full diagnostics and high-accuracy current-sense features enable intelligent control of the load. The adjustable current-limit function greatly improves the reliability of whole system. The device has two versions with different diagnostic reporting, the open-drain digital output (version A) and the current-sense analog output (version B).

For version A, the device implements the digital fault report with an open-drain structure. When a fault occurs, the device pulls STx down to GND. A 3.3- or 5-V external pullup is required to match the microcontroller supply level. The digital status of each channel can report individually, or globally by connecting the STx pins together.

For version B, high-accuracy current sense makes the diagnostics more accurate without further calibration. One integrated current mirror can source 1 / K(CS) of the load current. The mirrored current flows into the CS-pin resistor to become a voltage signal. K(CS) is a constant value across temperature and supply voltage. A wide linear region from 0 V to 4 V allows a better real-time load-current monitoring. The CS pin can also report a fault with pullup voltage of VCS(H).

The external high-accuracy current limit allows setting the current-limit value by applications. When overcurrent occurs, the device improves system reliability by clamping the inrush current effectively. The device can also save system cost by reducing the size of PCB traces and connectors, and the capacity of the preceding power stage. Besides, the device also implements an internal current limit with a fixed value.

For inductive loads (relays, solenoids, valves), the device implements an active clamp between drain and source to protect itself. During the inductive switching-off cycle, both the energy of the power supply and the load are dissipated on the high-side switch. The device also optimizes the switching-off slew rate when the clamp is active, which helps the system design by keeping the effects of transient power and EMI to a minimum.

The TPS4H160-Q1 device is a smart high-side switch for a wide variety of resistive, inductive, and capacitive loads, including low-wattage bulbs, LEDs, relays, solenoids, heaters, and sub-modules.

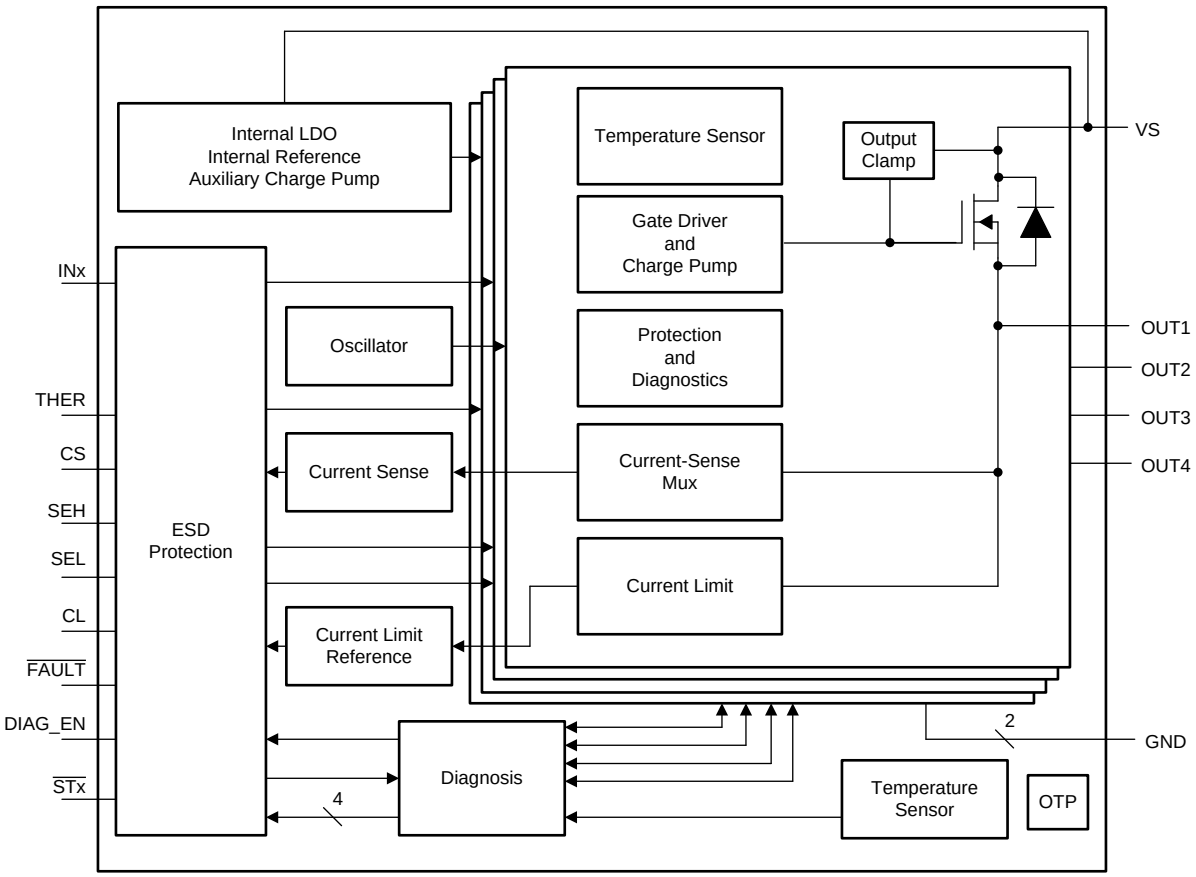


图 4. TPS4H160 Block Diagram

Key features that are of interest here:

- Quad-channel 160-mΩ smart high-side switch with full diagnostics
  - Version A: Open-drain digital output
  - Version B: Current-sense analog output
- Wide operating voltage 3.4 V to 40 V
- High-accuracy current sense: ±15% under >25- mA load
- Adjustable current limit with external resistor, ±15% under >500-mA load
- Protection
  - Short-to-GND protection by current limit (internal or external)
  - Thermal shutdown with latch off option and thermal swing
  - Inductive load negative voltage clamp with optimized slew rate
  - Loss-of-GND and loss-of-battery protection
- Diagnostics
  - Overcurrent and short-to-ground detection
  - Open-load and short-to-battery detection
  - Global fault report for fast interrupt

2.2.4 INA253

The INA253 features a 2-mΩ, precision, current-sensing resistor and a 80-V common-mode, zero-drift topology, precision, excellent common-mode rejection ratio (CMRR), and features enhanced pulse width modulation (PWM) rejection current-sensing amplifier integrated into a single package. High precision measurements are enabled through the matching of the shunt resistor value and the current-sensing amplifier gain providing a highly-accurate, system-calibrated solution. Enhanced PWM rejection reduces the effect of common-mode transients on the output signal that are associated with PWM signals. Multiple gain versions are available to allow for the optimization of the desired full-scale output voltage based on the target current range expected in the application.

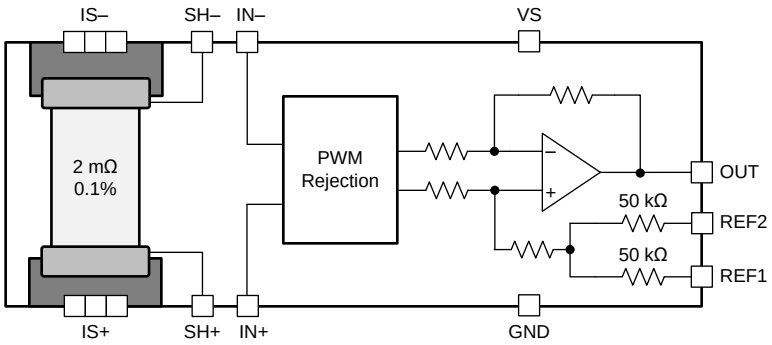


图 5. INA253 Block Diagram

The device has following key features:

- Precision integrated shunt resistor
  - Shunt resistor: 2 mΩ
  - Shunt resistor tolerance: 0.1% (maximum)
  - ±15 A continuous from –40°C to 85°C
  - 0°C to 125°C temperature coefficient: 10 ppm/°C
- Accuracy:
  - Gain error: 0.25% (maximum)
  - Gain drift: 10 ppm/°C (maximum)
  - Offset voltage: ±2 mA
  - Offset drift: 125 µA/°C (maximum)
- Wide common-mode range: –4 V to 80 V
- Available gains: 100 mV/A, 200 mV/A, and 400 mV/A

2.2.5 TIOL111

The robust TIOL111 family of transceivers implements the IO-Link interface for industrial point-to-point communication. When a device is connected to an IO-Link master through a three-wire interface, the master can initiate communication and exchange data with the remote node while the TIOL111 device acts as a complete physical layer for the communication.

These devices are capable of withstanding up to 1 kV (500 Ω) of IEC 61000-4-5 surge and feature integrated reverse-polarity protection.

A simple pin-programmable interface allows for easy interfacing to the controller circuits. The output current limit can be configured using an external resistor.

Fault reporting and internal protection functions are provided for undervoltage, short-circuit current, and overtemperature.

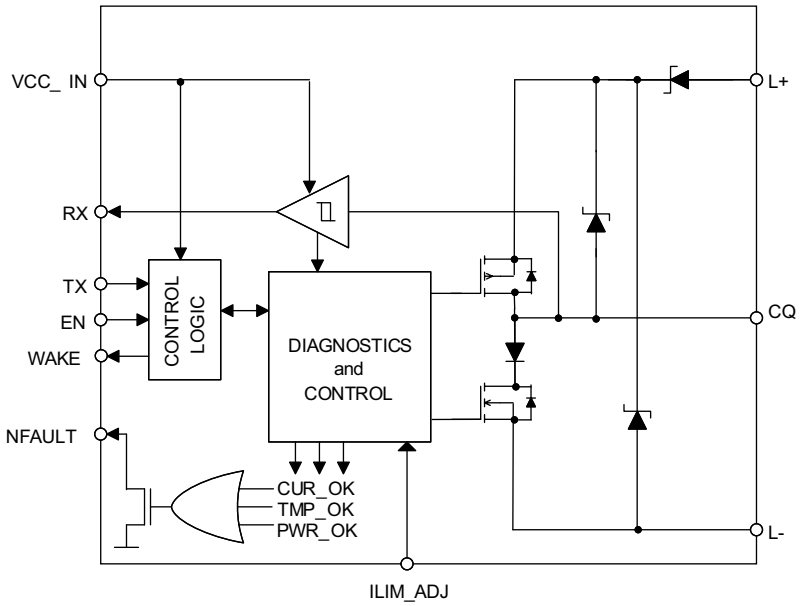


图 6. TIOL111 Block Diagram

Features of the TIOL111 device:

- PNP, NPN or IO-Link configurable output
  - IEC 61131-9 COM1, COM2 and COM3 data rate support
- 50-mA to 350-mA configurable current limit
- Tolerant to ±65-V transients < 100 µs
- Reverse polarity protection of up to 55 V on L+, CQ and L–
- Integrated EMC protection on L+ and CQ
- Integrated LDO options for up to 20-mA current

2.3 System Design Theory

This reference design implements an IO-Link master using the TIOL111 device PHY and surrounding components needed to build a complete IO-Link master design. Therefore, on the physical side in addition to the TIOL111 device, a power supply for the ports, as well as a current sink is necessary. Also the hardware must be able to drive the wake-up pulse.

On the other side it is necessary to have a hardware as well as frame handler that support all three communication speeds. The TIOL111 device used as PHY here can handle all speeds (COM1, COM2, COM3) the eight port frame handler is implemented on the PRU of the used AM437x.

To realize an eight-port master, eight TIOL111 devices are necessary; For each four ports, one TPS4H160 is necessary. Each port also needs one current sink. This results in only eight TIOL111 devices (IO-Link PHY), two TPS4H160 devices (high-side switch) and one TLC59282 device(LED driver).

2.3.1 IO-Link® PHY

The TIOL111 device used here has the main purpose to shift levels between the 3.3-V logic side and the 24-V interface. The optional internal LDO, the wake up detection and overcurrent detection is not used.

However, the TIOL111 device in master configuration has to be able to drive an IO-Link conform wake-up pulse. IO-Link devices start up in SIO mode and have to be configured to IO-Link prior to communication. So, the output is either on a low (around 0 V) or high level (around 24 V) and is driven. To switch the mode, the master has to send a pulse of 80-µs length and must be able to drive 500 mA during this pulse and still reach a certain voltage. The device will switch to IO-Link mode after detection of this pulse and communication can begin.

The exact parameters for testing this are listed in the *IO-Link® Test Specification, Version 1.1.2*, see 表 2 and 表 3. Both parts of the specification have to be met to be compliant.

表 2. Wake-Up Pulse Test Specification High Pulse

TEST CASE ATTRIBUTES	IDENTIFICATION, REFERENCE
Identification (ID)	SDCI_TC_0021
Name	TCM_PHYL_INTF_IQWUH
Purpose (short)	Driver capability of the wake-up pulse – high-side driver
Equipment under test (EUT)	Master and Legacy Master
Test case version	1.0
Category, type	Master protocol test; test to pass (positive testing)
Specification (clause)	See *Section 5.3.3.3*, *Table 9* of *IO-Link Interface and System Specification Version 1.1.2*
Configuration, setup	–
TEST CASE	**CONDITIONS, PERFORMANCE**
Purpose (detailed)	The Master shall drive the resistive load above the threshold high level of a receiver. Measure pulse voltage at Master C/Q port with Master configured for SDCI. The pulse voltage is measured with a resistive load applied between C/Q and L–.
Precondition	Master configured to SDCI mode
Procedure	a) Apply minimum supply voltage (VSM = 20 V) to Master b) Apply resistive load Rload between C/Q and L–: Rload = $VTHHM_{max}$ / $IQPKHM_{min}$ = 26 Ohm (51 Ohm shunted by 51 Ohm) c) Trigger on wake-up request d) Measure voltage at C/Q port during wake-up request e) Check if VIM is exceeding $VTHHM_{max}$ f) Repeat test with maximum supply voltage (VSM = 30 V)
Input parameter	–
Post condition	–
TEST CASE RESULTS	**CHECK, REACTION**
Evaluation	–
Test passed	Level at C/Q during wake-up request greater than or equal $VTHHM_{max}$
Test failed (examples)	Level at C/Q during wake-up request less thanl $VTHHM_{max}$
Results	VIM@WURQ (VSM = 18 V): <value> VIM@WURQ (VSM = 30 V): <value>

表 3. Wake-Up Pulse Test Specification Low Pulse

TEST CASE ATTRIBUTES	IDENTIFICATION, REFERENCE
Identification (ID)	SDCI_TC_0023
Name	TCM_PHYL_INTF_IQWUL
Purpose (short)	Driver capability of the wake-up pulse – low-side driver
Equipment under test (EUT)	Master and Legacy Master
Test case version	1.0
Category, type	Master protocol test; test to pass (positive testing)
Specification (clause)	See *Section 5.3.3.3*, *Table 9* of *IO-Link Interface and System Specification Version 1.1.2*
Configuration, setup	–
TEST CASE	**CONDITIONS, PERFORMANCE**
Purpose (detailed)	The Master shall drive the resistive load below the threshold low level of a receiver. Measure pulse voltage at Master C/Q port with Master configured for SDCI. The pulse voltage is measured with a resistive load applied between C/Q and L+.
Precondition	Master configured to SDCI mode
Procedure	a) Apply minimum supply voltage (VSM = 20 V) to Master b) Apply resistive load Rload between C/Q and L+: Rload = (VSM – $VTHLM_{min}$) / $IQPKLM_{min}$ = 24 Ohm (47 Ohm shunted by 51 Ohm) c) Trigger on wake-up request d) Measure voltage at C/Q port during wake-up request e) Check if VIM is below $VTHLM_{min}$ f) Repeat test with maximum supply voltage (VSM = 30 V) to Master: Rload = 44 Ohm (82 Ohm shunted by 100 Ohm)
Input parameter	–
Post condition	–
TEST CASE RESULTS	**CHECK, REACTION**
Evaluation	–
Test passed	Level at C/Q during wake-up request less than or equal $VTHLM_{min}$
Test failed (examples)	Level at C/Q during wake-up request greater thanl $VTHLM_{min}$
Results	VIM@WURQ (VSM = 20 V): <value> VIM@WURQ (VSM = 30 V): <value>

Prior to design, it is verified that the TIOL111 device can generate the wake-up pulse. In 图 7 one of the four test options is shown. In this case, the high-side driver is tested with VCC at 30 V. CQ is loaded with a 26-Ω resistor, here the CQ line reaches almost 30 V and the CQ current is larger than 500 mA. So this meets the requirements.

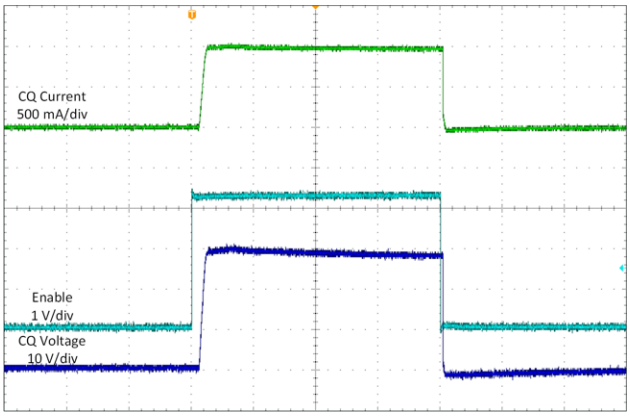


图 7. Test Results of TIOL111 Device Wake-Up Pulse

By design, the TIOL111 device is able to deliver the current necessary for the wake-up pulse, so it can be used as a master PHY.

2.3.2 Current Sink

Beside the wake-up pulse, the master PHY has a second important difference to the device PHY shown in 图 8. It has to include a current sink. Since the TIOL111 device does not include this in the chip, it is implemented on the board.

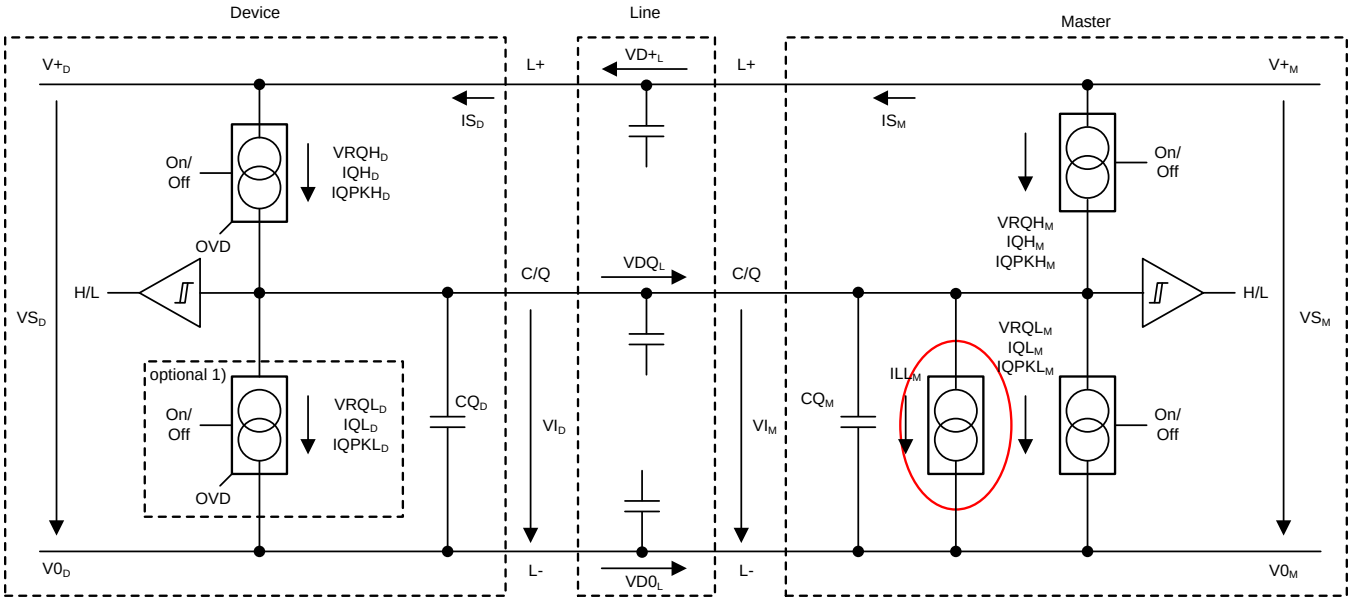


图 8. Block Diagram IO-Link® System

As the excerpt of the specification in 表 4 shows, the current has to be between 5 mA to 15 mA.

表 4. Specification for IO-Link® Master Current Sink(1)

ILL_M	Load or discharge current for: 0 V < VI_M < 5 V 5 V < VI_M < 15 V 15 V < VI_M < 30 V	 0 5 5	 N/A N/A N/A	 15 15 15	 mA mA mA

(1) Currents are compatible with the definition of type 1 digital inputs in IEC 61131-2. However, for the range 5 V < VI_M < 15 V, the minimum current is 5 mA instead of 2 mA in order to achieve short enough slew rates for pure p-switching devices.

Implementing such a small and tolerable current sink that is only active when the transmitter is disabled can be done with a simple NPN transistor.

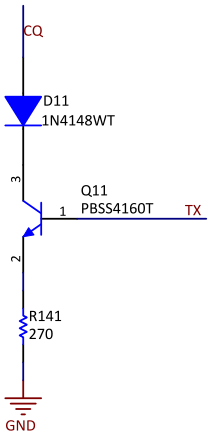


图 9. Simple Current Sink

图 9 shows the schematic. The current sink is controlled by the TX line coming from the MCU and going to the TIOL111 device. Since the logic of the TIOL111 device is inverting and the default level on the TX line is high in idle state, this will enable the current sink whenever the driver is disabled or transmitting a 0 V on the CQ line. So it does not increase the current consumption in normal operation.

2.3.3 Power Supply for L+

An IO-Link master has to power the L+ line with a current capability of at least 200 mA and 400 mA pulse for 50 ms. The specification states this as shown in 表 5.

表 5. Specification for L+ Supply

Property	Designation	Minimum	Typical	Maximum	Unit	Remark
VS_M	Supply voltage for devices	20	24	30	V	See *Voltage level definitions* in *IO-Link Interface and System Specification Version 1.1.2*
IS_M	Supply current for devices	200	N/A	N/A	mA	External supply required for > 200 mA
$ISIR_M$	Current pulse capability for devices	400	N/A	N/A	mA	Master supply current capability for a minimum of 50 ms at 18 V after power-on of the port supply

To supply this, a TPS4H160 device is used. This quad-channel, high-side switch provides a programmable current limit and has a current sense output that is connected to the MCU. So each channel is short-circuit protect and can be observed by the MCU to measure the current on each port and detect faults.

Meeting the requirements for the ISm is rather easy and can be achieved with any device with a low enough $R_{(DS)on}$. However, the ISIRm is more difficult to achieve, since the power dissipation from the junction to the ambient is a limiting factor here. When the output is shorted, or a large capacitor has to be charged, the power dissipation in the device is up to 400 mA × 30 V = 12 W for a short time. This can be even more, when the design drives more than the minimum current of 400 mA.

Charging a capacitor on the L+ line with a static load (which is a realistic scenario for an IO-Link device) relaxes this a bit, since the L+ line voltage increases, the voltage drop in the FET decreases and also the power dissipation decreases.

However, since the power does not propagate that fast to the PCB or a heat sink, mainly the package of the device is the limiting factor.

See the *Maximum Device consumption at power-up* table in *Section 4.4* of the *IO-Link Package 2015 & Corrigendum Version 1.0* for detailed specifications and the definition of a charge of 400 mA in the first 50 ms after power up, resulting in 20 mAs.

Due to this extension of the specification, the testing of the output on the L+ line is defined to be a large capacitor of 1000 µF in parallel with a 150-Ω resistor. This load simulates a device with a static load and a large input capacitor.

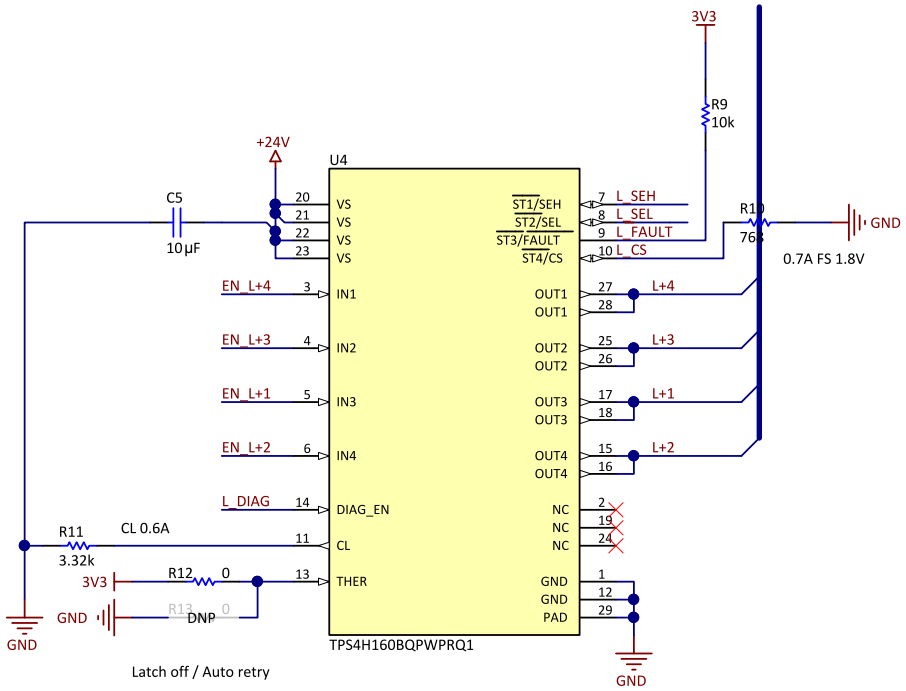


图 10. High-Side Switch Schematic

The high-side switch is configured to limit the current at 0.6 A. This current is selected to meet the requirements for the turn on behavior. At a higher current, the package cannot handle the power dissipation during charging the capacitor and the device switches off to cool down and restart again.

The current sense is configured to go up to 0.7 A at a maximum output voltage of 1.8 V (which is given by the ADC in the AM4379 device on the IDK used here). This results in the schematic seen in 图 10. The TPS4H160 device can be set to two different behaviors after a thermal error occurred: it can switch off or retry automatically, here it is configured to switch off until it is enabled again.

If other requirements are necessary or a turn on behavior with interruption is acceptable, a higher current of 1 A per port is feasible and working when turned on.

2.3.4 Power Supply

The IO-Link master is powered by 24 V. Since this design uses the AM437x IDK, which is also powered with 24 V, it is possible to power both boards with either one power supply or with two different 24-V supplies. However it is necessary to set the jumpers on the adapter board accordingly.

When the power supply is connected to the IDK and the IO-Link master should be powered through this, J7 on the adapter has to be shorted. The user has to take care that the total current is limited to 0.5 A on all ports. This configuration is not tested and not recommended.

The recommended way is to power the IDK through the adapter board, therefore one 24-V power supply should be connected either to J5 or J8. Jumpers J6 and J9 have to be shorted. To supply the IDK, J7 has to be shorted as well. When a separate power supply is used for the IDK, J7 has to be open.

表 6. Power Jumper Settings

Configuration	Power Supply	J6, J9	J7
Powered through IDK	Connected to IDK only	Open	Short
Powered through adapter	Connected to either J8 or J5	Short	Short
Separate power supplies	Connected to IDK and J8 or J5	Short	Open

The TLC59282 device, as well as the TIOL111 device need a 3.3-V supply. To not load the voltage regulator of the IDK, an additional LM5165 device is on the adapter board providing the required voltage. To ensure that the IO-Link master drives no signals to the IDK before all voltages there are stable, the LM5165 device will be turned on by the 3.3 V from the IDK.

2.3.5 Pinouts

The IO-Link master expansion for the AM437x IDK is connected through the two pin headers on the IDK. To get some of the necessary signals to the header modifications on the board are necessary. 图 11 shows the pinout, the modifications are listed in 表 7.

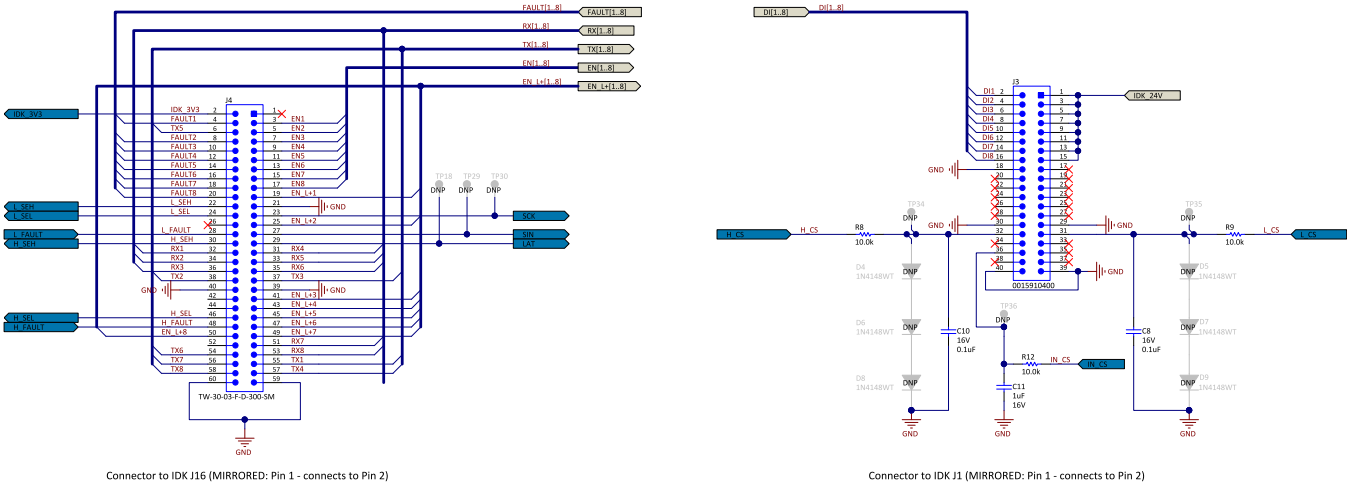


图 11. Pinout of the IO-Link® Board Connected to the IDK

表 7. Modifications

Pin	Signal	Remove	Add
J16 - 5	TX4	R187, R264	Wire from R187 to R264 (J16-5)
J16 - 23	GPIO5_20	-	10-kΩ resistor R343
J16 - 34	RX4	R541	-
J16 - 36	RX5	R541	-
J16 - 49	GPIO2_12	R406	-
J16 - 52	RX6	R541	-
J16 - 53	TX5	R179, R465	Wire from R179 to R465 (J16-53)
J16 - 54	RX7	R541	-
J16 - 55	TX6	R177, R471	Wire from R177 to R471 (J16-55)
J16 - 57	TX7	R70, R468	Wire from R70 to R468 (J16-57)
J1 - 31	AIN0	R454	0-Ω resistor R450
J1 - 32	AIN4	R109	0-Ω resistor R104
J1 - 35	AIN2	R561	0-Ω resistor R435

2.4 Software Frame Handler

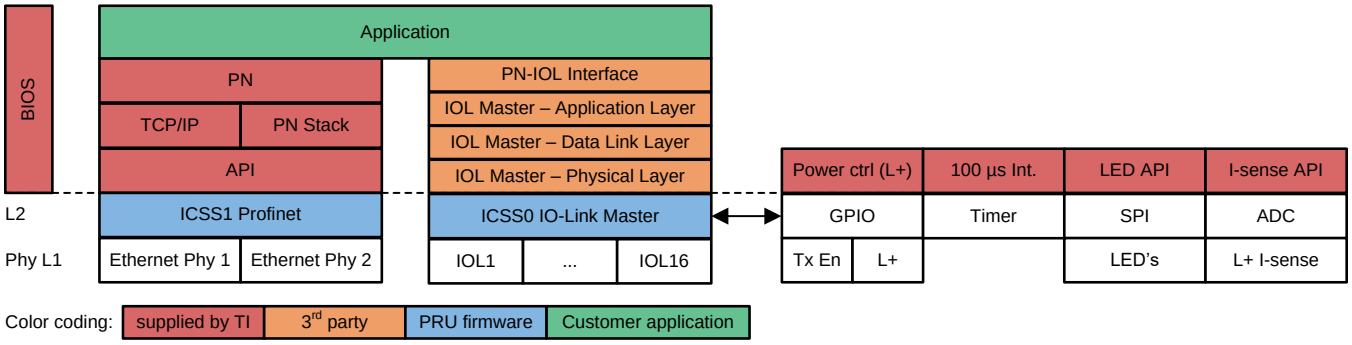


图 12. PRU-ICSS IO-Link® Master Project

图 12 shows the simplified structure of the PRU-ICSS IO-Link master project. It can be grouped into six independent parts:

- The PRU firmware which is the core component of the project and does the frame handling. It is basically a multichannel UART implementation with enhanced functionality.
- The IO-Link driver which is located between the PRU firmware and the different layers of the third-party supplied stack
- Additional TI-supplied RTOS driver functionality for IO-Link master specific features like power- and LED control
- The third-party supplied stack
- A customer specified application
- An optional second interface like Profinet (may be supplied by TI)

2.4.1 PRU-ICSS IO-Link® Frame-Handler

The IO-Link frame-handler is the core software component of the design. It replaces hardware UARTs by a software implementation and eliminates the need for external processing hardware.

2.4.1.1 Performance Advantages and Benefits

The Programmable Real-time Unit and Industrial Communication Sub-System (PRU-ICSS) hardware allows the user to write and run highly-predictable and deterministic software which is able to replace many solutions which are too time critical for a usual microcontroller. This hardware-like behavior enables the eight channel IO-Link master to react very fast and almost free of jitter.

The IO-Link frame-handler requires one PRU per eight channels and can provide 16 channels per ICSS. The often available second ICSS can be used to process something else like real-time Ethernet.

2.4.1.2 Principle of Operation

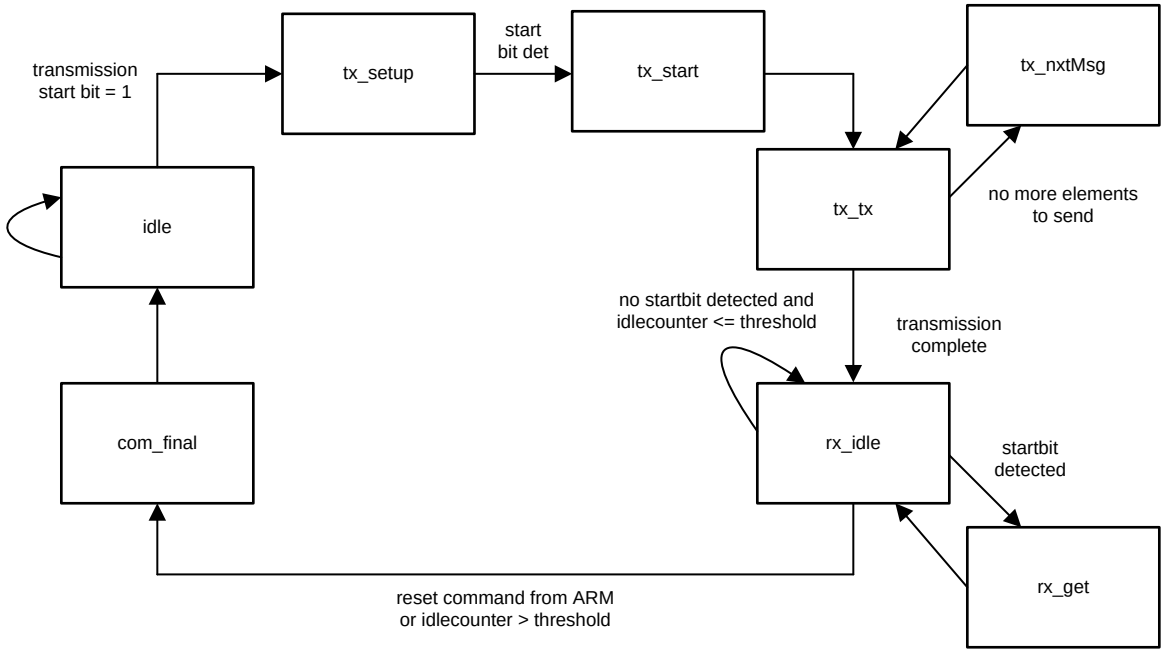


图 13. State Machine of the Frame-Handler Simplified Overview

图 13 shows an overview of the state machine of the frame-handler. This is by no means a complete description of the firmware but an illustration of the communication cycle.

The frame-handler is started by the “transmission start bit” which will trigger a new transmission of the selected transmit buffer. It will then transmit until the transmit buffer pointer has reached the last byte of the ongoing transmission. The end of the transmission will force a state change to the receive state which will receive data until the transmission is complete. A transmission can be completed with errors or without errors. These errors will just be reported by status bits. Error reactions and countermeasures are the responsibility of the IO-Link master stack. A completed communication cycle is indicated by bit-flags and an optional interrupt.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

To get started, the two IO-Link master boards have to be stacked together and have to be stacked to the AM437x IDK. A 24-V, 5-A power supply has to connected to J8 or J5. Jumpers J6, J7, and J9 on the adapter board have to be shorted. In 图 14 the related jumpers and connectors are shown. The LEDs for 24 V and 3.3 V should light up, when the corresponding voltage is present. In normal operation both LEDs will light.

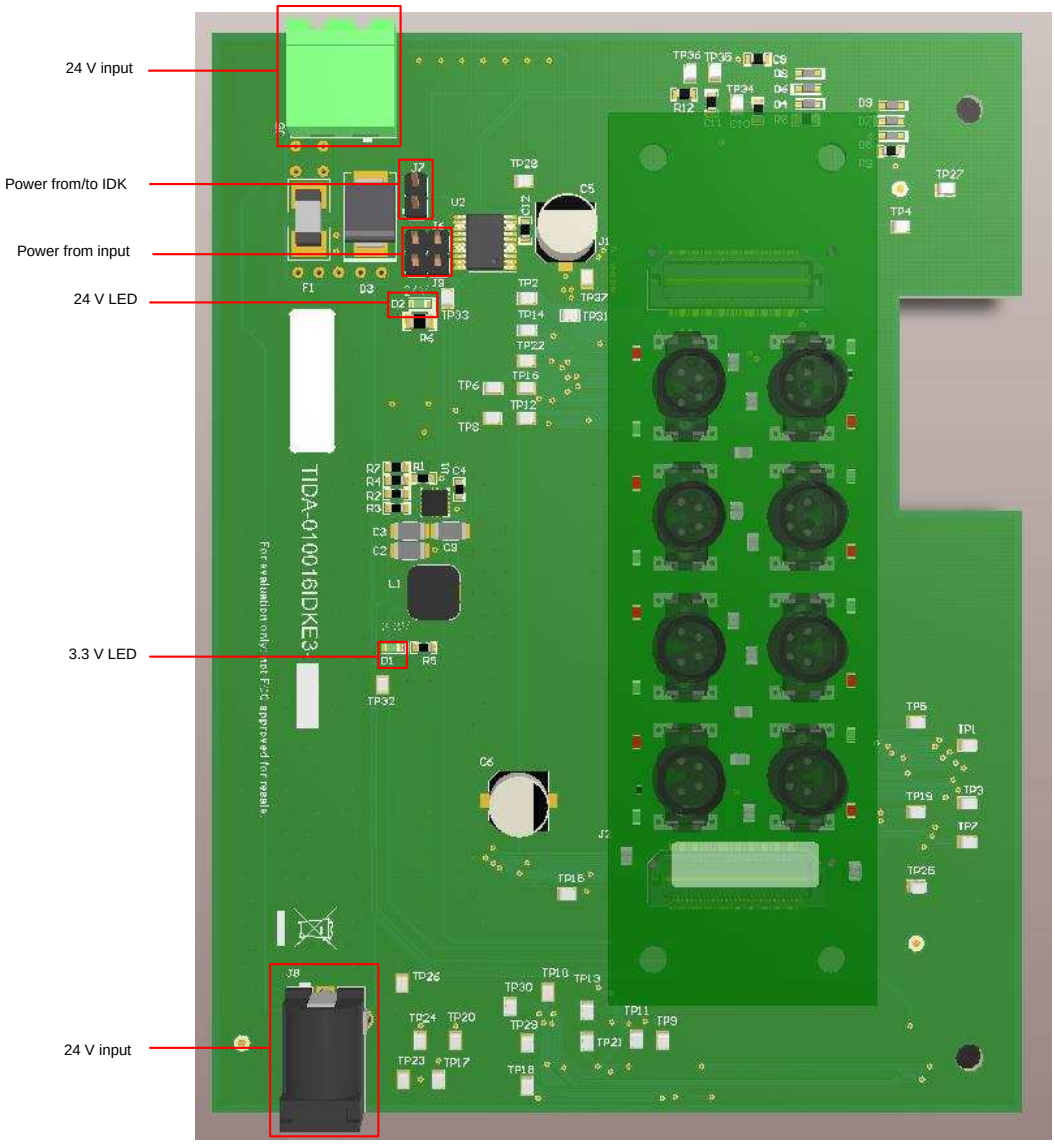


图 14. Power Connectors and Jumpers

3.1.2 Software

For simple testing, the corresponding GPIOs can be tied manually to the necessary level. For full IO-Link operation, a frame-handler is implemented on the PRU and an IO-Link stack is running on the ARM core.

3.2 Testing and Results

3.2.1 Test Setup

To test the different physical parameters, the IO-Link board is connected to 24-V supply without the IDK. The necessary signals for each test are explained in the following sections.

3.2.2 Test Results

3.2.2.1 IO-Link® Wake-Up Pulse

As previously described, the PHY must deliver a wake-up pulse of 80 µs and 500 mA. To test this, the enable signal is tied to 3.3 V and the TX signal is supplied from a function generator. This test is repeated with different polarities, loads, and voltages.

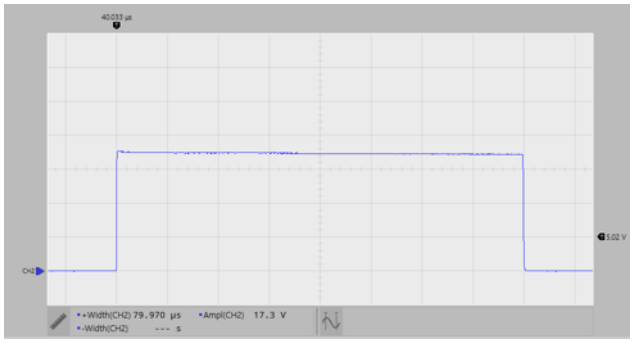


图 15. Testcase TCM_PHYL_INTF_IQWUH: High-Side Driver, Load = 26 Ω, 20-V Supply, 5 V/div, 10 µs/div

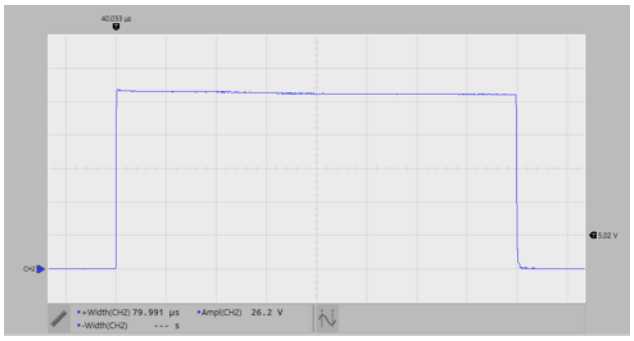


图 16. Testcase TCM_PHYL_INTF_IQWUH: High-Side Driver, Load = 26 Ω, 30-V Supply, 5 V/div, 10 µs/div

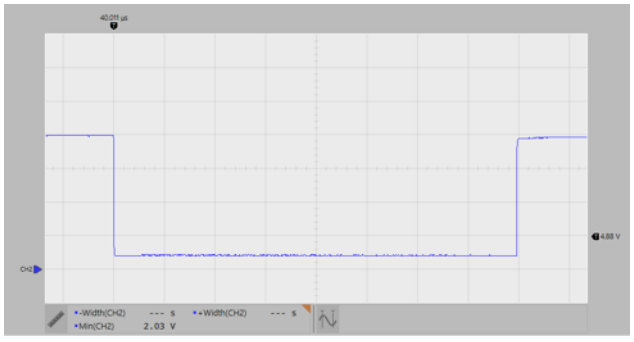


图 17. Testcase TCM_PHYL_INTF_IQWUL: Low-Side Driver, Load = 24 Ω, 20-V Supply, 5 V/div, 10 µs/div

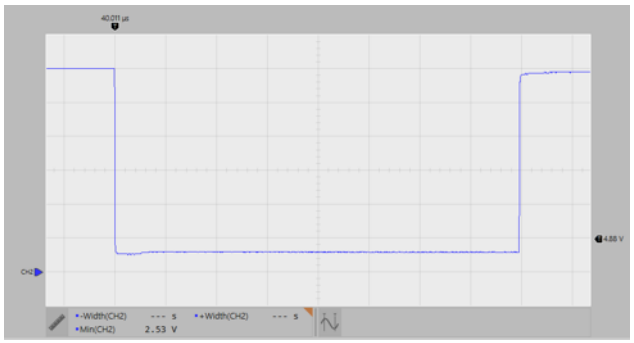


图 18. Testcase TCM_PHYL_INTF_IQWUL: Low-Side Driver, Load = 44 Ω, 30-V Supply, 5 V/div, 10 µs/div

As 图 15 through 图 18 show, the TIOL111 device passes the tests.

3.2.2.2 L+ Turnon Behavior

The turn on of the L+ line is tested by applying a capacitor of 1000 µF, shorted by 150-Ω resistive load. The IO-Link master has to deliver at least 400 mA for 50 ms to pass this test. This load simulates a IO-Link device with a large input capacitor and a static load.

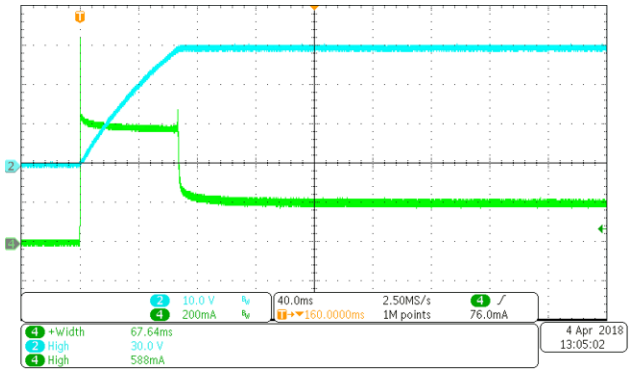


图 19. Testcase TCM_PHYL_INTF_ISIRM: – Power-On Supply Current Capability

图 19 shows the test results. Channel 2 shows the voltage on the L+ line, channel 4 shows the current on L+. As the load is capacitive and resistive, at the beginning the current is limited to 600 mA by the high-side switch, for about 70 ms. After this time, the resistive load remains and draws a current of 200 mA. Since this energy is more than the necessary 400 mA × 50 ms = 20 mA, this test is passed.

However, different IO-Link master implementations behave very different in this test.

3.2.2.3 Current Sink on CQ

To test the current sink, the port to test has to be defined as input. Therefore, the enable signal of the TIOL111 device is tied low, and the TX signal has to be at 3.3 V to enable the current sink. A variable voltage is then applied on the CQ line of the port. The testcase TCM_PHYL_INTF_ILLM defines the test procedure. It is necessary, that the current is below 15 mA below 5.1 V and from 5 to 15 mA for voltage from 5.1 V up to 30 V.

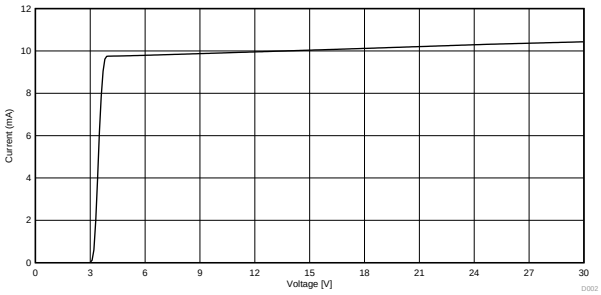


图 20. Input Current on the CQ Line

As the current of the sink is within the given range, the test is passed.

3.2.2.4 Residue Voltage

The test case TCM_PHYL_INTF_IQPKHM tests the voltage drop on the high side of the IO-Link PHY during the wake-up pulse. Therefore the CQ line is loaded with 26 Ω and the wake-up pulse is generated. The voltage on the CQ line has to exceed 13 V to pass this test. This test is done with a L+ voltage of 20 V and 30 V.

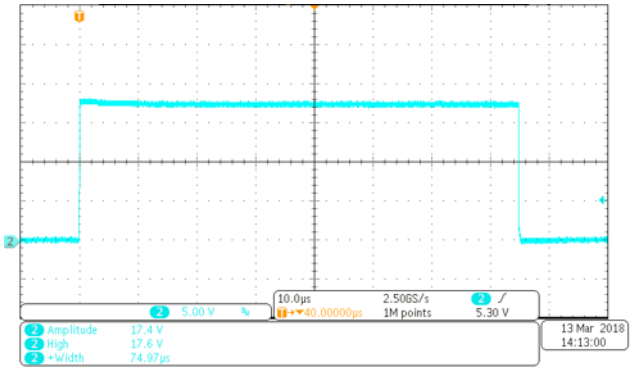


图 21. Testcase TCM_PHYL_INTF_IQPKHM: Wake-Up Current High Side - 20 V L+ Resulting in 17.4 V

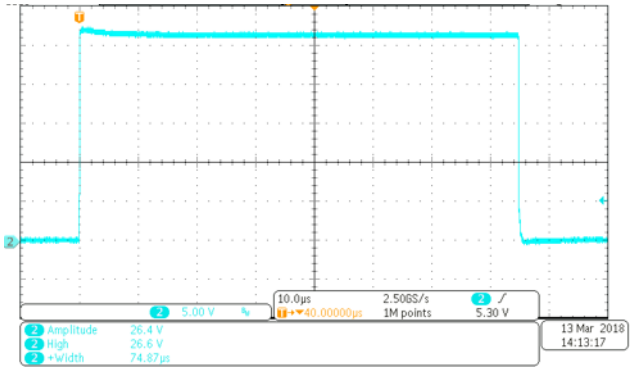


图 22. Testcase TCM_PHYL_INTF_IQPKHM: Wake-Up Current High Side - 30 V L+ Resulting in 26.4 V

As 图 21 and 图 22 show, the voltage is above 13 V, so the test of the high-side driver is passed.

The next relevant test case is TCM_PHYL_INTF_IQPKLM. This test is similar than before, but testing the low-side switch. Therefore the load is 24 Ω for 20 V L+ voltage and 44 Ω for 30 V. The resistor must be connected between L+ and CQ to test the low side. The voltage has to be below 8 V to pass this test.

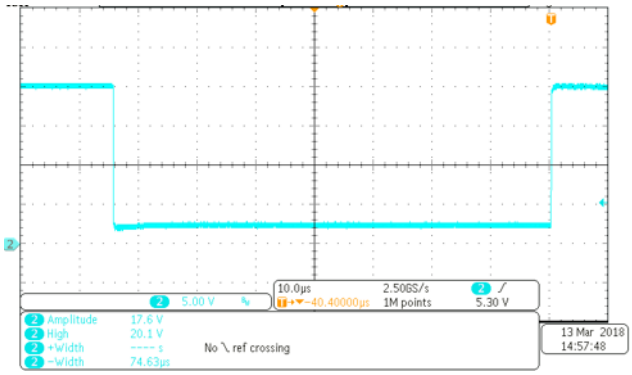


图 23. Testcase TCM_PHYL_INTF_IQPKLM: Wake-Up Current Low Side - 20 V L+ Resulting in 2 V

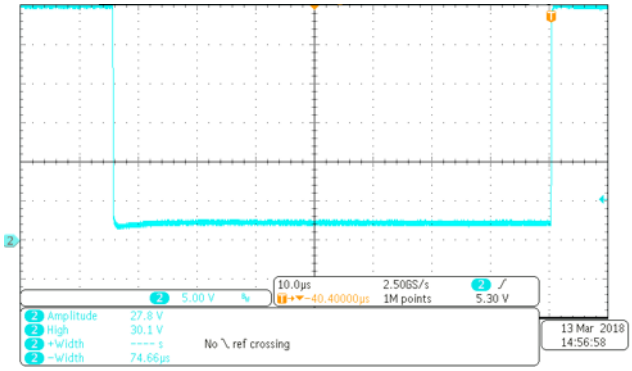


图 24. Testcase TCM_PHYL_INTF_IQPKLM: Wake-Up Current Low Side - 30 V L+ Resulting in 2 V

So all the tests for the current capability during the wake-up pulse are passed.

3.2.2.5 IO-Link® Physical Layer Test Summary

表 8 lists the physical layer test summary and results.

表 8. IO-Link® Physical Layer Test

ID	Name	Configuration	Specification (Clause)	Comment	Result
SDCI_TC_0001	TCM_PHYL_INTF_ISM	The supply current at the Master port is monitored.	See *Section 5.3.2.3*, *Table 6* in *IO-Link Interface and System Specification Version 1.1.2*	Test with 200 mA	20 V: Pass 30 V: Pass
SDCI_TC_0002	TCM_PHYL_INTF_ISIRM	The supply current at the Master port is monitored.		Test with 500 mA	20 V: Pass 30 V: Pass
SDCI_TC_0003	TCM_PHYL_INTF_ILLM	The input current at C/Q at the Master port is monitored.			ILLM (VIM = 5 V, VSM = 20 V): 9.77 mA Pass ILLM (VIM = 5,1 V, VSM = 20 V): 9.77 mA Pass ILLM (VIM = 15 V, VSM = 20 V): 10.04 mA Pass ILLM (VIM = VSM = 20 V): 10.17 mA Pass ILLM (VIM = 5 V, VSM = 30 V): 9.77 mA Pass ILLM (VIM = 5,1 V, VSM = 30 V): 9.77 mA Pass ILLM (VIM = 15 V, VSM = 30 V): 10.04 mA Pass ILLM (VIM = VSM = 30 V): 10.43 mA Pass
SDCI_TC_0004	TCM_PHYL_INTF_VREShigh	The output level at the Master C/Q output is measured.			VRQHM (VSM = 20 V): 1.003 V VRQHM (VSM = 30 V): 1.002 V Pass
SDCI_TC_0005	TCM_PHYL_INTF_VRESLOW	The output level at the Master C/Q output is measured.			VRQLM (VSM = 20 V): 0.984 V VRQLM (VSM = 30 V): 0.983 V Pass
SDCI_TC_0006	TCM_PHYL_INTF_VTHHM	The digital input signal for C/Q input is monitored	See *Section 5.3.2.2*, *Table 5* in *IO-Link Interface and System Specification Version 1.1.2*		VIM@VTHHM (VSM = 20 V): 11.47 V VIM@VTHHM (VSM = 30 V): 11.47 V Pass
SDCI_TC_0007	TCM_PHYL_INTF_VTHLM	The digital input signal for C/Q input is monitored			VIM@VTHLM (VSM = 20 V): 10.75 V VIM@VTHLM (VSM = 30 V): 10.75 V Pass
SDCI_TC_0008	TCM_PHYL_INTF_VHYSM	Comparison of values from SDCI_TC_0006 and SDCI_TC_0007			VHYSM (VSM = 20 V): 0.72 V VHYSM (VSM = 30 V): 0.72 V Pass
SDCI_TC_0009	TCM_PHYL_INTF_IQPKHM	The output level at the Master C/Q output is measured.			VIM (VSM = 20 V): 17.4 V VIM (VSM = 30 V): 26.4 V Pass
SDCI_TC_0010	TCM_PHYL_INTF_IQPKLM	The output level at the Master C/Q output is measured.	See *Section 5.3.2.3*, *Table 6* in *IO-Link Interface and System Specification Version 1.1.2*		VIM (VSM = 20 V): 2.2 V VIM (VSM = 30 V): 2.2 V Pass
SDCI_TC_0299	TCM_PHYL_INTF_VOLTRANGECQ	Test if working after connecting CQ to 0 V and 30 V via 1 Ω	See *Section 5.3.2.2*, *Table 5* - VIL and VIH, in *IO-Link Interface and System Specification Version 1.1.2*		Pass
SDCI_TC_0021	TCM_PHYL_INTF_IQWUH		See *Section 5.3.3.3*, *Table 9* in *IO-Link Interface and System Specification Version 1.1.2*	Wake-up pulse from function generator	VIM@WURQ (VSM = 20 V): 17.3 V VIM@WURQ (VSM = 30 V): 26.2 V Pass
SDCI_TC_0022	TCM_PHYL_INTF_TWUH			Wake-up pulse from function generator	TWUH@WURQ (VSM = 20 V): 80 µs TWUH@WURQ (VSM = 30 V): 80 µs Pass
SDCI_TC_0023	TCM_PHYL_INTF_IQWUL			Wake-up pulse from function generator	VIM@WURQ (VSM = 20 V): 2 V VIM@WURQ (VSM = 30 V): 2.5 V Pass
SDCI_TC_0024	TCM_PHYL_INTF_TWUL			Wake-up pulse from function generator	TWUL@WURQ (VSM = 20 V): 80 µs TWUL@WURQ (VSM = 30 V): 80 µs Pass

3.2.2.6 Current Sense on Each Port

To test the current sense of the TPS4H160 device, each channel is selected by setting the select pins accordingly, the device is powered with 24 V and every channel is loaded with an adjustable current sink. The current sense output is connected to a voltmeter. One channel at a time is tested and the results are plotted in 图 25 and 图 26.

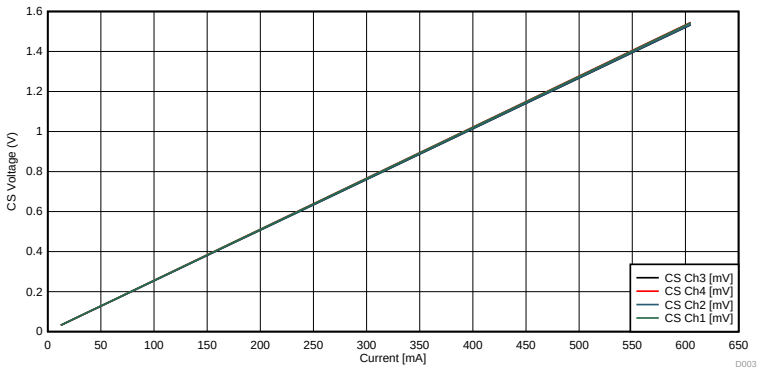


图 25. Output Voltage of TPS4H160 vs Current

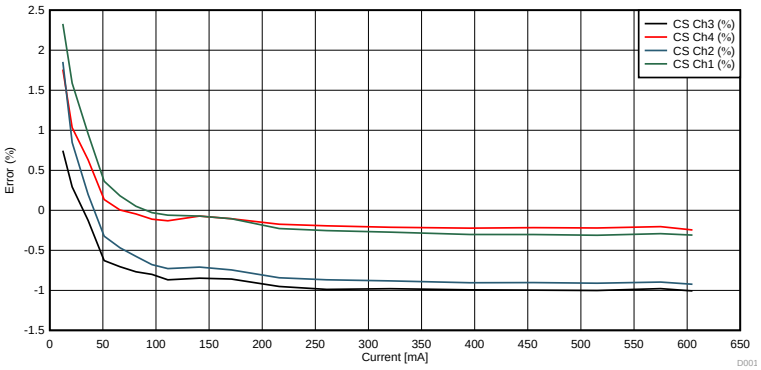


图 26. Error of Current Measurement

The error is calculated by converting the output voltage to a current: I[mA] = 300 / 768 × U × 1000. The error can than be calculated by E[%] = (I_{TPS} – I_{is}) / I_{is}.

3.2.2.7 TPS4H160 Thermal Behavior

The TPS4H160 device is loaded with 1 A per port and all 8 ports are switched on. 图 27 shows the thermal image of the board at room temperature. The design is also able to handle 1 A without overheating at 85 °C ambient temperature.

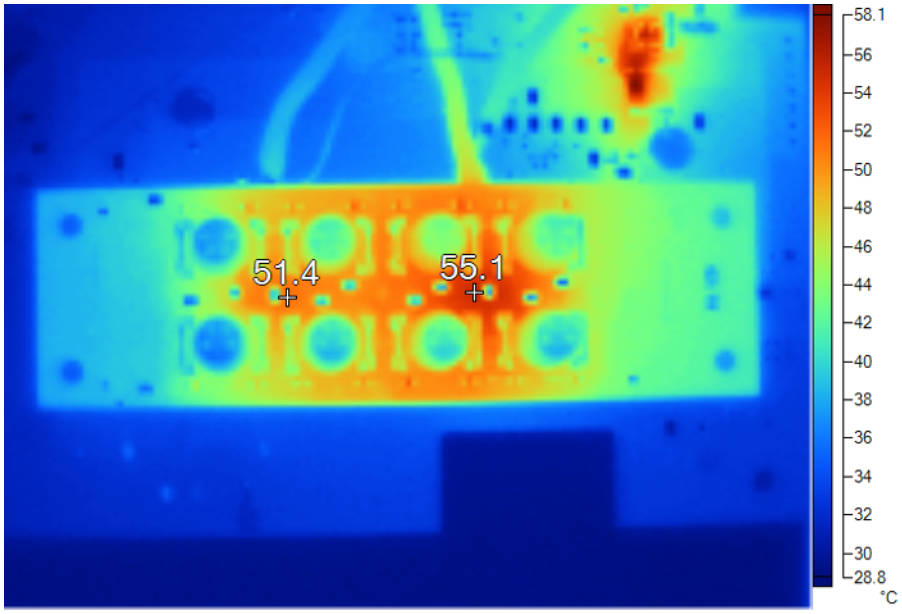


图 27. IO-Link® Master Thermal Image at 1-A Load per Port

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-010016.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-010016.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-010016.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-010016.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-010016.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-010016.

5 Software Files

To download the software files, see the design files at TIDA-010016.

6 Related Documentation

1. IO-Link Consortium, *IO-Link Test Specification Version 1.1.2*
2. IO-Link Consortium, *IO-Link Interface and System Specification Version 1.1.2*
3. IO-Link Consortium, *IO-Link Package 2015 & Corrigendum Version 1.0*
4. Texas Instruments, *Selecting the right industrial communications standard for sensors*

6.1 商标

7 About the Author

STEFFEN GRAF is a systems engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. He earned his master of science in electrical engineering at the University of applied science in Darmstadt, Germany.

修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from A Revision (November 2018) to B Revision **Page**

- 已更改 *将英文原文中的“scaleable”*更改为“*scalable*” 1

Changes from Original (July 2018) to A Revision **Page**

- 已更改 *O-Link* to *IO-Link* 2
- 已更改 data in 表 4 13

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