

N チャネル NexFET™ パワー MOSFET

1 特長

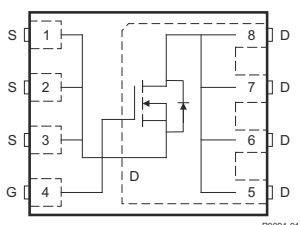
- 5V ゲート・ドライブに最適化
- 非常に低い Q_g および Q_{gd}
- 低い熱抵抗
- アバランシェ定格
- 鉛不使用の端子メッキ処理
- RoHS 準拠
- ハロゲン不使用
- SON 5mm × 6mm プラスチック・パッケージ

2 アプリケーション

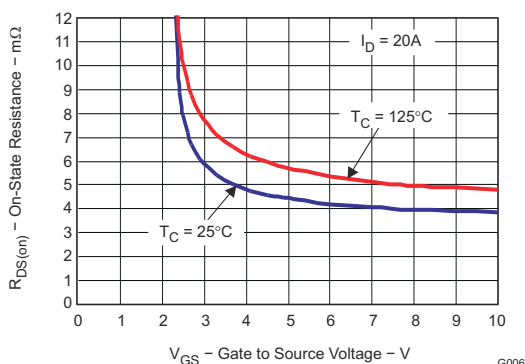
- ネットワーク、テレコム、およびコンピューティング・システムのポイント・オブ・ロード同期整流降圧
- 同期整流または制御 FET アプリケーション

3 概要

NexFET™ パワー MOSFET はパワー・コンバージョン・アプリケーションにおいて損失を最小限とするよう設計され、5V ゲート・ドライブ・アプリケーションに最適化されています。



上面図



$R_{DS(on)}$ と V_{GS} との関係

製品概要

| パラメータ | 説明 | 値 | 単位 |
|--------------|-------------------|-----------------|--------|
| V_{DS} | ドレイン - ソース間電圧 | 25 | V |
| Q_g | ゲートの合計電荷 (4.5V) | 6.8 | nC |
| Q_{gd} | ゲート電荷、ゲート - ドレイン間 | 1.3 | nC |
| $R_{DS(on)}$ | ドレイン - ソース間オン抵抗 | $V_{GS} = 3V$ | 5.4 mΩ |
| | | $V_{GS} = 4.5V$ | 4.6 mΩ |
| | | $V_{GS} = 8V$ | 3.9 mΩ |
| $V_{GS(th)}$ | スレッシュホールド電圧 | 1.1 | V |

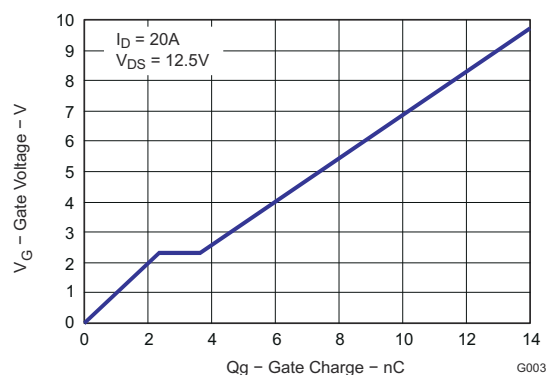
製品情報

| 製品名 | パッケージ | メディア | 数量 | 配送 |
|------------|----------------------------|------------|------|-------------|
| CSD16322Q5 | SON 5mm × 6mm プラスチック・パッケージ | 13 インチ・リール | 2500 | テープ・アンド・リール |

絶対最大定格

| $T_A = 25^\circ C$ (特に記述のない限り) | | 値 | 単位 |
|--------------------------------|--|-----------|------------|
| V_{DS} | ドレイン - ソース間電圧 | 25 | V |
| V_{GS} | ゲート - ソース間電圧 | +10 / -8 | V |
| I_D | 連続ドレイン電流、 $T_C = 25^\circ C$ | 97 | A |
| | 連続ドレイン電流 ⁽¹⁾ | 21 | A |
| I_{DM} | パルス・ドレイン電流、 $T_A = 25^\circ C$ ⁽²⁾ | 136 | A |
| P_D | 消費電力 ⁽¹⁾ | 3.1 | W |
| T_J, T_{STG} | 動作時の接合部温度、保存温度 | -55 ~ 150 | $^\circ C$ |
| E_{AS} | アバランシェ・エネルギー、単一パルス $I_D = 50A, L = 0.1mH, R_G = 25\Omega$ | 125 | mJ |

- $R_{\theta JA} = 39^\circ C/W$ (標準値、厚さ 0.06 インチ (1.52mm) の FR4 PCB 上の面積 1 平方インチ (6.45cm²)、厚さ 2oz (0.071mm) の Cu パッドに実装した場合)。
- パルス幅 $\leq 300\mu s$ 、デューティ・サイクル $\leq 2\%$



ゲート電荷



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision B (May 2010) to Revision C (October 2023) | Page |
|---|------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 7 |
| Changes from Revision A (April 2010) to Revision B (May 2010) | Page |
| • Changed $R_{DS(on)}$, $V_{GS} = 3\text{ V}$ in the Electrical Characteristics table From: 7 To: 7.2 in the max column..... | 3 |
| Changes from Revision * (August 2009) to Revision A (April 2010) | Page |
| • 絶対最大定格の注 1 を $R_{\theta JA} = 39^{\circ}\text{C/W}$ から $R_{\theta JA} = 39^{\circ}\text{C/W}$ (標準値) に変更..... | 1 |
| • Changed 図 7-1 text From: $R_{\theta JA} = 99^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 98^{\circ}\text{C/W}$ | 4 |
| • Changed 図 7-10 text From: $R_{\theta JA} = 99^{\circ}\text{C/W}$ To: Typical $R_{\theta JA} = 98^{\circ}\text{C/W}$ | 4 |
| • Changed 図 7-11 X-axis values..... | 4 |

5 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

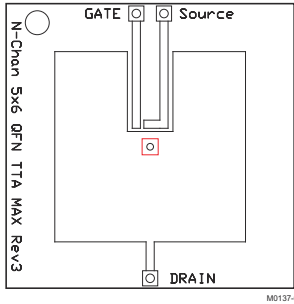
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------------------|---|------|------|-----|------|
| Static Characteristics | | | | | | |
| B _V DSS | Drain to Source Voltage | V _{GS} = 0 V, I _D = 250 μA | 25 | | | V |
| I _{DSS} | Drain to Source Leakage Current | V _{GS} = 0 V, V _{DS} = 20 V | | | 1 | μA |
| I _{GSS} | Gate to Source Leakage Current | V _{DS} = 0 V, V _{GS} = +10/-8 V | | | 100 | nA |
| V _{GS(th)} | Gate to Source Threshold Voltage | V _{DS} = V _{GS} , I _D = 250 μA | 0.9 | 1.1 | 1.4 | V |
| R _{DS(on)} | Drain to Source On Resistance | V _{GS} = 3 V, I _D = 20 A | | 5.4 | 7.2 | mΩ |
| | | V _{GS} = 4.5 V, I _D = 20 A | | 4.6 | 5.8 | mΩ |
| | | V _{GS} = 8 V, I _D = 20 A | | 3.9 | 5 | mΩ |
| g _{fs} | Transconductance | V _{DS} = 15 V, I _D = 20 A | | 106 | | S |
| Dynamic Characteristics | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} = 0 V, V _{DS} = 12.5 V, f = 1 MHz | 1050 | 1365 | | pF |
| C _{oss} | Output Capacitance | | 740 | 950 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | 55 | 70 | | pF |
| R _G | Series Gate Resistance | | 1.1 | 2.2 | | Ω |
| Q _g | Gate Charge Total (4.5 V) | V _{DS} = 12.5 V, I _D = 20 A | 6.8 | 9.7 | | nC |
| Q _{gd} | Gate Charge Gate to Drain | | 1.3 | | | nC |
| Q _{gs} | Gate Charge Gate to Source | | 2.4 | | | nC |
| Q _{g(th)} | Gate Charge at V _{th} | | 1.3 | | | nC |
| Q _{oss} | Output Charge | V _{DS} = 13 V, V _{GS} = 0 V | | 17 | | nC |
| t _{d(on)} | Turn On Delay Time | V _{DS} = 12.5 V, V _{GS} = 4.5 V, I _D = 20 A, R _G = 2 Ω | 6.1 | | | ns |
| t _r | Rise Time | | 10.7 | | | ns |
| t _{d(off)} | Turn Off Delay Time | | 12.3 | | | ns |
| t _f | Fall Time | | 3.7 | | | ns |
| Diode Characteristics | | | | | | |
| V _{SD} | Diode Forward Voltage | I _{SD} = 20 A, V _{GS} = 0 V | 0.8 | 1 | | V |
| Q _{rr} | Reverse Recovery Charge | V _{DD} = 13 V, I _F = 20 A, di/dt = 300 A/μs | | 19 | | nC |
| t _{rr} | Reverse Recovery Time | V _{DD} = 13 V, I _F = 20 A, di/dt = 300 A/μs | | 21 | | ns |

6 Thermal Characteristics

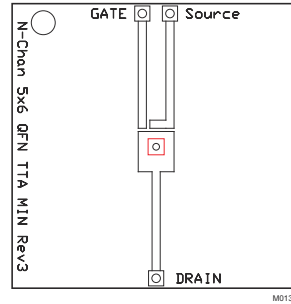
(T_A = 25°C unless otherwise stated)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|---|-----|-----|-----|------|
| R _{θJC} | Thermal Resistance Junction to Case ⁽¹⁾ | | | 2.4 | °C/W |
| R _{θJA} | Thermal Resistance Junction to Ambient ^{(1) (2)} | | | 50 | °C/W |

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



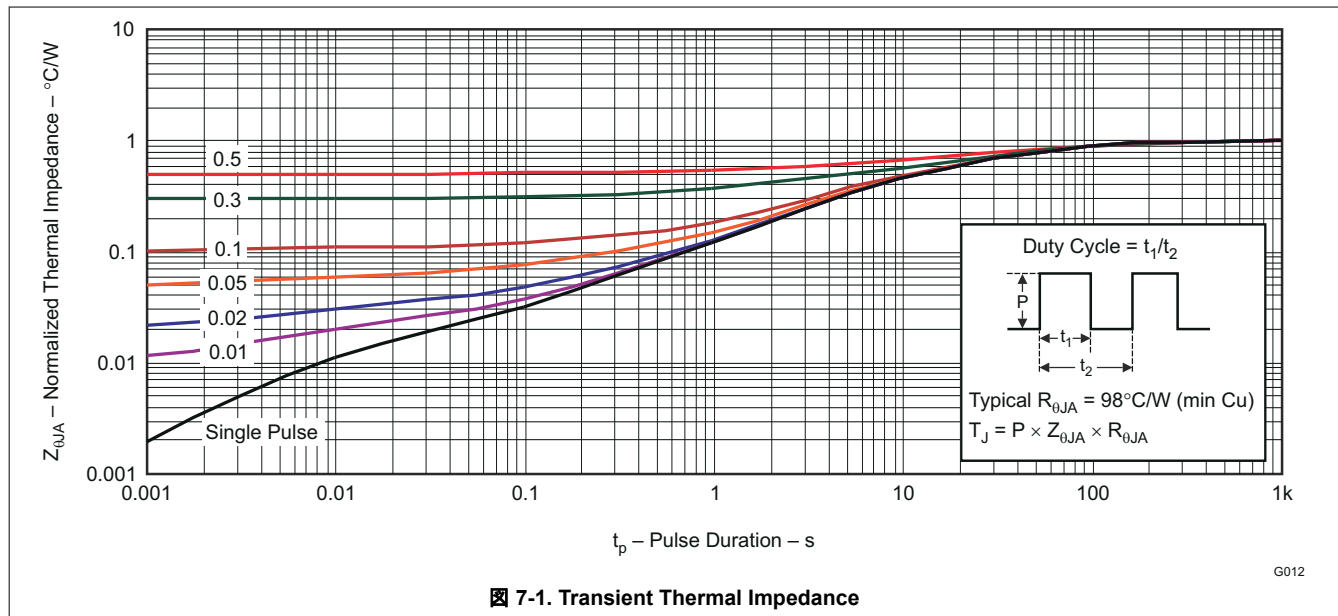
Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on 1 inch²
(6.45 cm²) of 2-oz. (0.071-
mm thick) Cu.



Max $R_{\theta JA} = 123^{\circ}\text{C/W}$ when
mounted on minimum pad
area of 2-oz. (0.071-mm
thick) Cu.

7 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



7 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

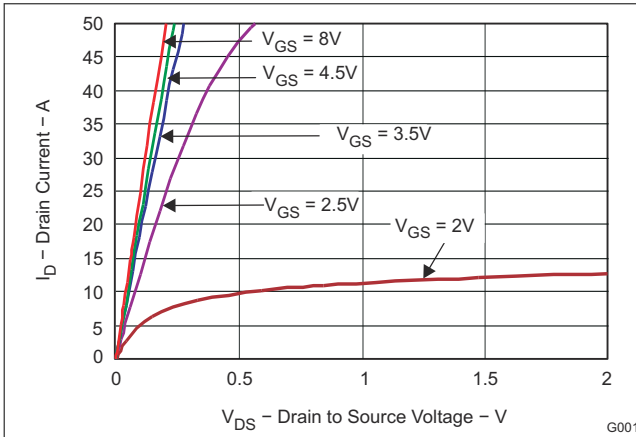


Figure 7-2. Saturation Characteristics

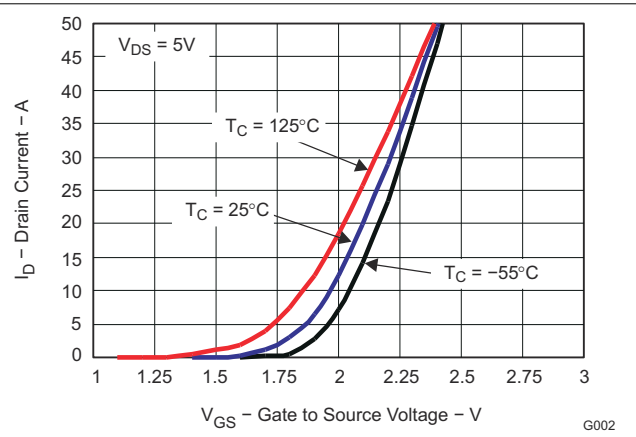


Figure 7-3. Transfer Characteristics

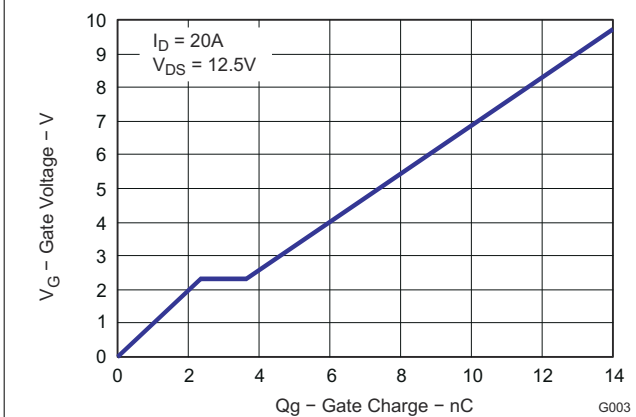


Figure 7-4. Gate Charge

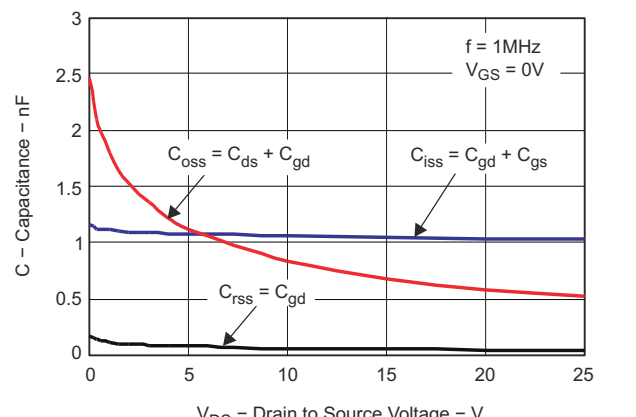


Figure 7-5. Capacitance

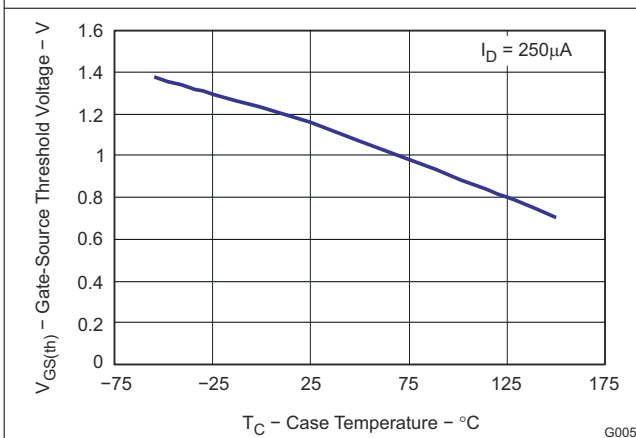


Figure 7-6. Threshold Voltage vs. Temperature

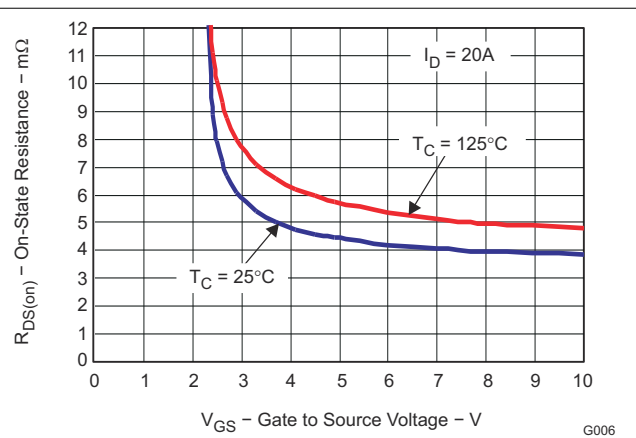


Figure 7-7. On-State Resistance vs. Gate to Source Voltage

7 Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

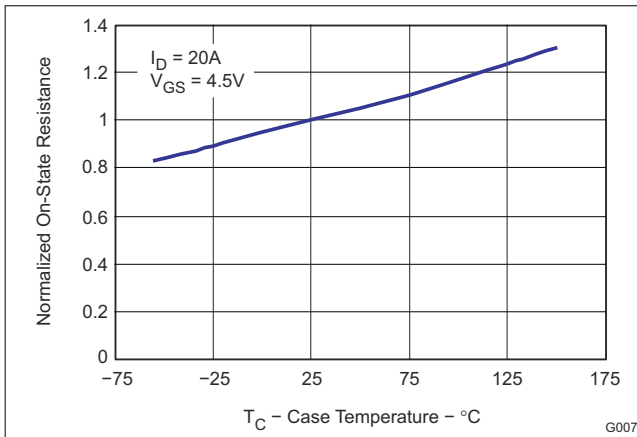


Figure 7-8. Normalized On-State Resistance vs. Temperature

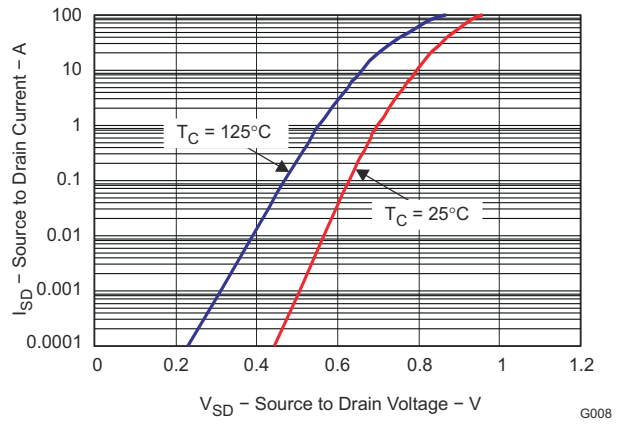


Figure 7-9. Typical Diode Forward Voltage

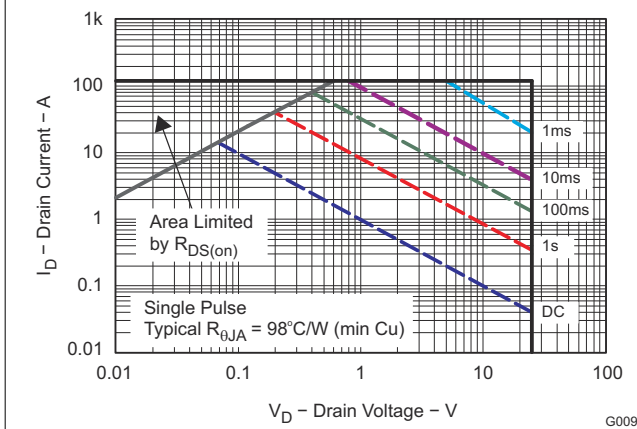


Figure 7-10. Maximum Safe Operating Area

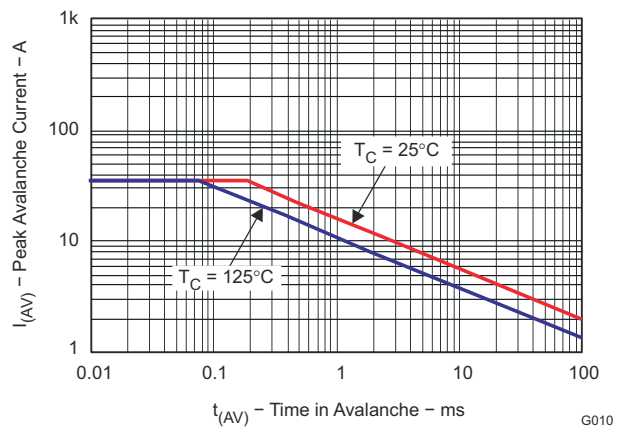


Figure 7-11. Single Pulse Unclamped Inductive Switching

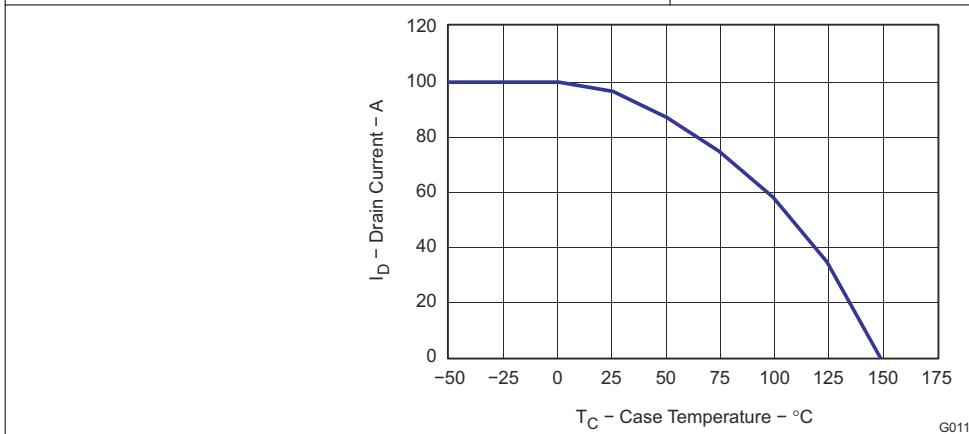


Figure 7-12. Maximum Drain Current vs. Temperature

8 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| CSD16322Q5 | ACTIVE | VSON-CLIP | DQH | 8 | 2500 | RoHS-Exempt & Green | SN | Level-1-260C-UNLIM | -55 to 150 | CSD16322 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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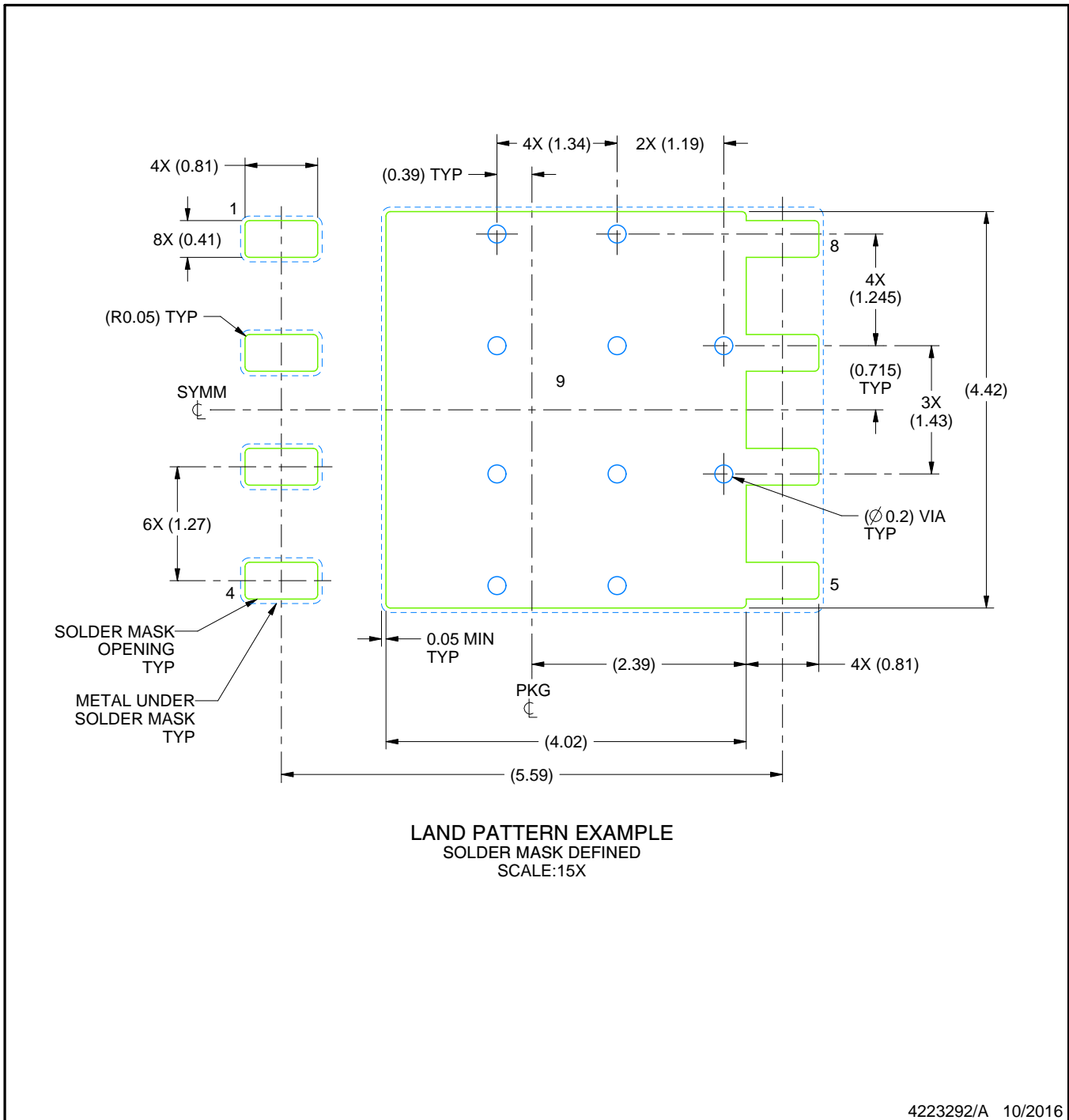
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EXAMPLE BOARD LAYOUT

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES: (continued)

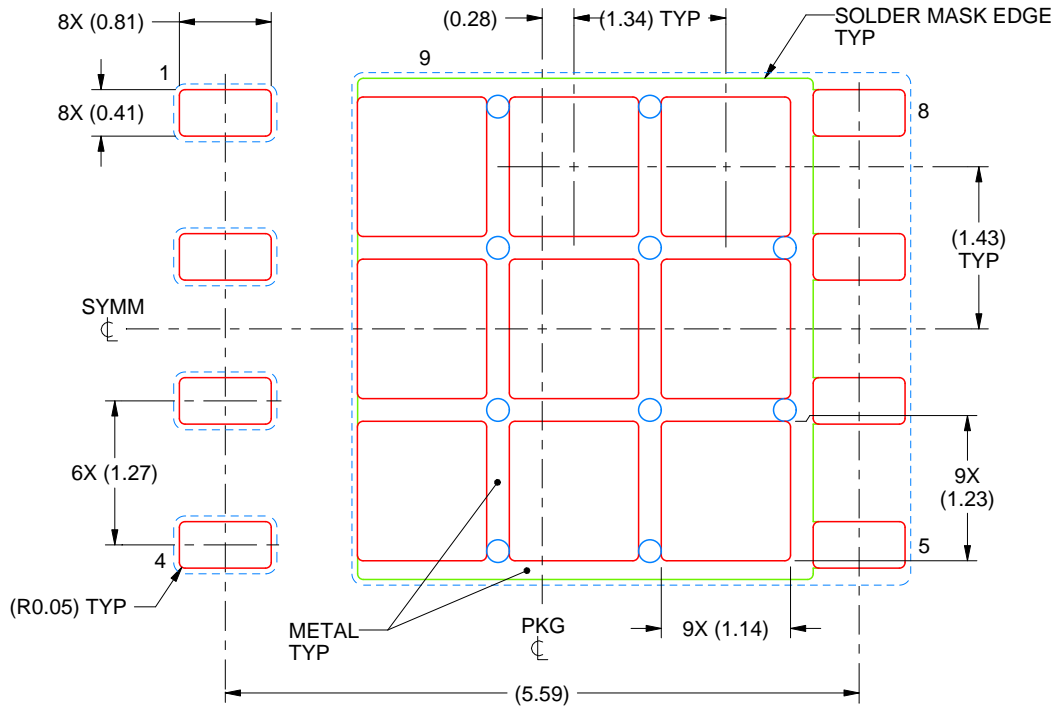
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DQH0008A

VSON-CLIP - 1.05 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
71% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4223292/A 10/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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