TEXAS INSTRUMENTS
ESD341
JAJSOL1A – APRIL 2022 – REVISED JULY 2022

ESD341 1 チャネル ±30kV ESD 保護ダイオード、0201 パッケージ

1 特長

- IEC 61000-4-2 レベル 4 ESD 保護
  - 30kV 接触放電
  - 30kV エアギャップ放電
- IEC 61000-4-5 サージ保護
  - 5.4A (8/20µs)
- IO 容量:
  - 0.66pF (標準値)
- DC ブレークダウン電圧:±6.2V (標準値)
- 超低リーク電流:100nA (最大値)
- 低い ESD クランプ電圧:10.2V (16A TLP の場合)
- 低挿入損失:5GHz (–3dB 帯域幅、DPL)
- 最大 3.4Gbps の高速インターフェイスをサポート
- 産業用温度範囲:–40℃～+125℃
- 省スペースの業界標準 0201 フットプリント (0.6mm × 0.3mm × 0.3mm)

2 アプリケーション

- 最終製品:
  - ウェアラブル
  - スマート・スピーカ
  - ポータブル・エレクトロニクス
  - 小型家電
  - ラップトップおよびデスクトップ PC
  - テレビ、モニタ
  - ヘッド・ユニット
  - 後部座席用エンターテインメント
  - ドッキング・ステーション
- インターフェイス:
  - USB 2.0
  - USB 3.0
  - HDMI 1.4 および 2.0
  - LVDS
  - DisplayPort
  - SIM カード

3 概要

ESD341 は、HDMI 1.4 回路保護用の双方向 TVS ESD 保護ダイオードです。ESD341 は、IEC 61000-4-2 国際規格で規定されている最大レベル (レベル 4) の ESD 耐性を備えています。

このデバイスの IO 容量は 0.66pF (標準値) で、最高 3.4Gbps の高速インターフェイス保護を実現し、HDMI 1.4b などのプロトコルをサポートしています。低い動的抵抗および低いクランピング電圧により、過渡現象に対してシステム・レベルの保護を確保します。

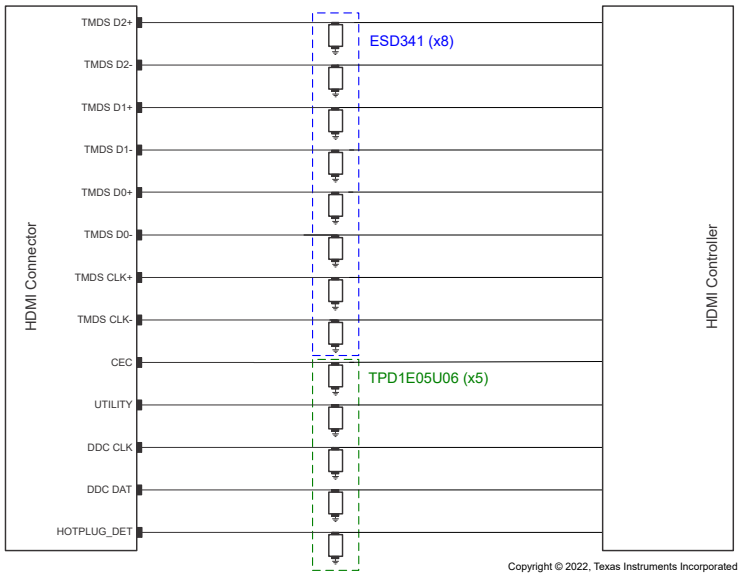
30kV の ESD 定格と 5.4A のサージ耐性を備えており、小型パッケージで堅牢な過渡保護を提供し、ポータブル電子機器やウェアラブルなどスペースに制約のあるアプリケーションで 3.6V の電源レールを保護します。

ESD341 は、業界標準の 0201 (DPL) パッケージで供給されます。

製品情報 (1)

部品番号	パッケージ	本体サイズ (公称)
ESD341	X2SON (2)	0.60mm × 0.30mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2022) to Revision A (July 2022)	Page
• データシートのステータスを「事前情報」から*「量産データ」に変更*	1

5 Pin Configuration and Functions

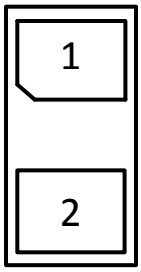


図 5-1. DPL Package, 2-Pin X2SON (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
2	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

(1) I = input, O = output

6 Specifications

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Peak Pulse (2) (3)	IEC 61000-4-5 power (t_p - 8/20 µs)		54	W
	IEC 61000-4-5 Current (t_p - 8/20 µs)		5.4	A
T_A	Ambient Operating Temperature	-40	125	°C
T_J	Junction Temperature	-40	125	°C
T_{stg}	Storage Temperature	-65	155	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Voltages are with respect to GND unless otherwise noted.
(3) Measured at 25℃

6.1 ESD Ratings—JEDEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2500	V
		Charged device model (CDM), per JEDEC specification JS-002	±1000	V

6.2 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IO}	Input pin voltage	Pin 1 to 2 or Pin 2 to 1	-3.6		3.6	V
T_A	Operating free-air temperature		-40		125	°C

6.3 Thermal Information

THERMAL METRIC (1)		ESD341 DPL (X2SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	356.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	208.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	136.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	3.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	135.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	NA	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	Pin 1 to Pin 2 or Pin 2 to Pin 1	-3.6		3.6	V
V_{BRF}	Break-down voltage	I_{IO} = 1 mA, Pin 1 to Pin 2	5	6.2	7.2	V
V_{BRR}	Break-down voltage	I_{IO} = -1 mA, Pin 2 to Pin 1	-7.2	-6.2	-5	V
V_{HOLD}	Holding voltage (2)	TLP, Pin 1 to Pin 2 or Pin 2 to Pin 1		6.2		V
V_{Clamp_TLP}	Clamp voltage with TLP (2)	I_{PP} = 1 A, TLP, Pin 1 to Pin 2		6.3		V
		I_{PP} = 5 A, TLP, Pin 1 to Pin 2		7.4		
		I_{PP} = 16 A, TLP, Pin 1 to Pin 2		10.2		
		I_{PP} = 1 A, TLP, Pin 2 to Pin 1		6.3		
		I_{PP} = 5 A, TLP, Pin 2 to Pin 1		7.4		
		I_{PP} =16 A, TLP, Pin 2 to Pin 1		10.2		
V_{Clamp_Surge}	Clamp voltage with surge strike (4)	I_{PP} = 5.4 A, t_p = 8/20 µs , Pin 1 to Pin 2 or Pin 2 to Pin 1		8.8		V
I_{LEAK}	Leakage current	V_{IO} = 3.6 V, Pin 1 to Pin 2 or Pin 2 to Pin 1		5	100	nA
R_{DYN}	Dynamic resistance (3)	Pin 1 to Pin 2		0.25		Ω
		Pin 2 to Pin 1				
C_L	Line capacitance	V_{IO} = 0 V; f = 1 MHz, Pin 1 to Pin 2, T_A = 25℃		0.66		pF

(1) Typical parameters are measured at 25℃
(2) Transition line pulse with 100 ns width and 10 ns rise and fall time
(3) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A
(4) Nonrepetitive current pulse 8 to 20 µs exponentially decaying waveform according to IEC 61000-4-5

6.5 Typical Characteristics

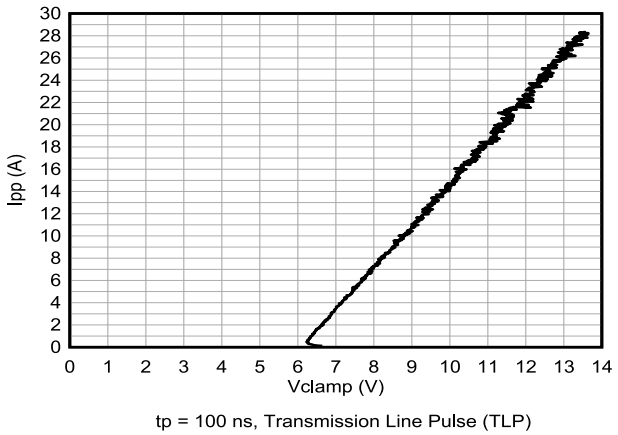


図 6-1. Positive TLP Curve

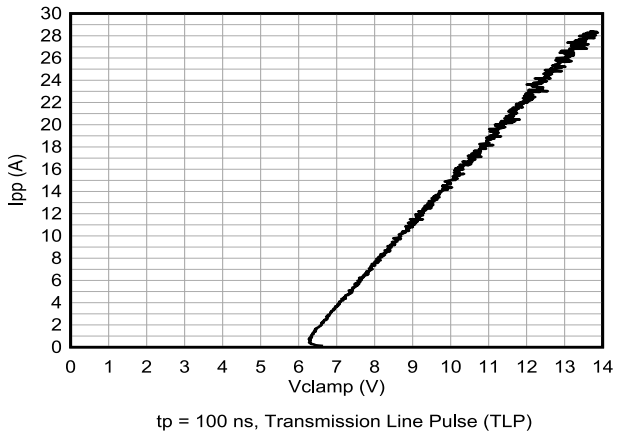


図 6-2. Negative TLP Curve

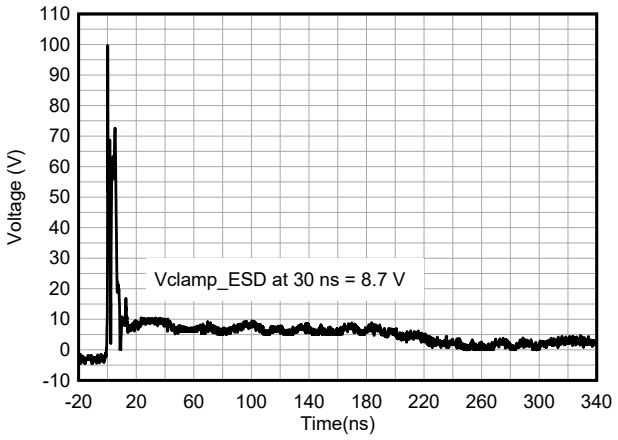


図 6-3. +8-kV Clamped IEC Waveform

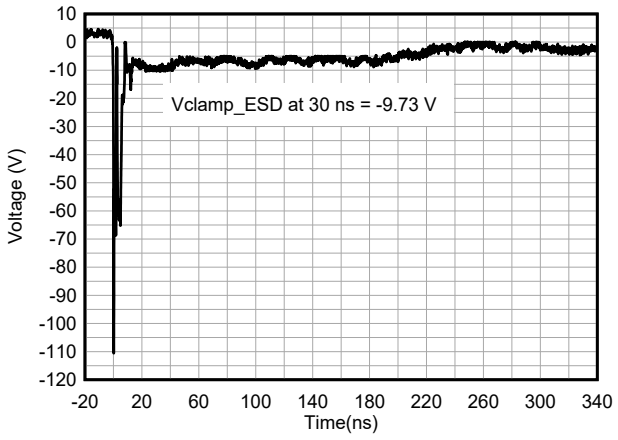


図 6-4. -8-kV Clamped IEC Waveform

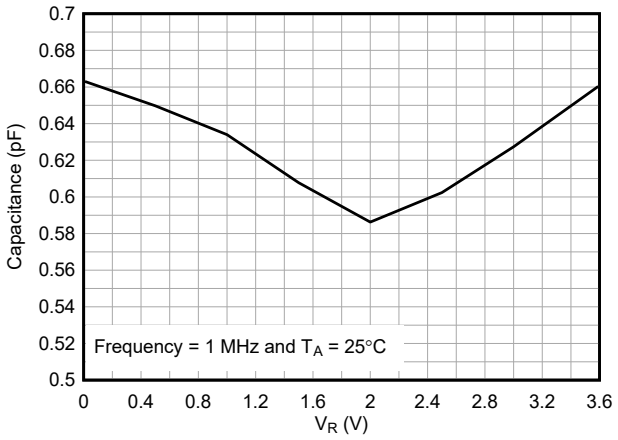


図 6-5. Bias Voltage vs. Capacitance

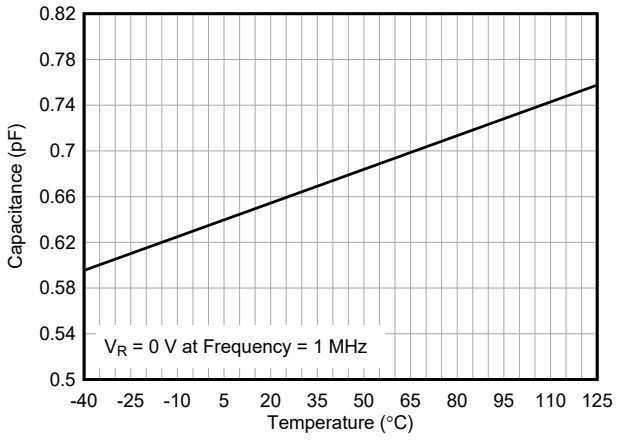


図 6-6. Temperature vs. Capacitance

6.5 Typical Characteristics (continued)

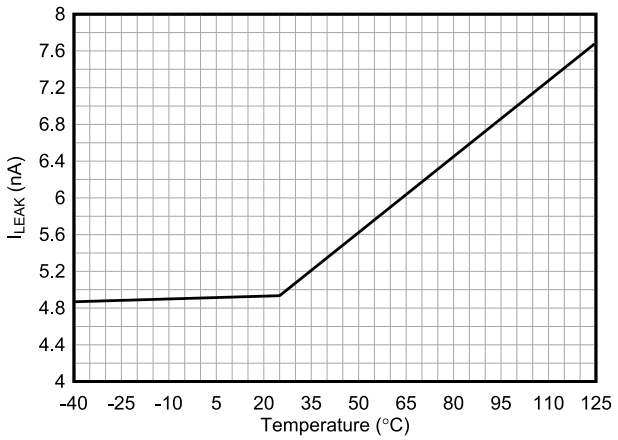


図 6-7. Temperature vs. Leakage Current

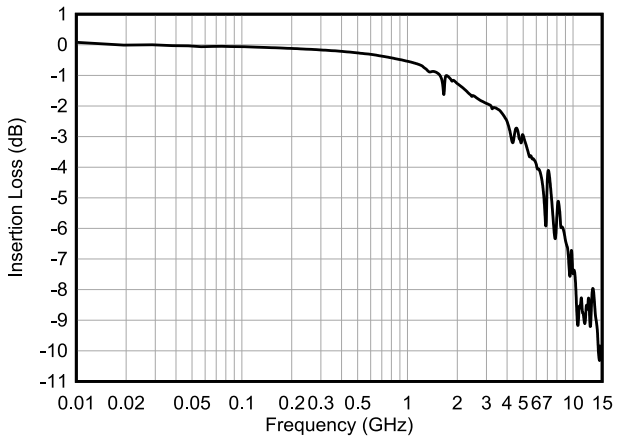


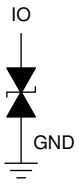
図 6-8. Insertion Loss

7 Detailed Description

7.1 Overview

The ESD341 device is a bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low capacitance allows this device to protect high-speed signal pins including HDMI 1.4b.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±30 kV contact and ±30 kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 5.4 A and 54 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.3 IO Capacitance

The capacitance between each I/O pin to ground is 0.66 pF (typical). This device supports data rates up to 3.4 Gbps.

7.3.4 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±6.2 V (typical). This DC breakdown voltage ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.5 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 100 nA (maximum) with a bias of ±3.6 V.

7.3.6 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 7.4 V (I_{PP} = 5 A, TLP).

7.3.7 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 3.4 Gbps, because of the extremely low IO capacitance.

7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.4 Device Functional Modes

The ESD341 device is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±30 kV (air or contact) can be directed to ground through the internal diode network. When the voltages on the protected line fall below the V_{HOLD} of ESD341 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ESD341 is a diode type TVS which provides a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage (V_{CLAMP}) to a safe level for the protected IC.

8.2 Typical Application

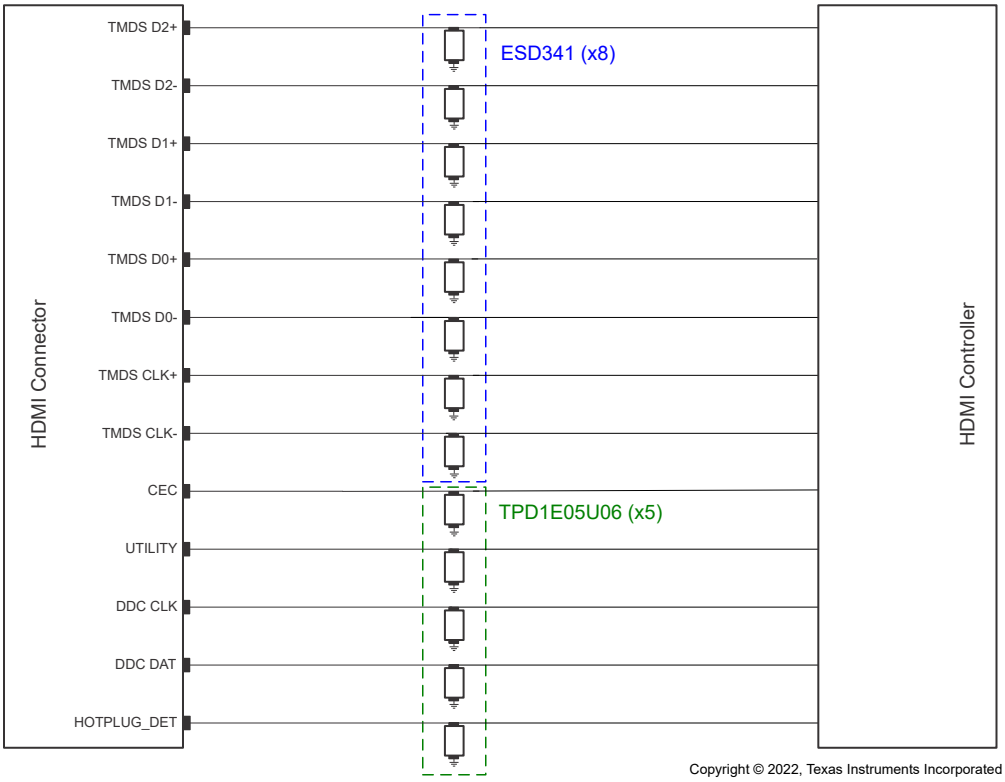


図 8-1. HDMI 1.4 Application

8.2.1 Design Requirements

For this design example, 8 ESD341 devices and 5 TPD1E05U06 devices are being used in an HDMI 1.4 application, which provides a complete port protection scheme.

表 8-1 lists the parameters for the HDMI 1.4 application.

表 8-1. Design Parameters

DESIGN PARAMETER	VALUE
TMDS signal range on pins	0 V to 3.6 V
Other signal range on pins	0 V to 5 V
Operating frequency	1.7 GHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The ESD341 supports signal ranges between –3.6 V and 3.6 V, which supports the TMDS signals. The TPD1E05U06 supports signal ranges between 0 V and 5.5 V, which supports the other signals (CEC, UTILITY, DDC CLK, DDC DAT, and HOTPLUG_DET) in the HDMI 1.4 application.

8.2.2.2 Operating Frequency

The ESD341 has a 0.66 pF (typical) capacitance, which supports the 3.4 Gbps data rate needed for the HDMI 1.4 application.

8.2.3 Application Curves

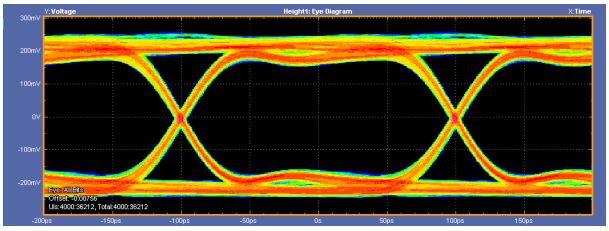


図 8-2. Data Rate > 3.4 Gbps Eye Diagram (Bare Board)

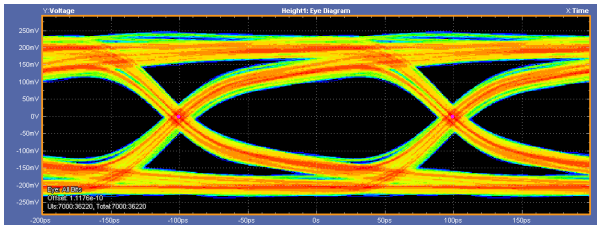


図 8-3. Data Rate > 3.4 Gbps Eye Diagram (with ESD341)

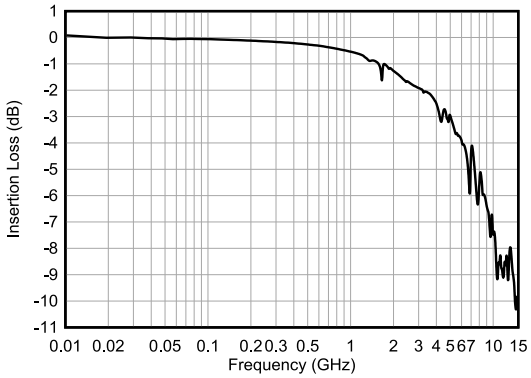


図 8-4. Insertion Loss

9 Power Supply Recommendations

This is a passive TVS diode-based ESD protection device, therefore there is no need to power it. Take care that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement of the ESD protection device is as close to the connector as possible
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector
- Route the protected traces as straight as possible
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible
  - Electric fields tend to build up on corners, increasing EMI coupling
- If pin 1 or pin 2 is connected to ground, use a thick and short trace for this return path

10.2 Layout Example

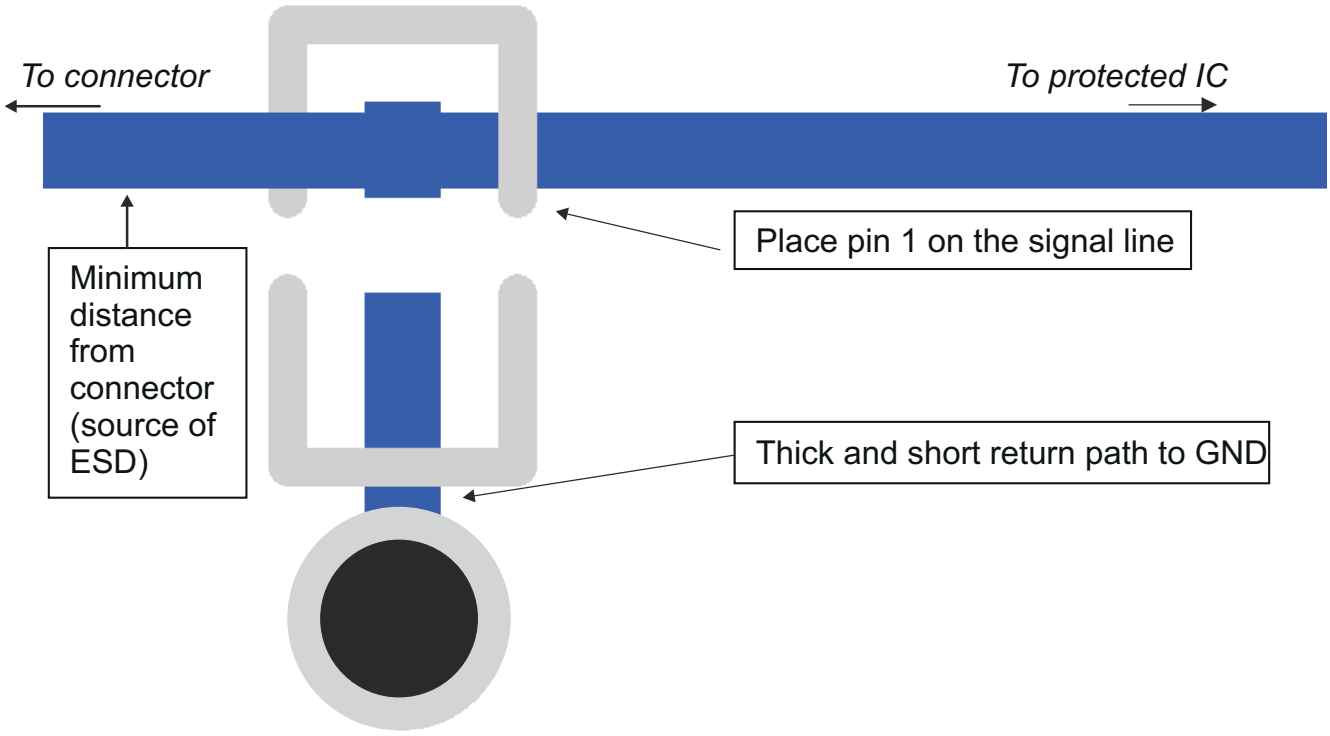


図 10-1. Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *ESD Layout Guide* application reports
- Texas Instruments, *Generic ESD Evaluation Module* user's guide
- Texas Instruments, *Picking ESD Diodes for Ultra High-Speed Data Lines* application reports
- Texas Instruments, *Reading and Understanding an ESD Protection* data sheet

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.4 Trademarks

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

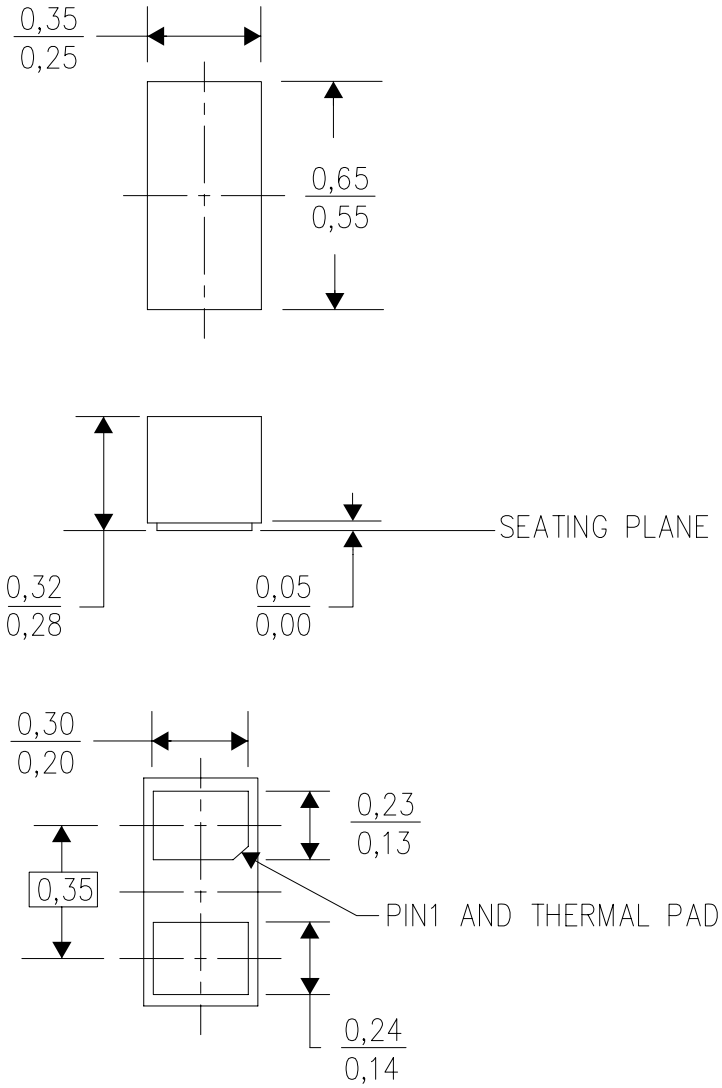
TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

MECHANICAL DATA

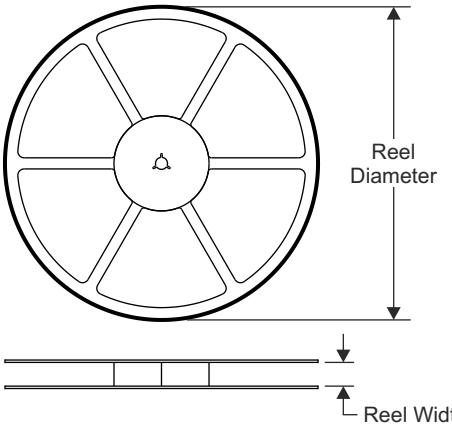
DPL (R–PX2SON–N2) PLASTIC SMALL OUTLINE NO–LEAD



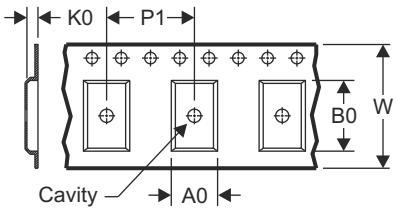
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.

12.1 Tape and Reel Information

REEL DIMENSIONS

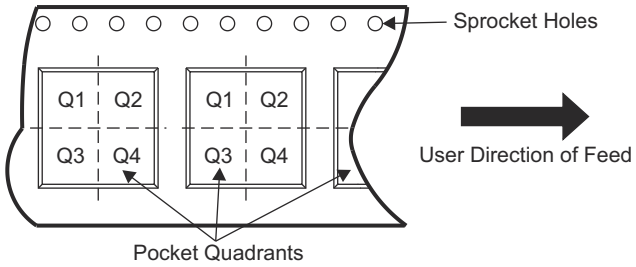


TAPE DIMENSIONS



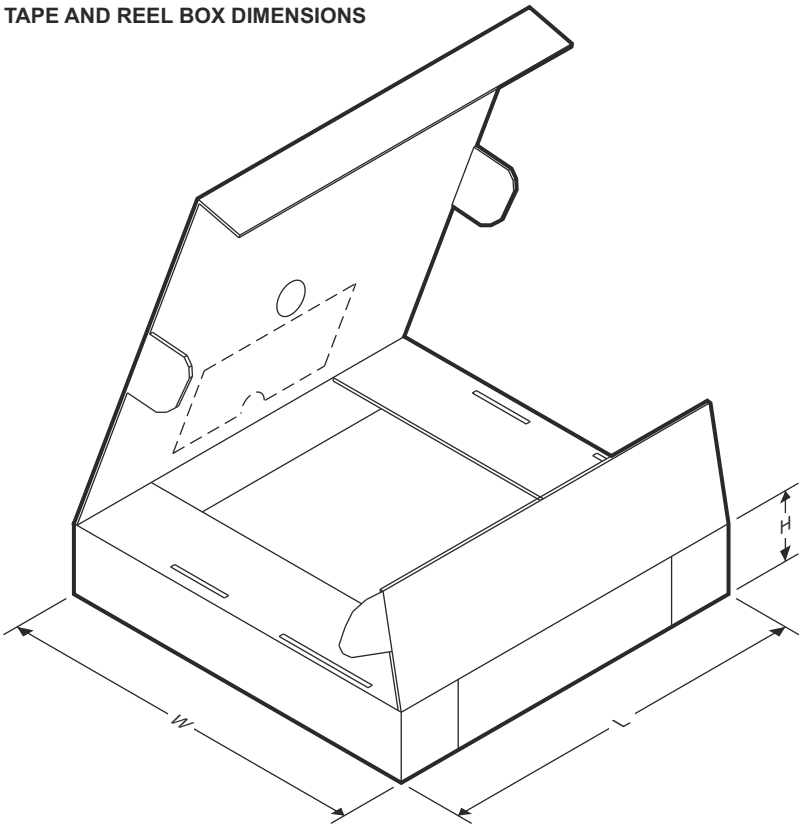
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ESD341DPLR	X2SON	DPL	2	15000	178	8.4	0.36	0.66	0.33	0.2	8	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ESD341DPLR	X2SON	DPL	2	15000	205	200	33

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ESD341DPLR	ACTIVE	X2SON	DPL	2	15000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265