ISO724xC-Q1 高速、クワッド チャネル デジタル アイソレータ

1 特長

- 25Mbps の信号速度オプション
  - 低いチャネル間の出力スキュー:
    最大値 1ns
  - 低いパルス幅歪み (PWD) :
    最大値 2ns
  - 低ジッタ成分:25Mbps で標準値 1ns
- 選択可能なデフォルト出力 (ISO7240CF)
- 定格動作電圧での寿命 > 25 年 (「絶縁特性曲線」を参照)
- 4kV の ESD 保護
- 3.3V または 5V 電源で動作
- -40℃～+125℃の動作温度範囲
- 安全関連の認証:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL 1577 部品認定プログラム
  - IEC 61010-1 認定、IEC 62368-1 認定

2 アプリケーション

- ファクトリ オートメーション
  - Modbus
  - Profibus™
  - DeviceNet™ データ バス
- コンピュータ ペリフェラル インターフェイス
- サーボ制御インターフェイス
- データ アクイジション

3 概要

ISO7240CF-Q1、ISO7241C-Q1、ISO7242C-Q1 の各デバイスは、複数のチャネル構成と出力イネーブル機能を備えたクワッド チャネル デジタル アイソレータです。これらのデバイスは、テキサス インスツルメンツ独自の二酸化ケイ素 (SiO_2) 絶縁バリアで分離されたロジック入出力バッファを備えています。これらのデバイスは、絶縁型電源と組み合わせて使用することで、高電圧を遮断し、グランドを絶縁し、ノイズ電流がローカル グランドに入り込んでノイズに敏感な回路に干渉したり損傷を与えたりすることを防止します。

ISO7240C-Q1 ファミリのデバイスは、同じ方向に 4 チャネルを備えています。ISO7241C-Q1 ファミリのデバイスは、同じ方向に 3 チャネル、反対方向に 1 チャネルを備えています。ISO7242C-Q1 ファミリのデバイスは、各方向に 2 チャネルを備えています。

接尾辞 C (C オプション) のデバイスには、TTL 入力スレッショルドと、遷移パルスがデバイスの出力に渡されるのを防ぐノイズ フィルタが入力に備わっています。接尾辞 M (M オプション) のデバイスには、CMOS $V_{CC}/2$ 入力スレッショルドが備わっていますが、入力ノイズ フィルタはなく、追加の伝搬遅延も発生しません。

ISO7240CF デバイスは、ピン 7 に入力ディセーブル機能を備え、CTRL ピン (ピン 10) に High または Low が選択可能なフェイルセーフ出力機能を備えています。フェイルセーフ出力は、CTRL ピンにロジック High が印加された場合、またはピンが未接続のままである場合、ロジック High になります。CTRL ピンにロジック Low 信号が印加されると、フェイルセーフ出力はロジック Low 出力状態になります。ISO7240CF デバイスの入力ディセーブル機能により、絶縁バリアを通過してデータが出力に渡されるのを防ぎます。入力がディセーブルされるか、V_{CC1} がパワーダウンすると、出力は CTRL ピンによって設定されます。

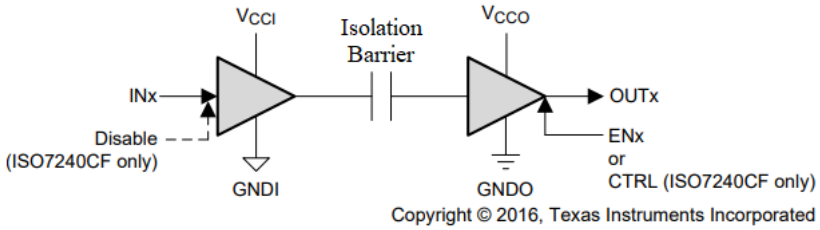
これらのデバイスは、どちらの側でも 3.3V または 5V 電源から電力を供給でき、任意の組み合わせが可能です。信号入力ピンは、使用される電源電圧レベルに関係なく 5V 許容です。

これらのデバイスは、-40℃～+125℃の周囲温度範囲で動作するように特性評価されています。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)	パッケージ サイズ(2)
ISO7240CF-Q1	DW (SOIC、16)	10.30mm × 7.50mm	10.30mm × 10.30mm
ISO7241C-Q1			
ISO7242C-Q1			

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



V_{CCI} および GNDI は、それぞれ入力チャネルの電源およびグランド接続です。
V_{CCO} および GNDO は、それぞれ出力チャネルの電源およびグランド接続です。

概略回路図

Table of Contents

4 Pin Configurations and Functions

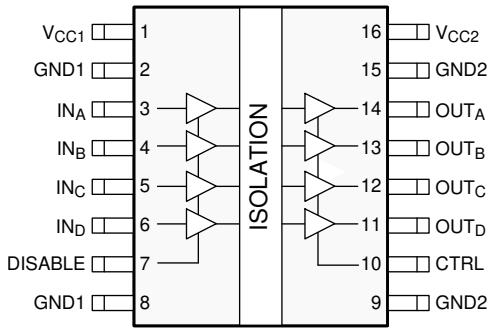


図 4-1. ISO7240CF-Q1 DW Package 16-Pin SOIC Top View

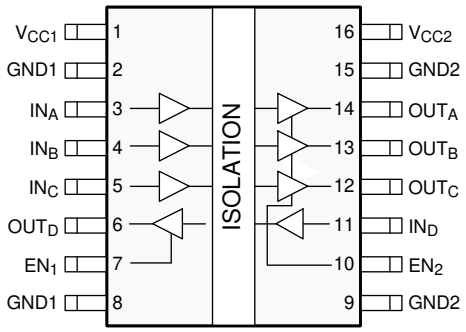


図 4-2. ISO7241C-Q1 DW Package 16-Pin SOIC Top View

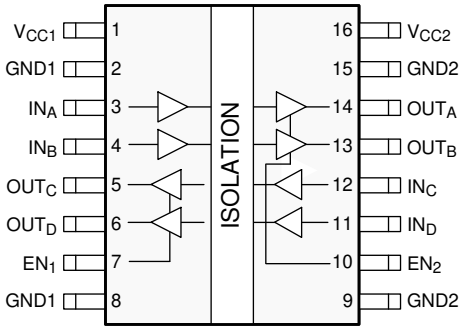


図 4-3. ISO7242C-Q1 DW Package 16-Pin SOIC Top View

表 4-1. Pin Functions

PIN				Type[1]	DESCRIPTION
NAME	ISO7240CF-Q1	ISO7241C-Q1	ISO7242C-Q1		
CTRL	10	—	—	I	Failsafe output control. Output state is determined by CTRL pin when DISABLE is high or V_{CC1} is powered down. Output is high when CTRL is high or open and low when CTRL is low.
DISABLE	7	—	—	I	Input disable. All input pins are disabled when DISABLE is high and enabled when DISABLE is low or open.
EN	—	—	—	I	Output enable. All output pins are enabled when EN is high or open and disabled when EN is low.
EN_1	—	7	7	I	Output enable 1. Output pins on side 1 are enabled when EN_1 is high or open and disabled when EN_1 is low.
EN_2	—	10	10	I	Output enable 2. Output pins on side-2 are enabled when EN_2 is high or open and disabled when EN_2 is low.
GND1	2, 8	2, 8	2, 8	—	Ground connection for V_{CC1}
GND2	9, 15	9, 15	9, 15	—	Ground connection for V_{CC2}
IN_A	3	3	3	I	Input, channel A
IN_B	4	4	4	I	Input, channel B
IN_C	5	5	12	I	Input, channel C
IN_D	6	11	11	I	Input, channel D
NC	—	—	—	—	No Connect pins are floating with no internal connection
OUT_A	14	14	14	O	Output, channel A
OUT_B	13	13	13	O	Output, channel B
OUT_C	12	12	5	O	Output, channel C
OUT_D	11	6	6	O	Output, channel D
V_{CC1}	1	1	1	—	Power supply, V_{CC1}
V_{CC2}	16	16	16	—	Power supply, V_{CC2}

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

See(1)

				VALUE	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}			–0.5 to 6	V
V_I	Voltage at IN, OUT, EN, DISABLE, CTRL			–0.5 to 6	V
ESD	Electrostatic discharge	Human-Body Model	All pins	±4	kV
		Field-Induced-Charged Device Model		±1	
T_J	Maximum junction temperature			150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	3.15		5.5	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current	–4			mA
t_{ui}	Input pulse width	40			ns
$1/t_{ui}$	Signaling rate	0	30(1)	25	Mbps
V_{IH}	High-level input voltage (IN, DISABLE, CTRL, EN)	2		V_{CC}	V
V_{IL}	Low-level input voltage (IN, DISABLE, CTRL, EN)	0		0.8	V
T_A	Operating free-air temperature	-40		125	°C
H	External magnetic field-strength immunity per IEC 61000-4-8 and IEC 61000-4-9 certification			1000	A/m

(1) Typical value at room temperature and well-regulated power supply.
(2) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.4 Thermal Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air	Low-K Thermal Resistance(1)		168		°C/W
		High-K Thermal Resistance		68.6		
θ_{JB}	Junction-to-Board Thermal Resistance			33.5		°C/W
θ_{JC}	Junction-to-Case Thermal Resistance			33.9		°C/W

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface mount packages.

5.5 Power Ratings

$V_{CC1} = V_{CC2} = 5.5$ V, $T_J = 150$C, $C_L = 15$ pF, Input a 25-Mbps 50% duty cycle square wave

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Device power dissipation, ISO724xC				220	mW

5.6 Safety-Related Certifications

VDE	CSA	UL
Plan to certify according to DIN EN IEC 60747-17 (VDE 0884-17)	Plan to certify according to IEC 62368-1	Plan to certify according to UL 1577 Component Recognition Program
Certificate planned	Certificate planned	Certificate planned

5.7 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C, see Thermal Characteristics			124	mA
		$R_{\theta JA}$ = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C, see Thermal Characteristics			190	
T_S	Safety temperature				150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

5.8 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	4	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.008	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	400	V
	Material group		II	
	Overvoltage category	Rated mains voltage ≤150 V_{RMS}	I-IV	
		Rated mains voltage ≤300 V_{RMS}	I-III	
		Rated mains voltage ≤400 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17):BASIC				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	560	V_{PK}
V_{IOTM}	Maximum transient isolation voltage	V_{TEST} = V_{IOTM} t = 60 s (qualification), t = 1 s (100% production)	4000	V_{PK}
q_{pd}	Apparent charge(3)	Method a: After I/O safety test subgroup 2/3. Vini = VIOTM, tini = 60 s; Vpd(m) = 1.2 × VIOR	≤5	pC
		Method a: After environmental tests subgroup 1, Vini = VIOTM, tini = 60 s; Vpd(m) = 1.3 × VIORM , tm = 10 s,	≤5	
		Method b1: At routine test (100% production) Vini = VIOTM, tini = 1 s; Vpd(m) = 1.5 × VIORM , tm = 1 s,	≤5	
C_{IO}	Barrier capacitance, input to output(4)	VI = 0.4 sin (2πft), f = 1 MHz	1	pF
R_{IO}	Isolation resistance, input to output(4)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 2500\ V_{RMS}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO} = 3000\ V_{RMS}$, t = 1 s (100% production)	2500	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for *basic electrical insulation* only within the maximum operating ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Apparent charge is electrical discharge caused by a partial discharge (pd).
(4) All pins on each side of the barrier tied together creating a two-terminal device

5.9 Electrical Characteristics: V_{CC1} and V_{CC2} at 5-V Operation

, over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240CF	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		1	3	mA
		25 Mbps			7	10.5	
	ISO7241C	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		6.5	11	mA
		25 Mbps			12	18	
	ISO7242C	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		25 Mbps			15	24	
I_{CC2}	ISO7240CF	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_2 at 3 V		15	22	mA
		25 Mbps			17	25	
	ISO7241C	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		13	20	mA
		25 Mbps			18	28	
	ISO7242C	Quiescent	$V_I = V_{CC}$ or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V		10	16	mA
		25 Mbps			15	24	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA	V_{CC} – 0.8			V
			I_{OH} = –20 µA	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
			I_{OL} = 20 µA			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2πft), f=2MHz		2		pF
CMTI	Common-mode transient immunity		$V_I = V_{CC}$ or 0 V; 図 6-5	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.10 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
I_{CC1}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_2 at 3 V		0.5	1.2	mA
		25 Mbps			3	5	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		4	7	mA
		25 Mbps			6.5	11	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	
		25 Mbps			9	14	
I_{CC2}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_2 at 3 V		9.5	15	mA
		25 Mbps			10.5	17	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		8	13	mA
		25 Mbps			11.5	18	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, all channels, no load, EN_1 at 3 V, EN_2 at 3 V		6	10	
		25 Mbps			9	14	
ELECTRICAL CHARACTERISTICS							
I_{OFF}	Sleep mode output current		EN at 0 V, single channel		0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA	V_{CC} – 0.4			V
			I_{OH} = –20 µA	V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA			0.4	V
			I_{OL} = 20 µA			0.1	
$V_{I(HYS)}$	Input voltage hysteresis				150		mV
I_{IH}	High-level input current		IN from 0 V or V_{CC}			10	µA
I_{IL}	Low-level input current			–10			
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2πft), f=2MHz		2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V; 図 6-5	25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.11 Electrical Characteristics: V_{CC1} at 3.3-V, V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			0.5	1.2	mA
		25 Mbps				3	5	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			4	7	mA
		25 Mbps				6.5	11	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6	10	mA
		25 Mbps				9	14	
I_{CC2}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			15	22	mA
		25 Mbps				17	25	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			13	20	mA
		25 Mbps				18	28	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			10	16	mA
		25 Mbps				15	24	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA	ISO7240	V_{CC} – 0.4			V
				ISO724x (5-V side)	V_{CC} – 0.8			
			I_{OH} = –20 µA		V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.4	V
			I_{OL} = 20 µA				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current				–10			
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2πft), f=2MHz			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V; 図 6-5		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.12 Electrical Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT								
I_{CC1}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			1	3	mA
		25 Mbps				7	10.5	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6.5	11	mA
		25 Mbps				12	18	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			10	16	mA
		25 Mbps				15	24	
I_{CC2}	ISO7240CF	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_2 at 3 V			9.5	15	mA
		25 Mbps				10.5	17	
	ISO7241C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			8	13	mA
		25 Mbps				11.5	18	
	ISO7242C	Quiescent	V_I = V_{CC} or 0 V, All channels, no load, EN_1 at 3 V, EN_2 at 3 V			6	10	mA
		25 Mbps				9	14	
ELECTRICAL CHARACTERISTICS								
I_{OFF}	Sleep mode output current		EN at 0 V, Single channel			0		µA
V_{OH}	High-level output voltage		I_{OH} = –4 mA	ISO7240	V_{CC} – 0.4			V
				ISO724x (5-V side)	V_{CC} – 0.8			
			I_{OH} = –20 µA		V_{CC} – 0.1			
V_{OL}	Low-level output voltage		I_{OL} = 4 mA				0.4	V
			I_{OL} = 20 µA				0.1	
$V_{I(HYS)}$	Input voltage hysteresis					150		mV
I_{IH}	High-level input current		IN from 0 V to V_{CC}				10	µA
I_{IL}	Low-level input current				–10			
C_I	Input capacitance to ground		IN at VCC, VI = 0.4 sin (2πft), f=2MHz			2		pF
CMTI	Common-mode transient immunity		V_I = V_{CC} or 0 V; 図 6-5		25	50		kV/µs

(1) For the 5-V operation, V_{CC1} or V_{CC2} is specified from 4.5 V to 5.5 V.
For the 3-V operation, V_{CC1} or V_{CC2} is specified from 3.15 V to 3.6 V.

5.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See 図 6-1	25		56	ns
PWD	Pulse-width distortion $\lvert t_{PHL} - t_{PLH} \rvert$ (1)				4	
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7240C, ISO7241C			3.5	ns
		ISO7242C			4	
t_r	Output signal rise time	See 図 6-1		2		ns
t_f	Output signal fall time			2		ns
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See 図 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See 図 6-3		18		µs
t_{wake}	Wake time from input disable	See 図 6-4		15		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.14 Switching Characterstics: V_{CC1} and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See 図 6-1	18		45	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$				5	
$t_{sk(pp)}$	Part-to-part skew (2)				8	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7240C, ISO7241C			3	ns
		ISO7242C			4	
t_r	Output signal rise time	See 図 6-1		2.4		ns
t_f	Output signal fall time			2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See 図 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See 図 6-3		12		µs
t_{wake}	Wake time from input disable	See 図 6-4		15		µs

(1) Also referred to as pulse skew.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.15 Switching Characteristics: V_{CC1} at 3.3-V and V_{CC2} at 5-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See 図 6-1		20		51	ns
PWD	Pulse-width distortion(1) $\lvert t_{PHL} - t_{PLH} \rvert$	See 図 6-1	ISO7240C, ISO7241C			3	ns
			ISO7242C			4	
$t_{sk(pp)}$	Part-to-part skew (2)					10	ns
$t_{sk(o)}$	Channel-to-channel output skew (3)	ISO7240C, ISO7241C				3	ns
		ISO7242C				4	
t_r	Output signal rise time	See 図 6-1			2.4		ns
t_f	Output signal fall time				2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See 図 6-2			15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output				15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				15	25	
t_{fs}	Failsafe output delay time from input power loss	See 図 6-3			12		µs
t_{wake}	Wake time from input disable	See 図 6-4			15		µs

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(3) $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

5.16 Switching Characteristics: V_{CC1} at 5-V, V_{CC2} at 3.3-V Operation

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay	See 図 6-1	20		50	ns
PWD(1)	See 図 6-1	ISO7240C, ISO7241C			3	
		ISO7242C			4	
PWD	See 図 6-1				3	ns
$t_{sk(pp)}$	Part-to-part skew (2)				10	ns
t_r	Output signal rise time	See 図 6-1		2.4		ns
t_f	Output signal fall time			2.3		
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See 図 6-2		15	25	ns
t_{PZH}	Propagation delay, high-impedance-to-high-level output			15	25	
t_{PLZ}	Propagation delay, low-level-to-high-impedance output			15	25	
t_{PZL}	Propagation delay, high-impedance-to-low-level output			15	25	
t_{fs}	Failsafe output delay time from input power loss	See 図 6-3		18		µs
t_{wake}	Wake time from input disable	See 図 6-4		15		µs

(1) Also known as pulse skew
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.17 Insulation Characteristics Curves

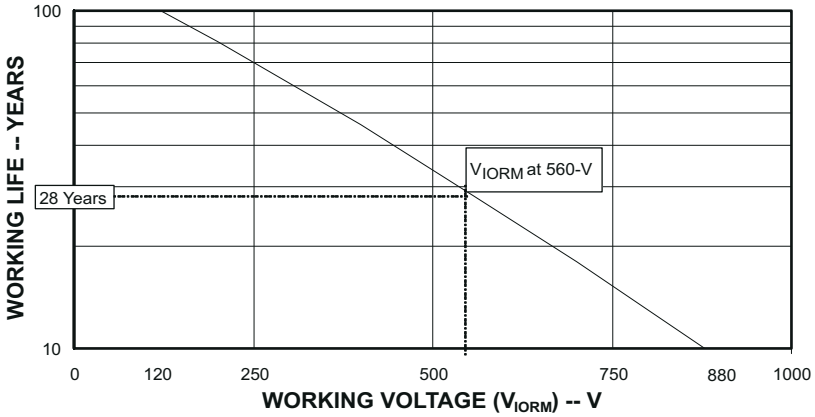


図 5-1. Time Dependent Dielectric Breakdown Testing Results

5.18 Typical Characteristic

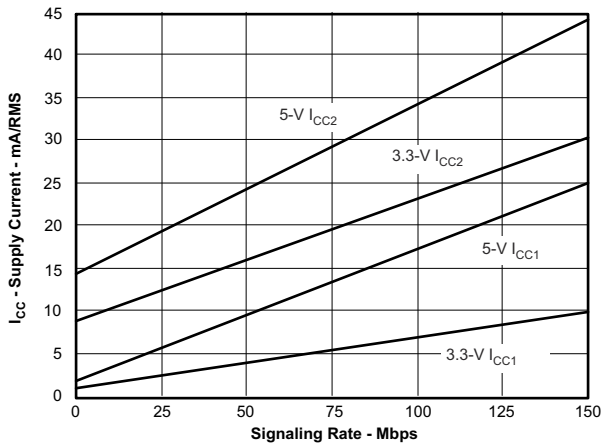


図 5-2. ISO7240C RMS Supply Current vs Signaling Rate

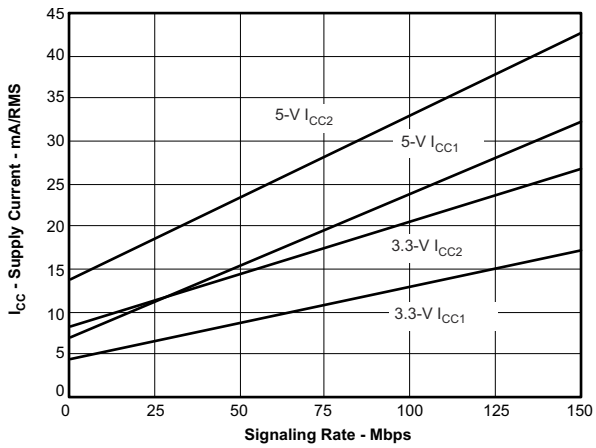


図 5-3. ISO7241C RMS Supply Current vs Signaling Rate

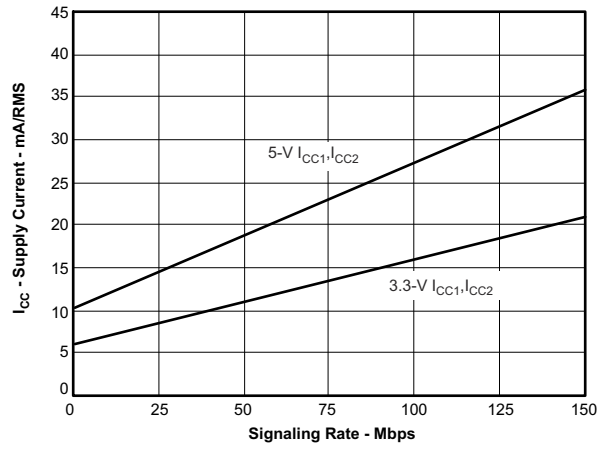


図 5-4. ISO7242C RMS Supply Current vs Signaling Rate

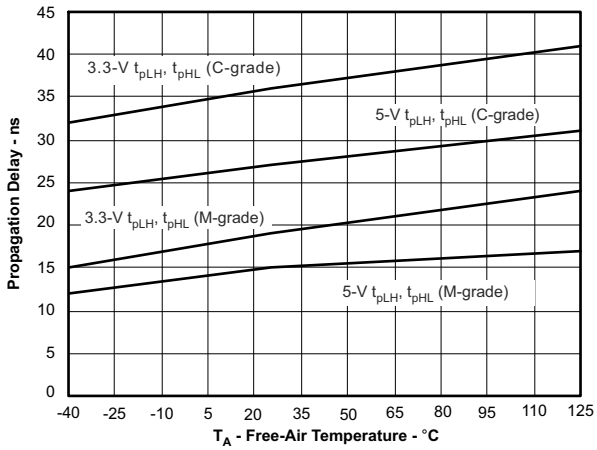


図 5-5. Propogation Delay vs Free-Air Temperature

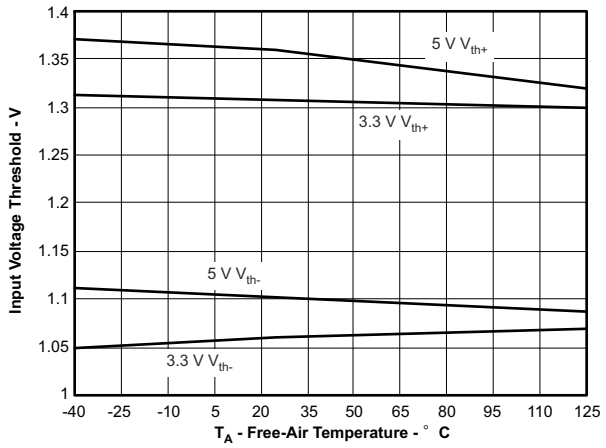


図 5-6. Input Voltage Threshold vs Free-Air Temperature

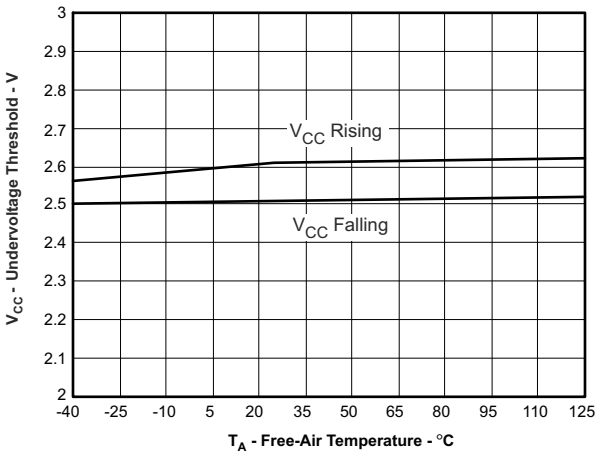


図 5-7. V_{CC1} Failsafe Threshold vs Free-Air Temperature

5.18 Typical Characteristic (continued)

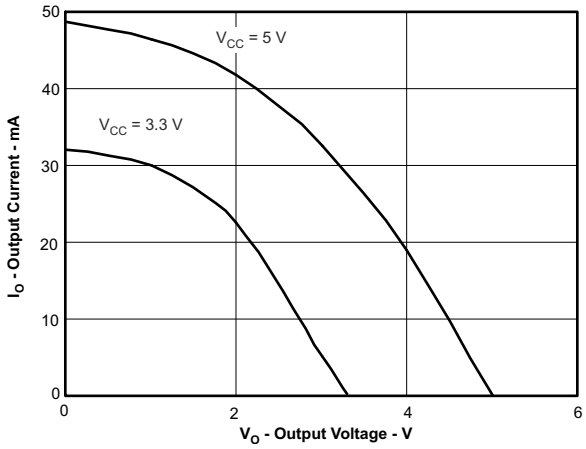


図 5-8. High-Level Output Current vs High-Level Output Voltage

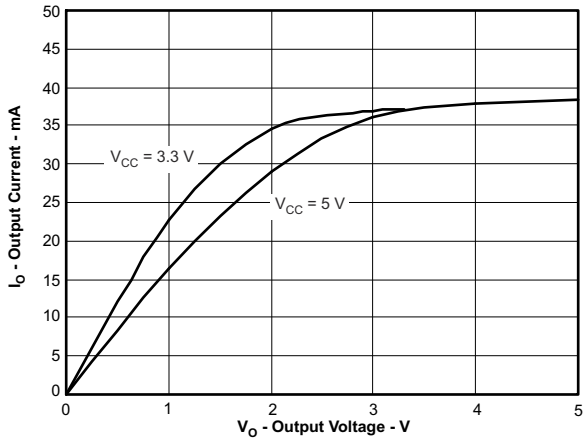
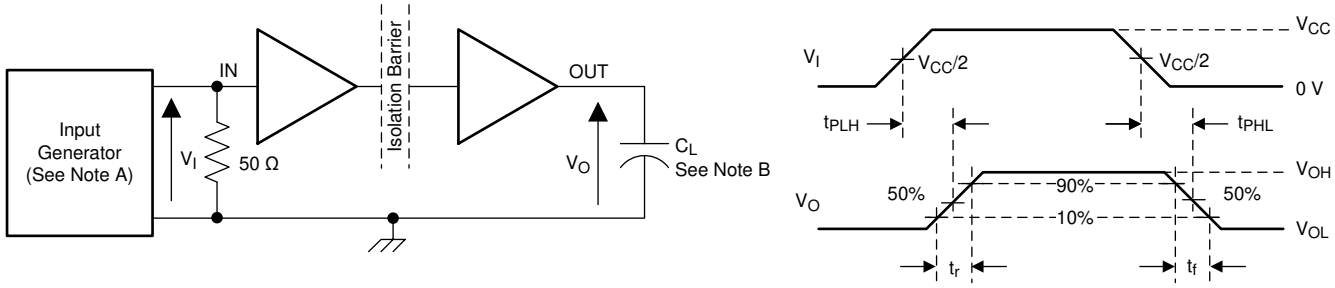


図 5-9. Low-Level Output Current vs Low-Level Output Voltage

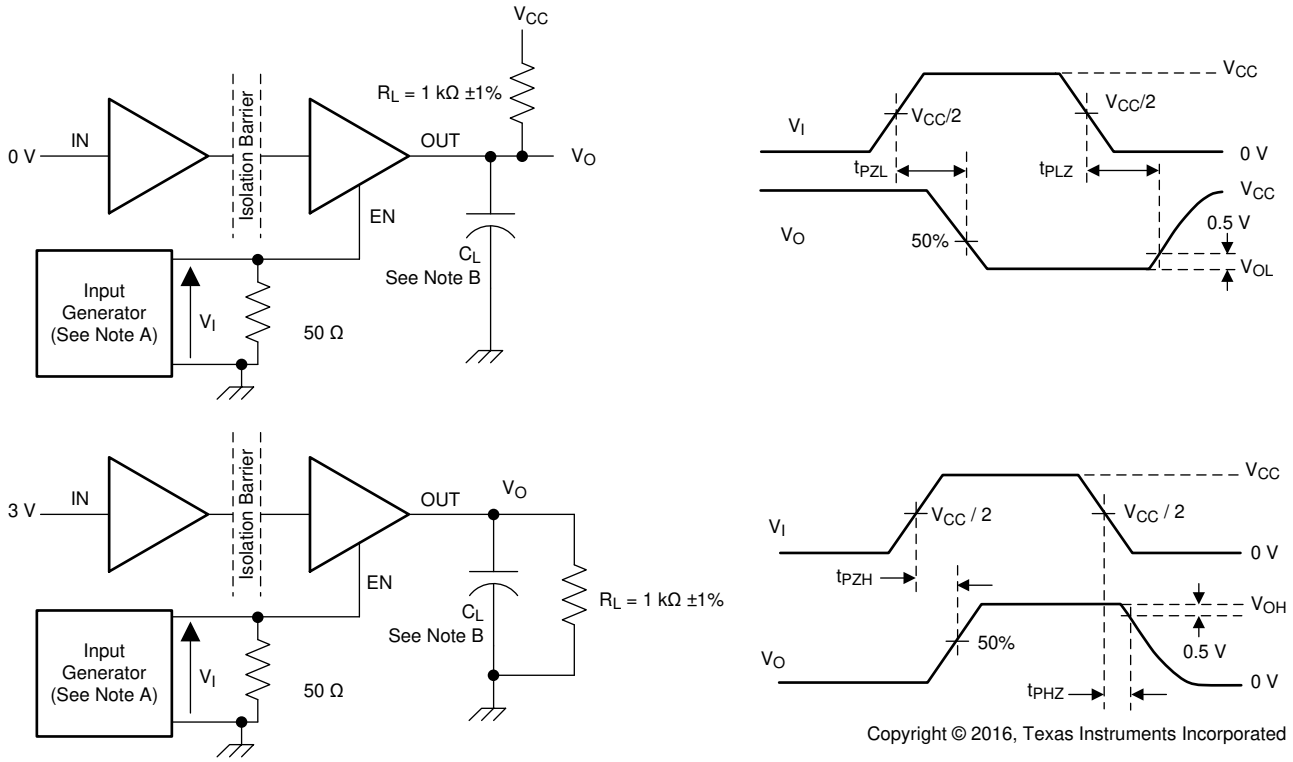
6 Parameter Measurement Information



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

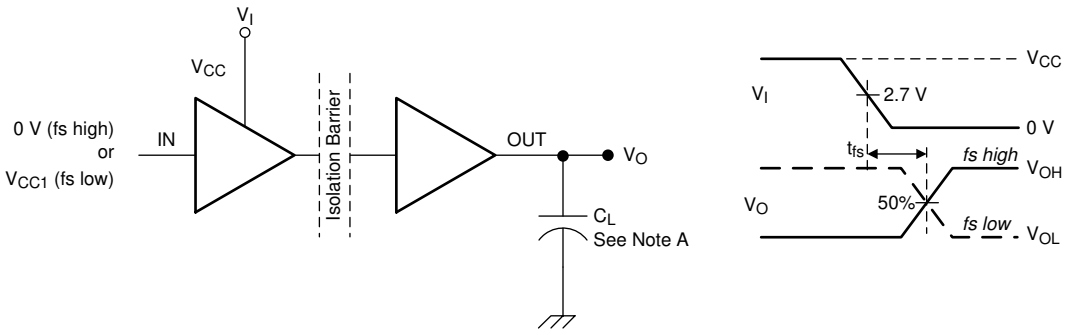
図 6-1. Switching Characteristic Test Circuit and Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

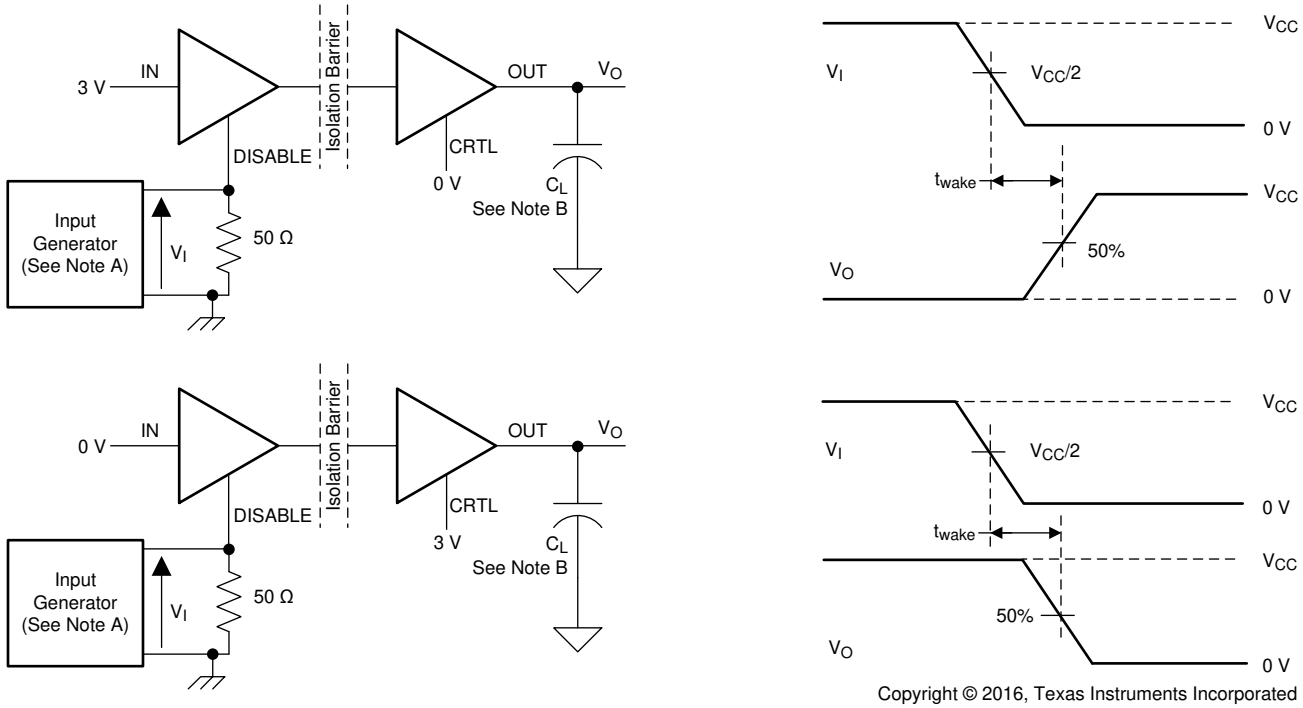
B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 6-2. Enable or Disable Propagation-Delay Time Test Circuit and Waveform



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

図 6-3. Failsafe Delay Time Test Circuit and Voltage Waveforms

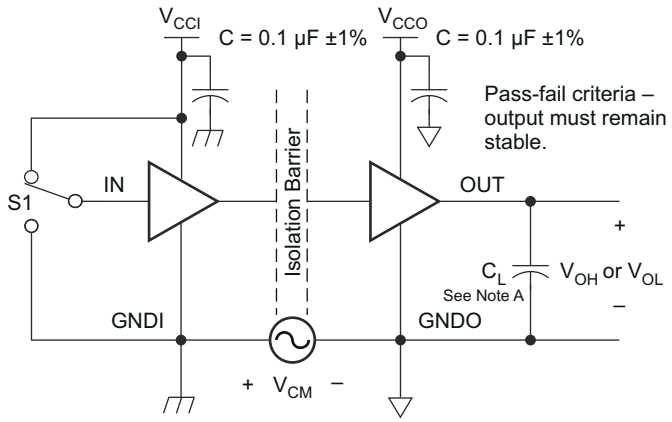


The test that yields the longest time is used in this data sheet.

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

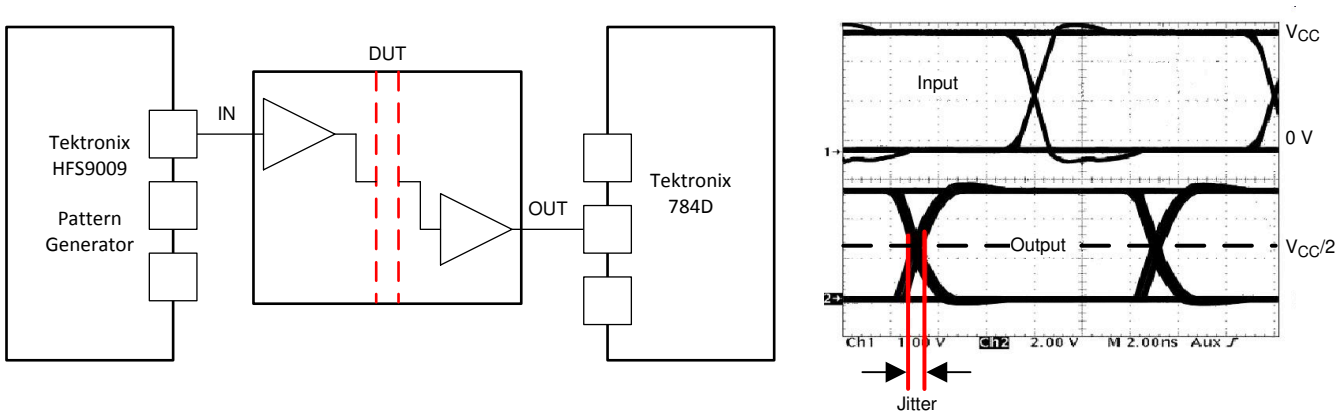
図 6-4. Wake Time From Input Disable Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

図 6-5. Common-Mode Transient Immunity Test Circuit and Voltage Waveform



PRBS bit pattern run length is 2^{16} – 1. Transition time is 800 ps. NRZ data input has no more than five consecutive 1s or 0s.

図 6-6. Peak-to-Peak Eye-Pattern Jitter Test Circuit and Voltage Waveform

7 Detailed Description

7.1 Overview

The ISO724x-Q1 family of devices transmit digital data across a silicon dioxide based isolation barrier. The digital input signal (IN) of the device is sampled by a transmitter and at every data edge the transmitter sends a corresponding differential signal across the isolation barrier. When the input signal is static, the refresh logic periodically sends the necessary differential signal from the transmitter. On the other side of the isolation barrier, the receiver converts the differential signal into a single-ended signal which is output on the OUT pin through a buffer. If the receiver does not receive a data or refresh signal, the timeout logic detects the loss of signal or power from the input side and drives the output to the default level.

7.2 Functional Block Diagram

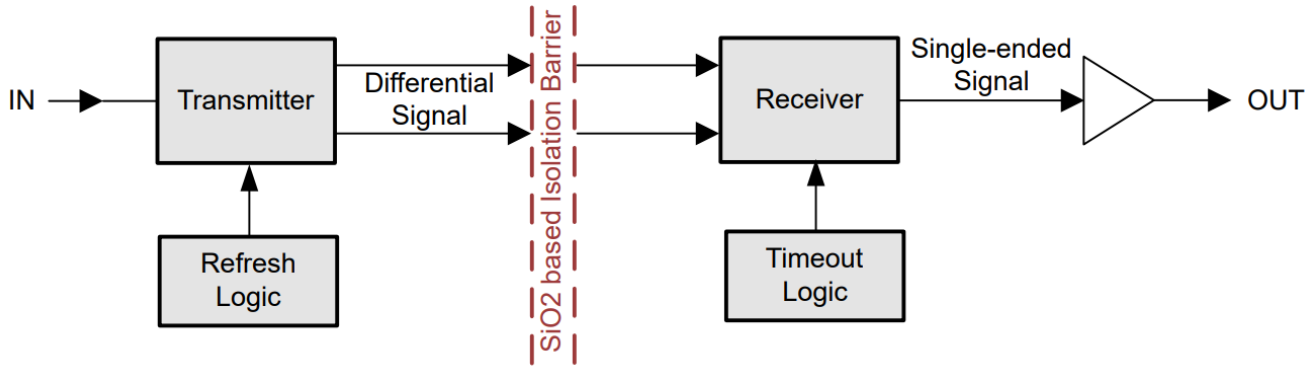


図 7-1. Conceptual Block Diagram of a Digital Isolator

7.3 Feature Description

The ISO724x-Q1 family of devices is available in multiple channel configurations and default output-state options to enable wide variety of application uses. 表 7-1 lists these device features.

表 7-1. Device Features

PRODUCT(1)	SIGNALING RATE	INPUT THRESHOLD	CHANNEL CONFIGURATION
ISO7240CF	25 Mbps	≅1.5 V (TTL)	4/0
ISO7241C	25 Mbps	≅1.5 V (TTL)	3/1
ISO7242C	25 Mbps	≅1.5 V (TTL)	2/2

(1) For the most current package and ordering information, see the *セクション 11* section, or see the TI website at www.ti.com.

7.4 Device Functional Modes

List of ISO724x-Q1 functional modes.

表 7-2. Device Function Table ISO724x-Q1

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (IN)	OUTPUT ENABLE (EN)	OUTPUT (OUT)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	H
PD	PU	X	H or Open	H
PD	PU	X	L	Z
X	PD	X	X	Undetermined

7.4.1 Device I/O Schematics

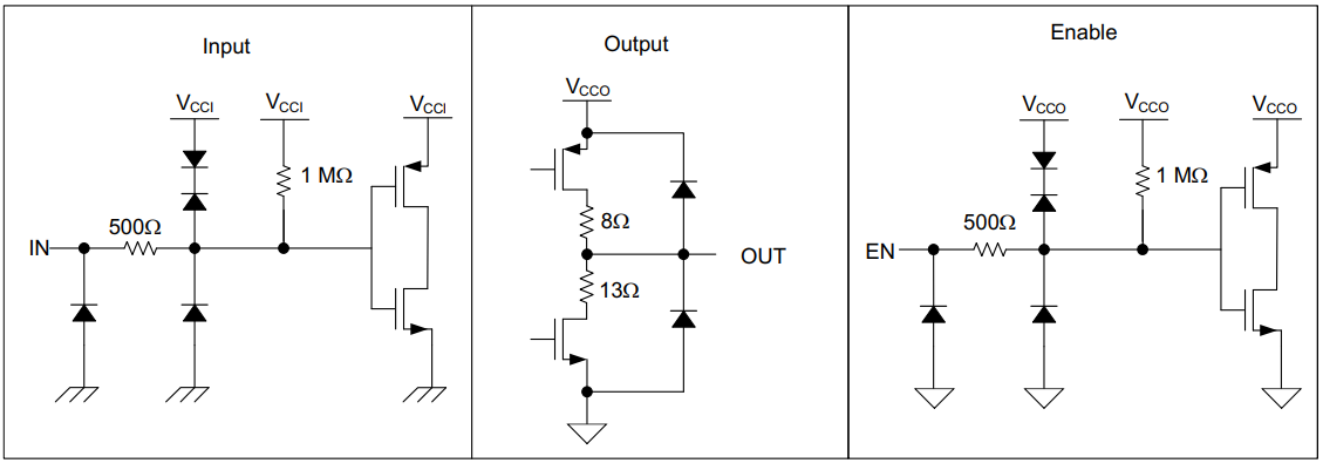


図 7-2. Device I/O Schematics

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ISO724x-Q1 family of devices uses a single-ended TTL or CMOS-logic switching technology. The supply voltage range is from 3.15 V to 5.5 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

8.2 Typical Application

8.2.1 Isolated Data Acquisition System for Process Control

The ISO724x-Q1 family of devices can be used with Texas Instruments' precision analog-to-digital converter and mixed signal microcontroller to create an advanced isolated data acquisition system as shown in 図 8-1.

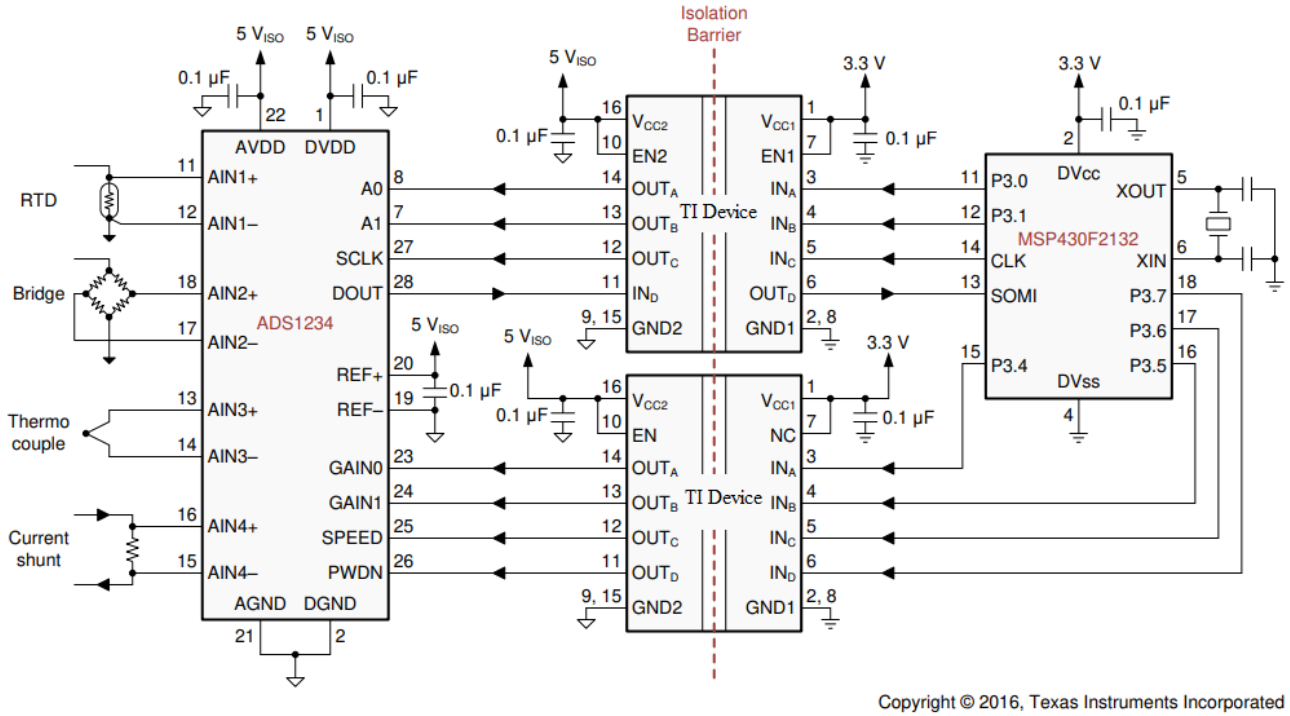


図 8-1. Isolated Data Acquisition System for Process Control

8.2.1.1 Design Requirements

Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO724x-Q1 family of devices only require two external bypass capacitors to operate.

8.2.1.2 Detailed Design Procedure

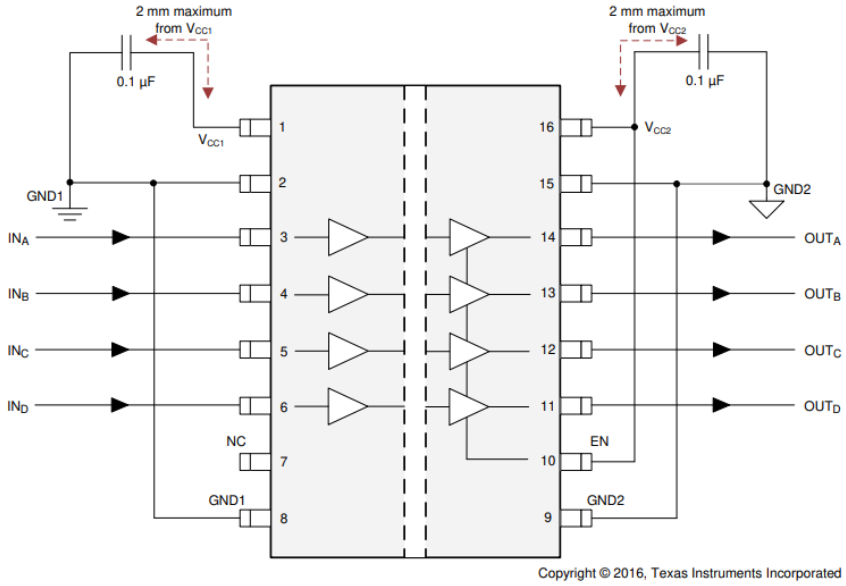


図 8-2. ISO7240x-Q1 Typical Circuit Hook-Up

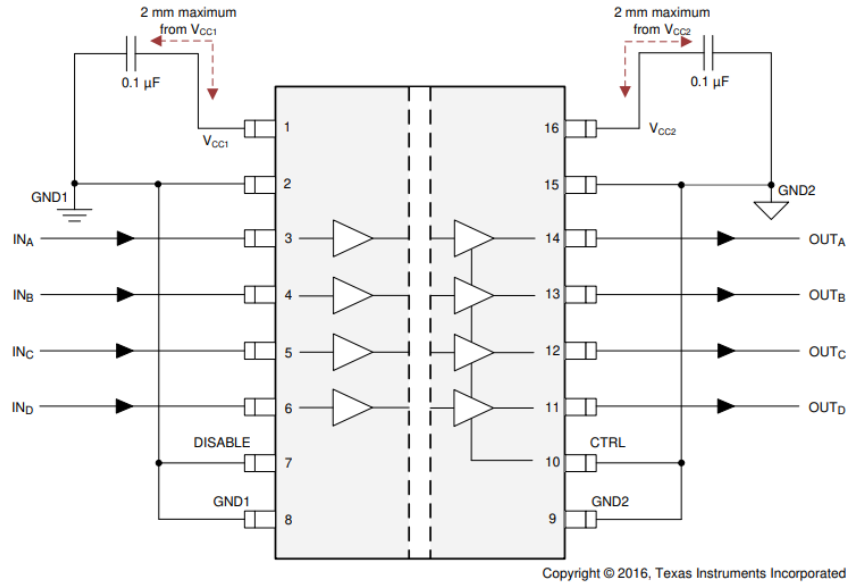


図 8-3. ISO7240CF-Q1 Typical Circuit Hook-Up

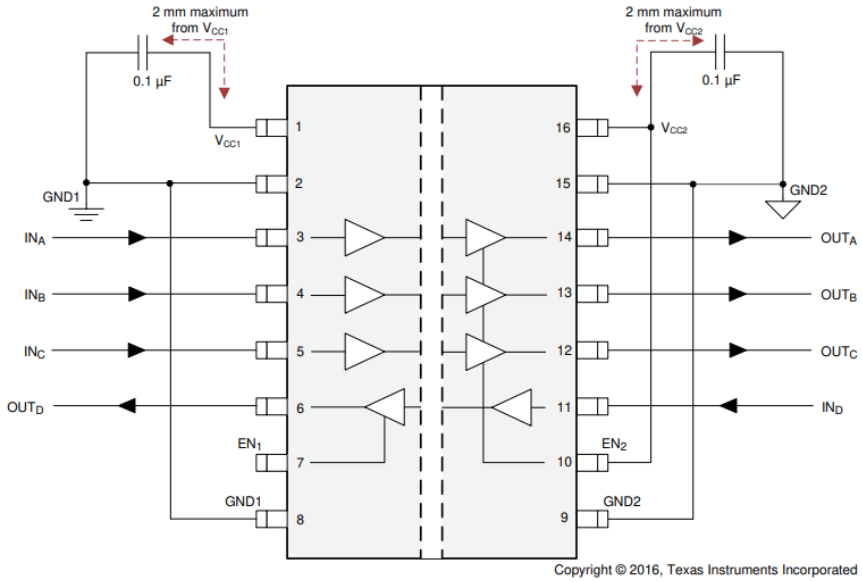


図 8-4. ISO7241x-Q1 Typical Circuit Hook-Up

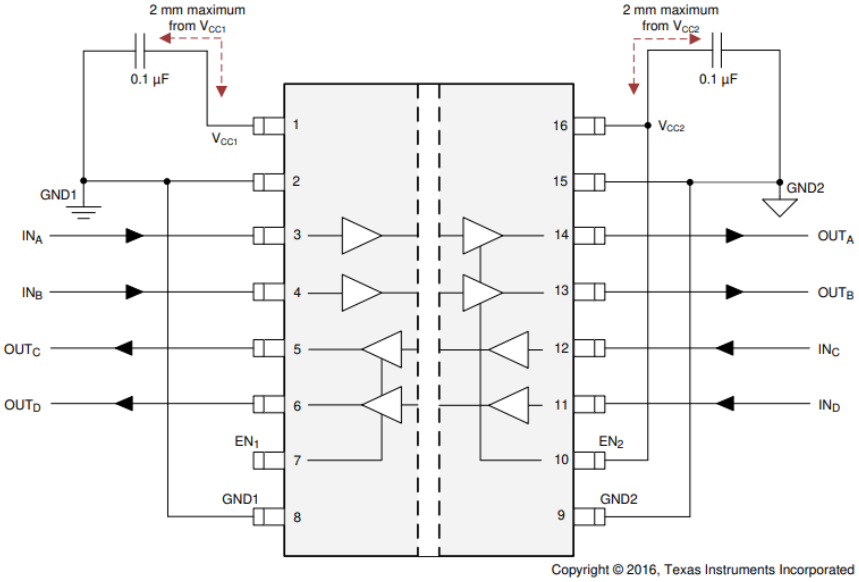


図 8-5. ISO7242x-Q1 Typical Circuit Hook-Up

8.2.2 Isolated SPI for an Analog Input Module with 16 Inputs

The ISO7241x-Q1 family of devices and several other components from Texas Instruments can be used to create an isolated SPI for an input module with 16 inputs.

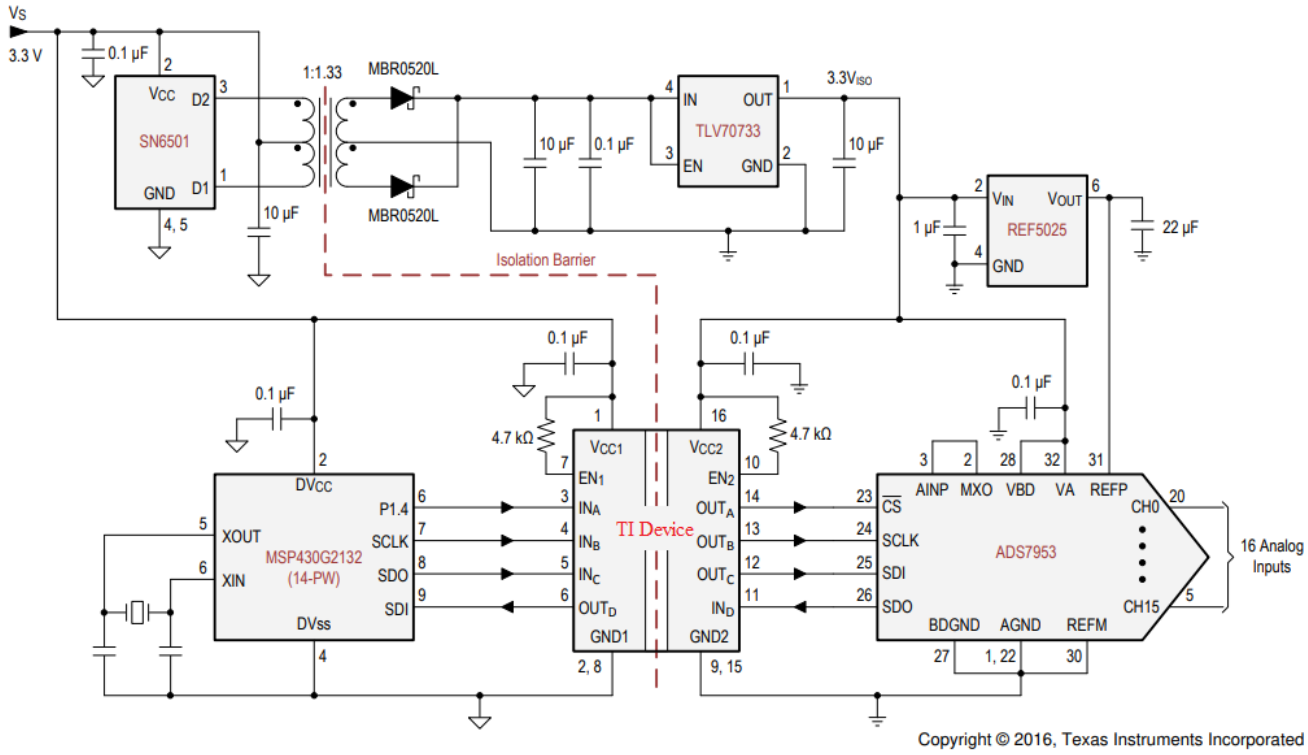


図 8-6. Isolated SPI for an Analog Input Module With 16 Inputs

8.2.2.1 Design Requirements

See the *Design Requirements* in *セクション 8.2.1*.

8.2.2.2 Detailed Design Procedure

See the *Detailed Design Procedure* in *セクション 8.2.1*.

8.2.3 Isolated RS-232 Interface

図 8-7 shows a typical isolated RS-232 interface implementation.

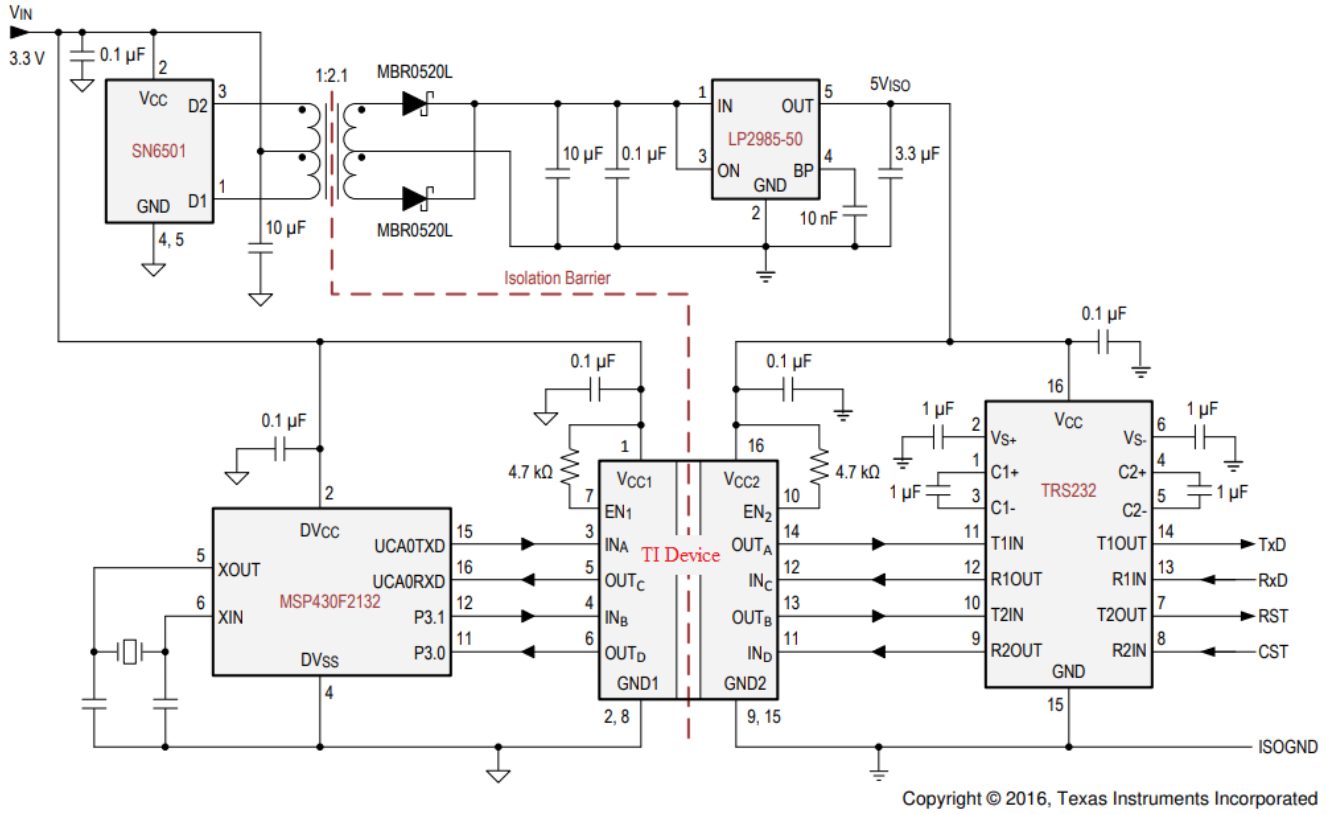


図 8-7. Isolated RS-232 Interface

8.2.3.1 Design Requirements

See the *Design Requirements* in *セクション 8.2.1*.

8.2.3.2 Detailed Design Procedure

See the *Detailed Design Procedure* in *セクション 8.2.1*.

8.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1-µF bypass capacitor is recommended at input and output supply pins (VCC1 and VCC2). The capacitors must be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501 device. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies*.

8.4 Layout

8.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see 図 8-8). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of the inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to *Digital Isolator Design Guide*.

8.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

8.4.2 Layout Example

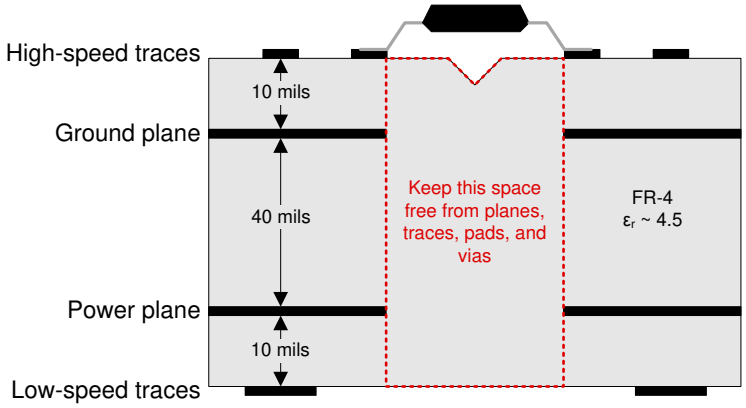


図 8-8. Recommended Layer Stack

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- *Digital Isolator Design Guide*
- *High-Voltage Lifetime of the ISO72x Family of Digital Isolators*
- *ISO72x Digital Isolator Magnetic-Field Immunity*

9.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ISO7240CF	Click here	Click here	Click here	Click here	Click here
ISO7240C	Click here	Click here	Click here	Click here	Click here
ISO7240M	Click here	Click here	Click here	Click here	Click here
ISO7241C	Click here	Click here	Click here	Click here	Click here
ISO7241M	Click here	Click here	Click here	Click here	Click here
ISO7242C	Click here	Click here	Click here	Click here	Click here
ISO7242M	Click here	Click here	Click here	Click here	Click here

9.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.4 サポート・リソース

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9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (September 2011) to Revision B (November 2024) **Page**

- ドキュメント全体を通して容量性絶縁から絶縁バリアに参照を更新 1
- ドキュメント全体で VDE V 0884-11 を DIN VDE 0884-17 に更新 1
- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 1
- Updated Thermal Characteristics, Safety Limiting Values, and Thermal Derating Curves to provide more accurate system-level thermal calculations 5
- Updated electrical and switching characteristics to match device performance 7
- Added the *Detailed Description*, *Overview*, *Feature Description*, *Functional Block Diagram*, and *Device Functional Modes* sections 19
- Added the *Typical Application*, *Power Supply Recommendations*, and *Layout* sections 21

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7240CFQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7240CFQ	Samples
ISO7241CQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7241CQ	Samples
ISO7242CQDWRQ1	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISO7242CQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ISO7240CF-Q1, ISO7241C-Q1, ISO7242C-Q1 :

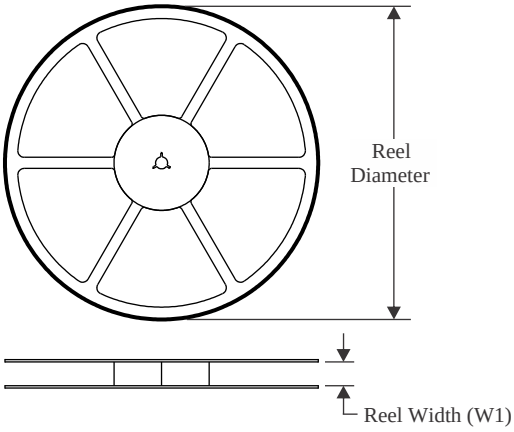
- Catalog : ISO7240CF, ISO7241C, ISO7242C

NOTE: Qualified Version Definitions:

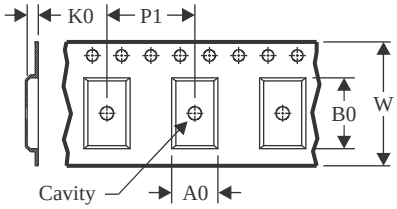
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

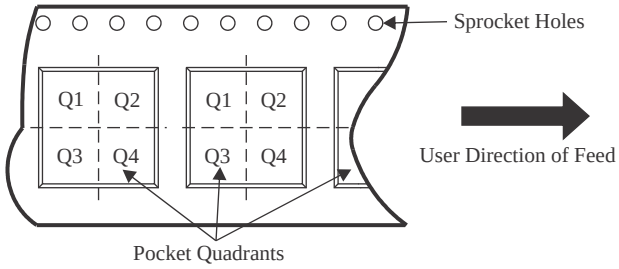


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

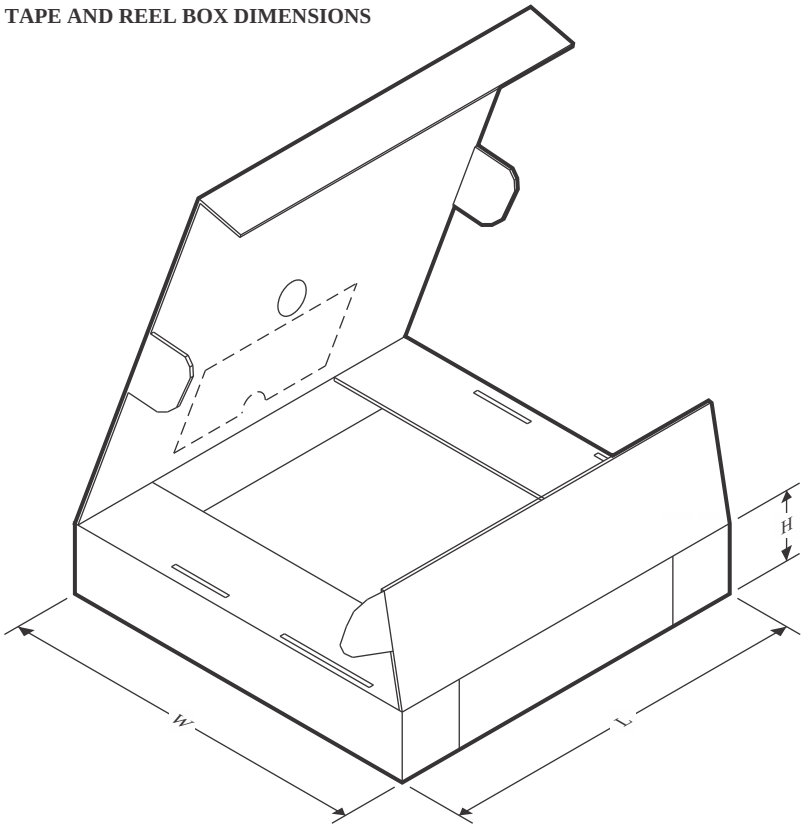
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7240CFQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7241CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7242CQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7240CFQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7241CQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
ISO7242CQDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

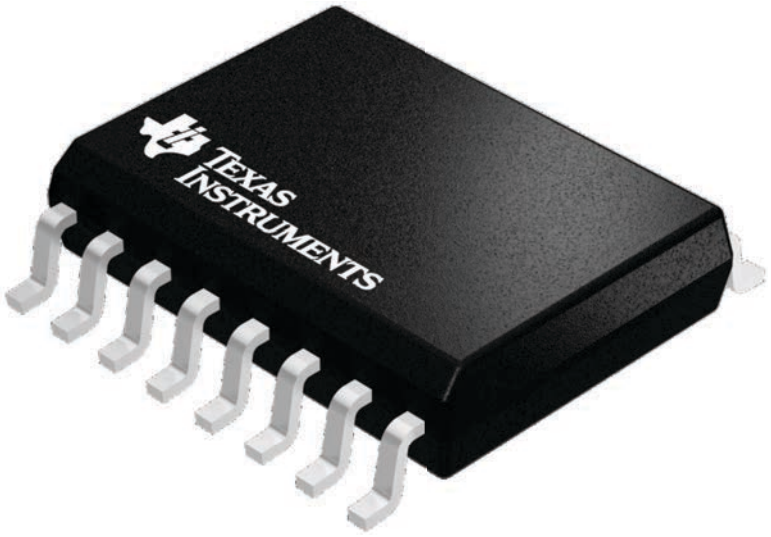
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

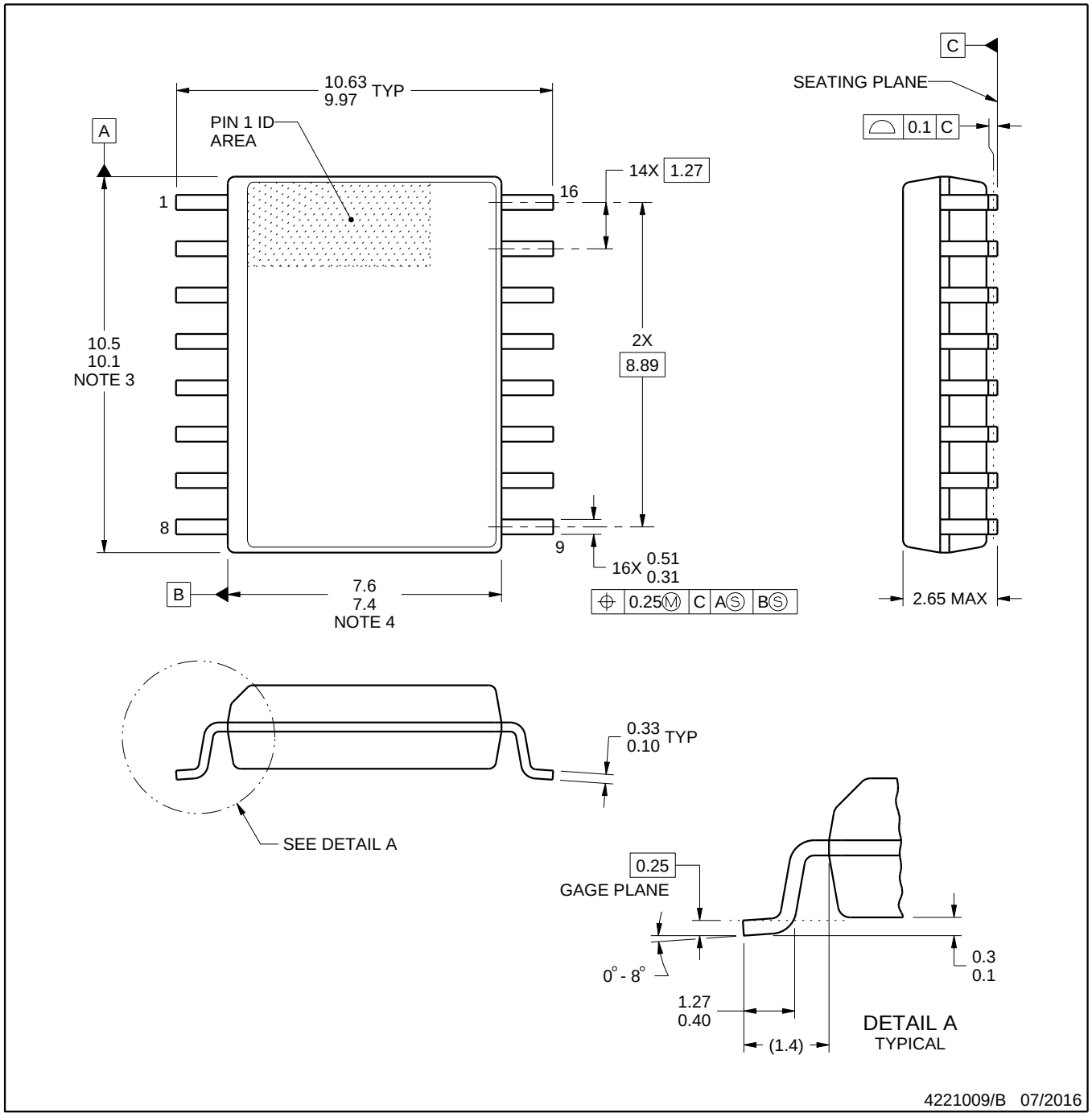
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



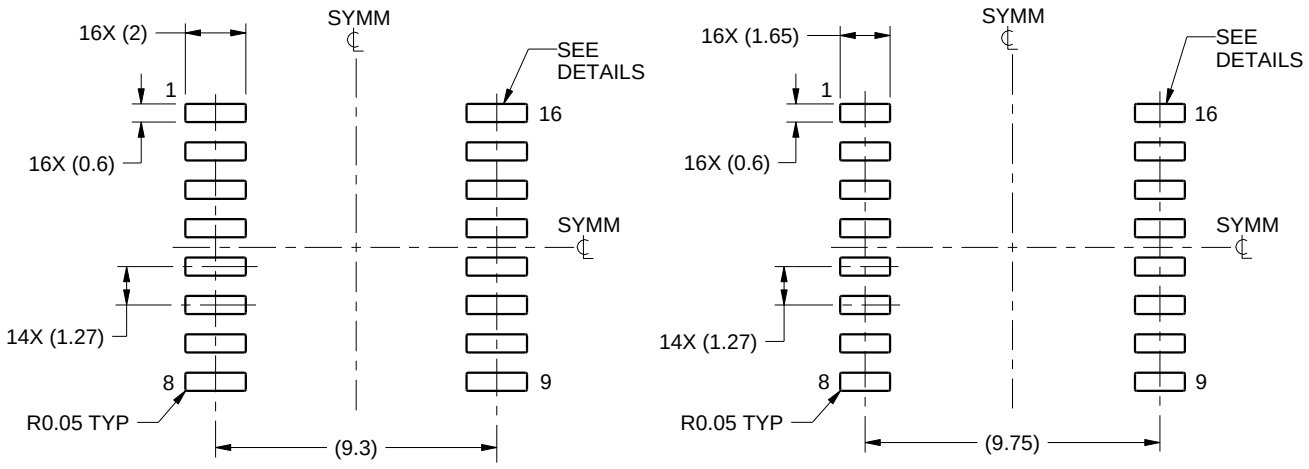
4224780/A

SOIC



NOTES:

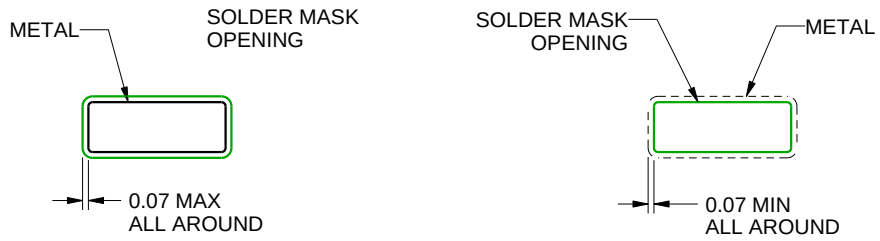
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

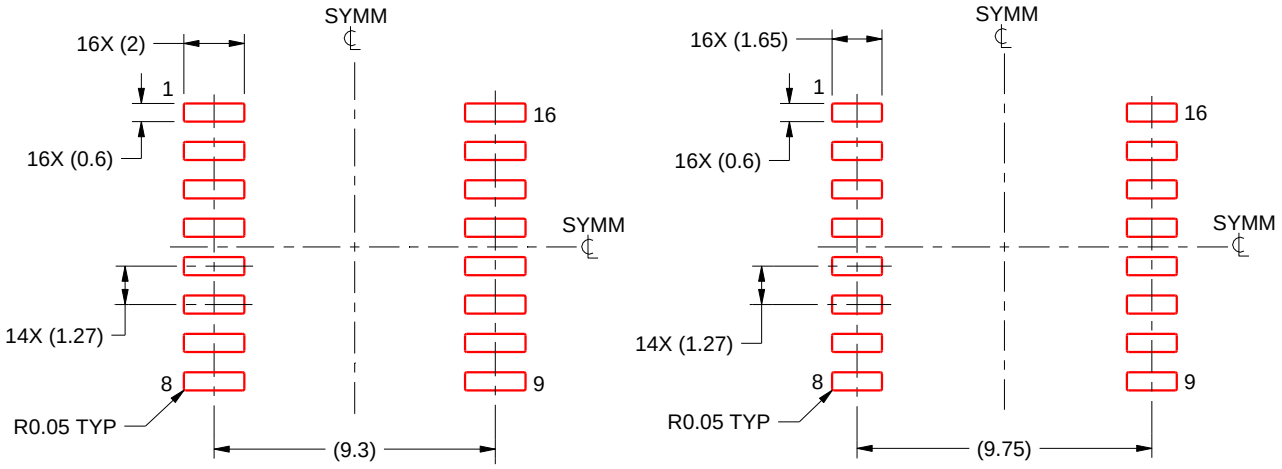
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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