MAX3221E 3V～5.5V シングルチャネル RS-232 ライン ドライバ / レシーバ、±15kV IEC ESD 保護

1 特長

- RS-232 ピンの ESD 保護
  - ±15kV 人体モデル (HBM)
  - ±8kV (IEC 61000-4-2、接触放電)
  - ±15kV (IEC 61000-4-2、エアギャップ放電)
- TIA/EIA-232-F および ITU v.28 規格の要件に適合またはそれを上回る性能
- 3V～5.5V の V_{CC} 電源で動作
- 最大 250kbit/s で動作
- 1 つのドライバと 1 つのレシーバ
- 小さいスタンバイ電流：1µA (代表値)
- 3.3V 電源で 5V ロジック入力を許容
- 自動パワー ダウン機能により、ドライバを自動的にディセーブルすることで電力を節約
- 代替の高速デバイス (1Mbit/s)
  - SN75C3221E、SN65C3221E

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびエンタープライズ・コンピューティング
- バッテリ駆動システム
- PDA
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

3 概要

MAX3221E は、1 つの V_{CC} 電源で動作するシングル ドライバ / シングル レシーバ RS-232 ソリューションです。RS-232 ピンは、IEC 61000-4-2 ESD 保護に対応しています。このデバイスは、TIA/EIA-232-F の要件を満たし、非同期通信コントローラとシリアルポート コネクタの間の電気的インターフェイスとして機能します。チャージ ポンプと 4 つの小さな外付けコンデンサにより、3V～5.5V の単一電源で動作できます。本デバイスは最大 250kbit/s のデータ信号速度、最大 30V/µs のドライバ出力スルーレートで動作します。

パワー マネージメント向けのフレキシブルな制御オプションも利用できます。レシーバの接続が切断された場合、またはリモート ドライバの電源がオフになった場合、自動パワー ダウンにより、ドライバとチャージ ポンプがディセーブルになります。このドライバは、手動でイネーブルまたはディセーブルにすることができます。レシーバ入力が接続されていないか、電源がオフのとき、$\overline{\text{INVALID}}$ 出力が LOW になります。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
MAX3221E	SSOP (DB、16)	6.2mm × 7.8mm
	TSSOP (PW、16)	5mm × 6.4mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

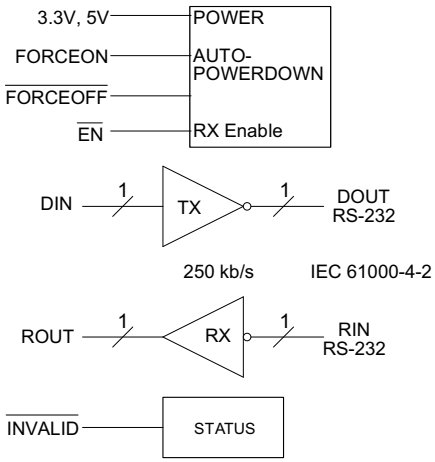

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Table of Contents

1 特長 ... 1
2 アプリケーション ... 1
3 概要 ... 1
4 Pin Configuration and Functions ... 3
5 Specifications ... 4
5.1 Absolute Maximum Ratings ... 4
5.2 ESD Ratings ... 4
5.3 ESD Ratings - IEC Specifications ... 4
5.4 Recommended Operating Conditions ... 5
5.5 Thermal Information ... 5
5.6 Electrical Characteristics ... 5
5.7 Electrical Characteristics: Driver ... 6
5.8 Electrical Characteristics: Receiver ... 6
5.9 Electrical Characteristics: Auto-Power Down ... 6
5.10 Switching Characteristics: Driver ... 7
5.11 Switching Characteristics: Receiver ... 7
5.12 Switching Characteristics: Auto-Power Down ... 7
5.13 代表的特性 ... 8
6 Parameter Measurement Information ... 9
7 Detailed Description ... 12
7.1 Overview ... 12
7.2 Functional Block Diagram ... 12
7.3 Feature Description ... 12
7.4 Device Functional Modes ... 13
8 Application and Implementation ... 14
8.1 Application Information ... 14
8.2 Typical Application ... 14
8.3 Power Supply Recommendations ... 15
8.4 Layout ... 16
9 Device and Documentation Support ... 17
9.1 ドキュメントの更新通知を受け取る方法 ... 17
9.2 サポート・リソース ... 17
9.3 Trademarks ... 17
9.4 静電気放電に関する注意事項 ... 17
9.5 用語集 ... 17
10 Revision History ... 17
11 Mechanical, Packaging, and Orderable Information ... 18

4 Pin Configuration and Functions

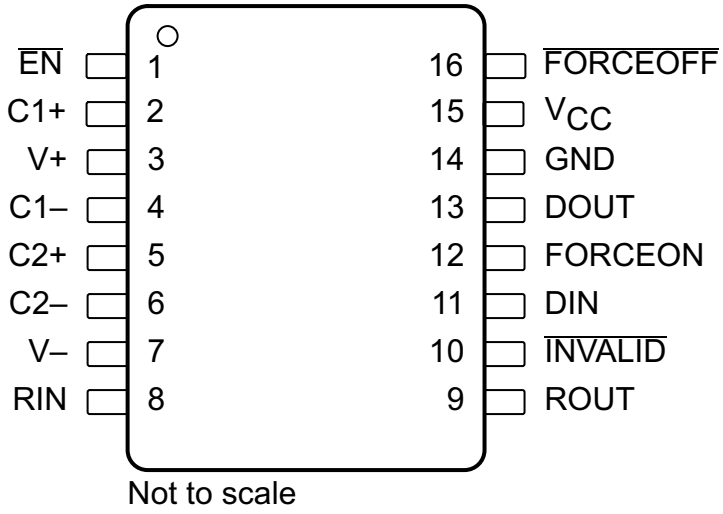


図 4-1. DB or PW Package
16-Pin SSOP or TSSOP
(Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
C1+	2	—	Positive terminals of the voltage-doubler charge pump capacitors
C2+	5		
C1–	4	—	Negative terminals of the voltage-doubler charge pump capacitors
C2–	6		
DIN	11	I	Driver input
DOUT	13	O	RS-232 driver output
$\overline{EN}$	1	I	Low input enables receiver ROUT output. High input sets ROUT to high impedance.
$\overline{FORCEOFF}$	16	I	Automatic power-down control input
FORCEON	12	I	Automatic power-down control input
GND	14	—	Ground
$\overline{INVALID}$	10	O	Invalid output pin. Output low when RIN input is unpowered.
RIN	8	I	RS-232 receiver input
ROUT	9	O	Receiver output
V_{CC}	15	—	3V to 5.5V supply voltage
V+	3	O	5.5V supply generated by the charge pump
V–	7	O	–5.5V supply generated by the charge pump

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.3	6	V
V+	Positive output supply voltage(2)		–0.3	7	V
V–	Negative output supply voltage(2)		0.3	–7	V
V+ – V–	Supply voltage difference(2)			13	V
V_I	Input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON, $\overline{\text{EN}}$	–0.3	6	V
		RIN	–25	25	
V_O	Output voltage	DOUT	–13.2	13.2	V
		ROUT, $\overline{\text{INVALID}}$	–0.3	V_{CC} + 0.3	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltages are with respect to network GND.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 8 and 13	±15000	V
			All other pins	±2000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 ESD Ratings - IEC Specifications

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 Contact Discharge, DOUT and RIN (1)	Pins 8 and 13	±8000	V
		IEC 61000-4-2 Air-Gap Discharge, DOUT and RIN (1)		±15000	

(1) A minimum of 1µF capacitor is required between VCC and GND to meet the specified IEC-ESD level.

5.4 Recommended Operating Conditions

See 図 8-1 (1)

				MIN	NOM	MAX	UNIT
	Supply voltage		V_{CC} = 3.3V	3	3.3	3.6	V
			V_{CC} = 5V	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$	V_{CC} = 3.3V	2			V
			V_{CC} = 5V	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, $\overline{FORCEOFF}$, FORCEON, $\overline{EN}$				0.8	V
V_I	Driver and control input voltage	DIN, $\overline{FORCEOFF}$, FORCEON		0		5.5	V
V_I	Receiver input voltage			–25		25	V
T_A	Operating free-air temperature	MAX3221EC		0		70	°C
		MAX3221EI		–40		85	

(1) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ± 0.5V.

5.5 Thermal Information

THERMAL METRIC(1)		MAX3221E		UNIT
		DB (SSOP)	PW (TSSOP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	105.8	110.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	41.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.6	57.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	14.1	4.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.8	56.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_I	Input leakage current	$\overline{FORCEOFF}$, FORCEON, $\overline{EN}$				±0.01	±1	µA
I_{CC}	Supply current	Auto-power down disabled	V_{CC} = 3.3V or 5V, T_A = 25°C	No load, $\overline{FORCEOFF}$ and FORCEON at V_{CC}		0.3	1	mA
		Powered off		No load, $\overline{FORCEOFF}$ at GND		1	10	µA
		Auto-power down enabled		No load, $\overline{FORCEOFF}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ± 0.5V.

5.7 Electrical Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	DOUT at R_L = 3kΩ to GND,	DIN = GND		5	5.4		V
V_{OL}	Low-level output voltage	DOUT at R_L = 3kΩ to GND,	DIN = V_{CC}		–5	–5.4		V
I_{IH}	High-level input current	V_I = V_{CC}				±0.01	±1	μA
I_{IL}	Low-level input current	V_I = GND				±0.01	±1	μA
I_{OS}	Short-circuit output current(2)	V_{CC} = 3.6V,	V_O = 0V			±35	±60	mA
		V_{CC} = 5.5V,	V_O = 0V			±35	±60	
r_o	Output resistance	V_{CC}, V+, and V– = 0V,	V_O = ±2V		300	10M		Ω
I_{off}	Output leakage current	$\overline{FORCEOFF}$ = GND	V_O = ±12V,	V_{CC} = 3V to 3.6V			±25	μA
			V_O = ±10V,	V_{CC} = 4.5V to 5.5V			±25	

(1) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power-dissipation ratings, and not more than one output should be shorted at a time.
(3) Test conditions are C1–C4 = 0.1μF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047μF, C2–C4 = 0.33μF at V_{CC} = 5V ± 0.5V.

5.8 Electrical Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1mA	V_{CC} – 0.6	V_{CC} – 0.1		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3V		1.6	2.4	V
		V_{CC} = 5V		1.9	2.4	
$V_{IT–}$	Negative-going input threshold voltage	V_{CC} = 3.3V	0.6	1.1		V
		V_{CC} = 5V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} – $V_{IT–}$)			0.5		V
I_{off}	Output leakage current	$\overline{EN}$ = V_{CC}		±0.05	±10	μA
r_i	Input resistance	V_I = ±3V to ±25V	3	5	7	kΩ

(1) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
(2) Test conditions are C1–C4 = 0.1μF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047μF, C2–C4 = 0.33μF at V_{CC} = 5V ± 0.5V.

5.9 Electrical Characteristics: Auto-Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{T–(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for I $\overline{NVALID}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	–0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	I_{OH} = –1mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} – 0.6		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	I_{OL} = 1.6mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		0.4	V

5.10 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
	Maximum data rate	C_L = 1000pF,	R_L = 3kΩ,	150	250		kbit/s
$t_{sk(p)}$	Pulse skew(2)	C_L = 150pF to 2500pF,	R_L = 3kΩ to 7kΩ, See 図 6-2		100		ns
SR(tr)	Slew rate, transition region (see 図 6-1)	V_{CC} = 3.3V, R_L = 3kΩ to 7kΩ	C_L = 150pF to 1000pF	6		30	V/µs
			C_L = 150pF to 2500pF	4		30	

(1) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ± 0.5V.

5.11 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(3)

PARAMETER		TEST CONDITIONS	TYP(1)	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150pF, See 図 6-3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output	C_L = 150pF, See 図 6-3	150	ns
t_{en}	Output enable time	C_L = 150pF, R_L = 3kΩ, See 図 6-4	200	ns
t_{dis}	Output disable time	C_L = 150pF, R_L = 3kΩ, See 図 6-4	200	ns
$t_{sk(p)}$	Pulse skew(2)	See 図 6-3	50	ns

(1) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.
(2) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
(3) Test conditions are C1–C4 = 0.1µF at V_{CC} = 3.3V ± 0.3V; C1 = 0.047µF, C2–C4 = 0.33µF at V_{CC} = 5V ± 0.5V.

5.12 Switching Characteristics: Auto-Power Down

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TYP(1)	UNIT
t_{valid}	Propagation delay time, low- to high-level output	1	µs
$t_{invalid}$	Propagation delay time, high- to low-level output	30	µs
t_{en}	Supply enable time	100	µs

(1) All typical values are at V_{CC} = 3.3V or V_{CC} = 5V, and T_A = 25°C.

5.13 代表的特性

T_A = 25℃、V_{CC} = 3.3V

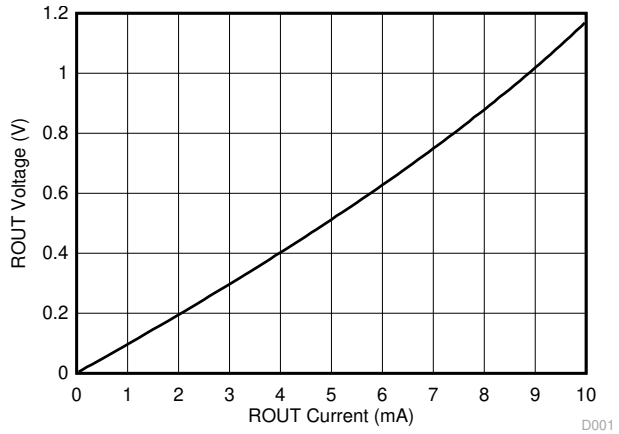


図 5-1. レシーバ VOL と負荷電流との関係

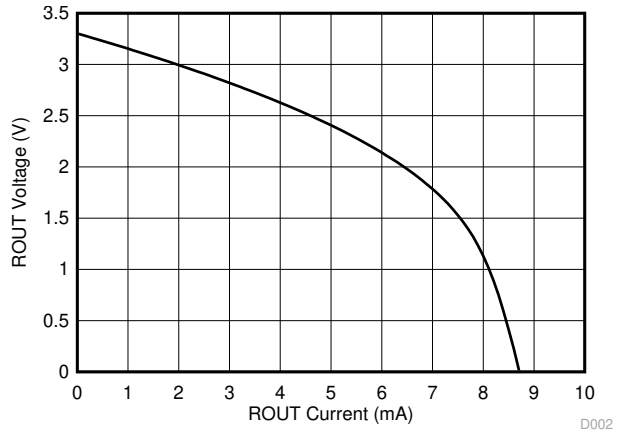


図 5-2. レシーバ VOH と負荷電流との関係

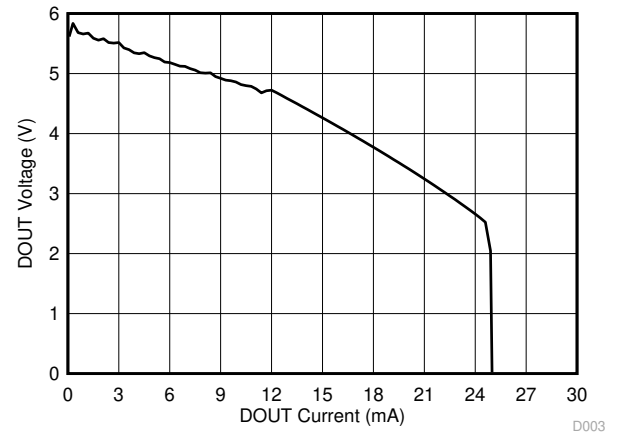


図 5-3. ドライバ VOH と負荷電流との関係

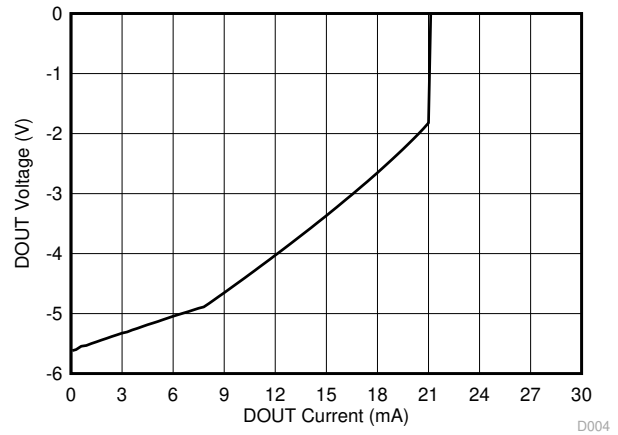
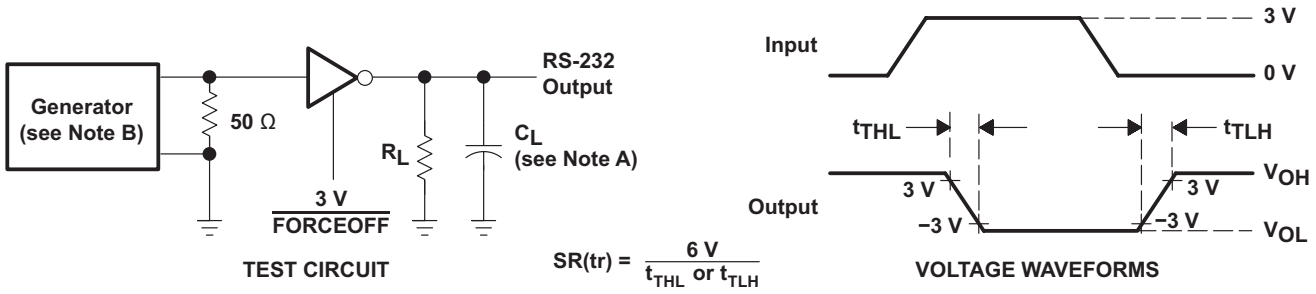


図 5-4. ドライバ VOL と負荷電流との関係

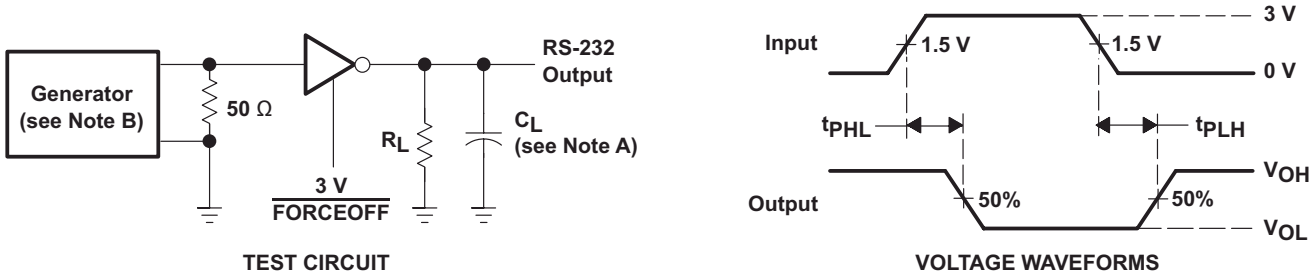
6 Parameter Measurement Information



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250kbps, Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

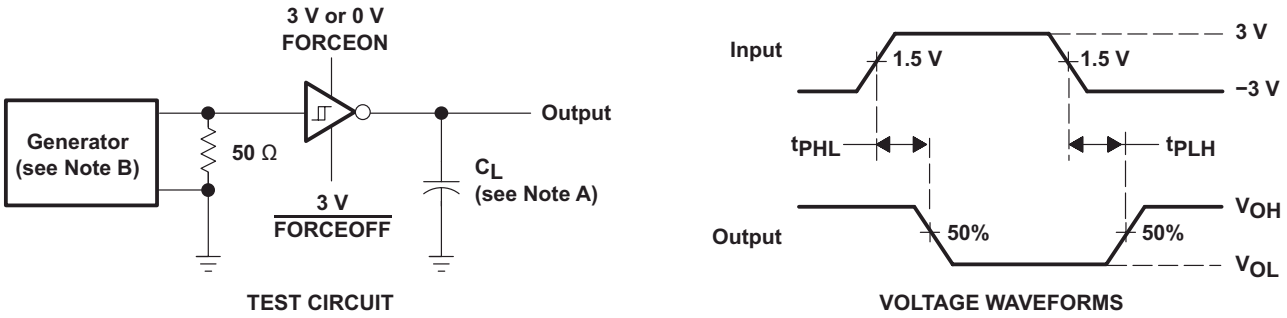
図 6-1. Driver Slew Rate



A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250kbps, Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

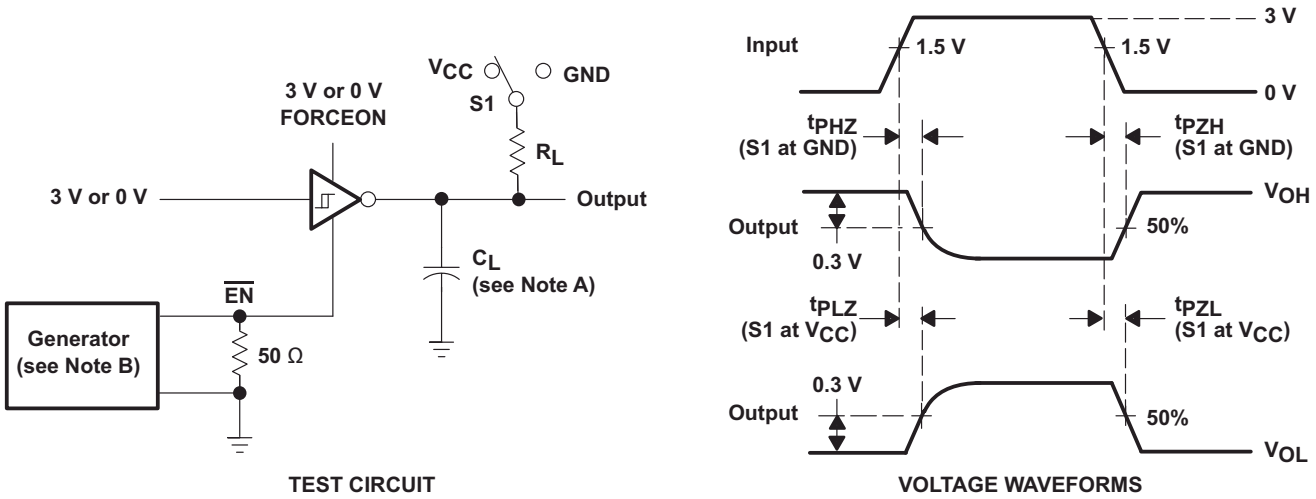
図 6-2. Driver Pulse Skew



A. C_L includes probe and jig capacitance.

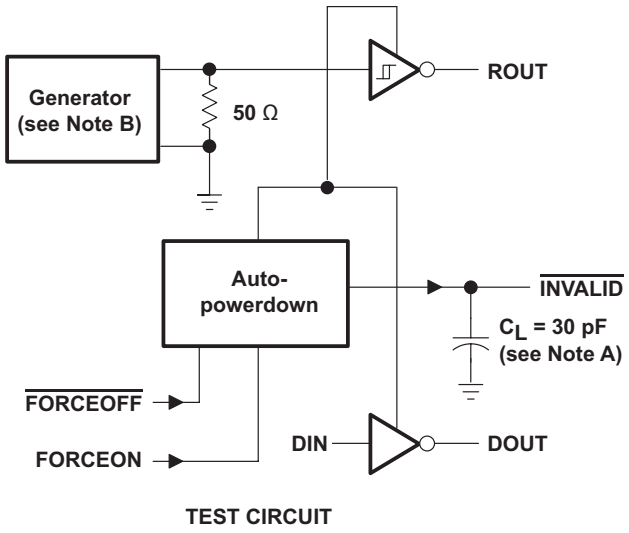
B. The pulse generator has the following characteristics: Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.

図 6-3. Receiver Propagation Delay Times

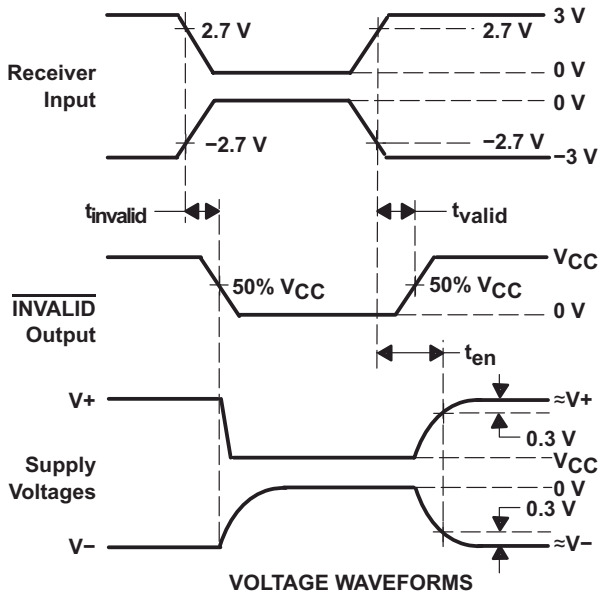


A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50Ω, 50% duty cycle, t_r ≤ 10ns, t_f ≤ 10ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

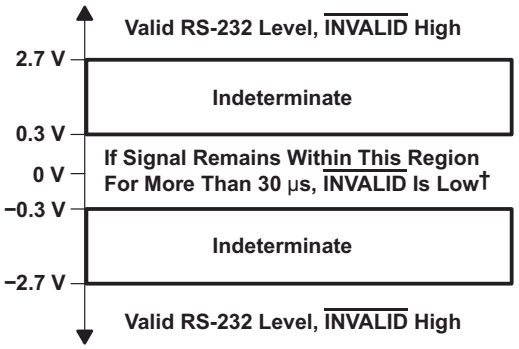
図 6-4. Receiver Enable and Disable Times



TEST CIRCUIT



VOLTAGE WAVEFORMS



† Auto-powerdown disables drivers and reduces supply current to 1 µA.

図 6-5. INVALID Propagation Delay Times and Driver Enabling Time

7 Detailed Description

7.1 Overview

The MAX3221E is a single driver, single receiver RS-232 solution operating from a single V_{CC} supply. The RS-232 pins provide IEC 61000-4-2 ESD protection. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3V to 5.5V supply. These devices operate at data signaling rates up to 250kbit/s and a maximum of 30V/µs driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The auto-power-down feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If $\overline{\text{FORCEOFF}}$ is set low and $\overline{\text{EN}}$ is high, both the driver and receiver are shut off, and the supply current is reduced to 1 µA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-power-down condition to occur. Auto-power down can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high. With auto-power down enabled, the device is activated automatically when a valid signal is applied to the receiver input. The $\overline{\text{INVALID}}$ output notifies the user if an RS-232 signal is present at the receiver input. $\overline{\text{INVALID}}$ is high (valid data) if the receiver input voltage is greater than 2.7V or less than –2.7V, or has been between –0.3V and 0.3V for less than 30µs. $\overline{\text{INVALID}}$ is low (invalid data) if the receiver input voltage is between –0.3V and 0.3V for more than 30µs. See 図 6-1 for receiver input levels.

7.2 Functional Block Diagram

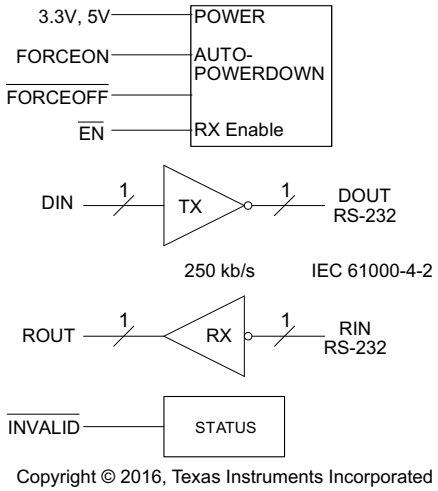


図 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

7.3.1 Power

The power block increases, inverts, and regulates voltage at V+ and V- pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by FORCEON and $\overline{\text{FORCEOFF}}$ inputs. Receiver is controlled by $\overline{\text{EN}}$ input. When unpowered, the MAX3221E can be safely connected to an active remote RS-232 device.

7.3.2 RS-232 Driver

One driver interfaces standard logic levels to RS-232 levels. DIN input must be valid high or low.

7.3.3 RS-232 Receiver

One receiver interfaces RS-232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS-232 load. A logic high input on the $\overline{EN}$ pin shuts down the receiver output.

7.3.4 RS-232 Status

The $\overline{INVALID}$ output goes low when RIN input is unpowered for more than 30µs. The $\overline{INVALID}$ output goes high when receiver has a valid input. The $\overline{INVALID}$ output is active when V_{CC} is powered irregardless of FORCEON and $\overline{FORCEOFF}$ inputs (see 表 7-3).

7.4 Device Functional Modes

表 7-1, 表 7-2, and 表 7-3 show the behavior of the driver, receiver, and $\overline{INVALID}$ features under all possible relevant combinations of inputs.

表 7-1. Function Tables Each Driver (1)

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{FORCEOFF}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-power down disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-power down enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-power down feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

表 7-2. Each Receiver (1)

INPUTS			OUTPUT ROUT
RIN	$\overline{EN}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

表 7-3. $\overline{INVALID}$ (1)

INPUTS				OUTPUT
RIN	FORCEON	$\overline{FORCEOFF}$	$\overline{EN}$	$\overline{INVALID}$
L	X	X	X	H
H	X	X	X	H
Open	X	X	X	L

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

8 Application and Implementation

注

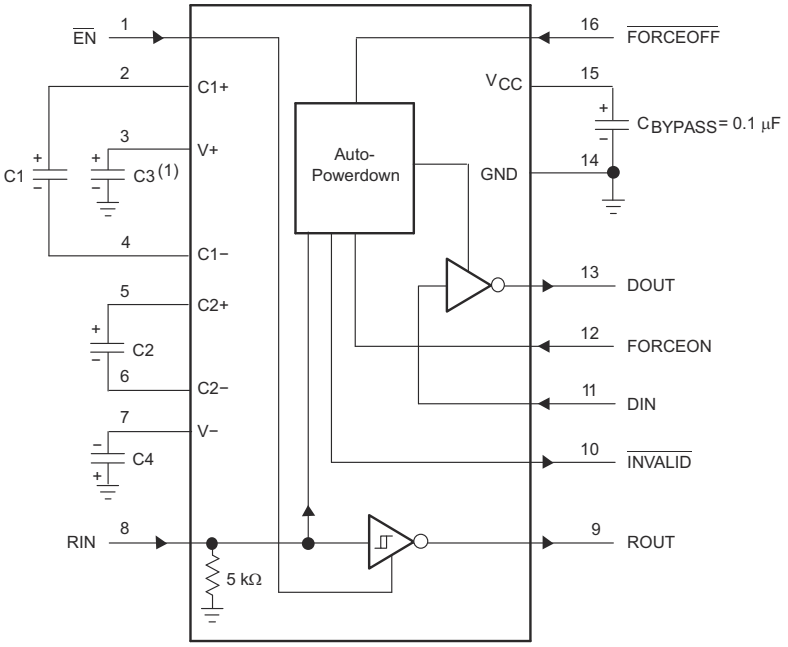
以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The MAX3221E line driver and receiver is a specialized device for 3V to 5.5V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in 図 8-1.

8.2 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or V_{CC}. $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS-232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.



(1) C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

図 8-1. Typical Operating Circuit and Capacitor Values

8.2.1 Design Requirements

- Recommended V_{CC} is 3.3V or 5V.
  - 3V to 5.5V is also possible
- Maximum recommended bit rate is 250kbps.
- Use capacitors as shown in 図 8-1.

8.2.2 Detailed Design Procedure

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels.
- Select capacitor values based on VCC level for best performance.

8.2.3 Application Curves

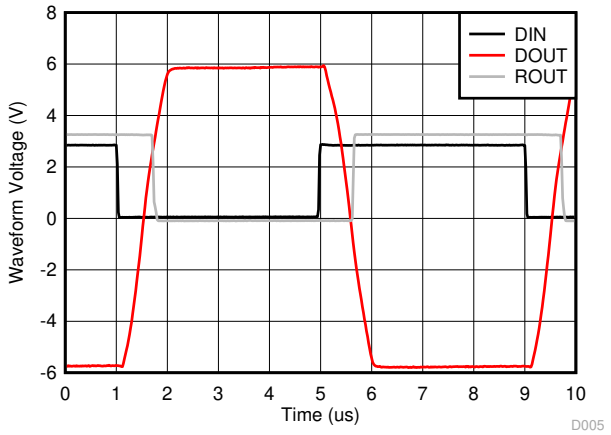


図 8-2. Loopback Waveforms V_{CC} = 3.3V, Data Rate 250kbit/s

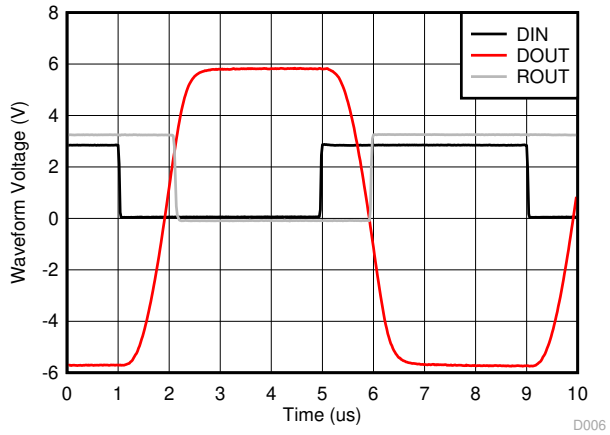


図 8-3. Loopback Waveforms with 1nF load V_{CC} = 3.3V, Data Rate 250kbit/s

8.3 Power Supply Recommendations

TI recommends a 0.1µF capacitor to filter noise on the power supply pin. For additional filter capability, a 0.01µF capacitor may be added in parallel as well. Power supply input voltage is recommended to be any valid level in *セクション 5.4* .

8.4 Layout

8.4.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times. Make the impedance from MAX3221E ground pin and the circuit board ground plane as low as possible for best ESD performance. Use wide metal and multiple vias on both sides of ground pin.

8.4.2 Layout Example

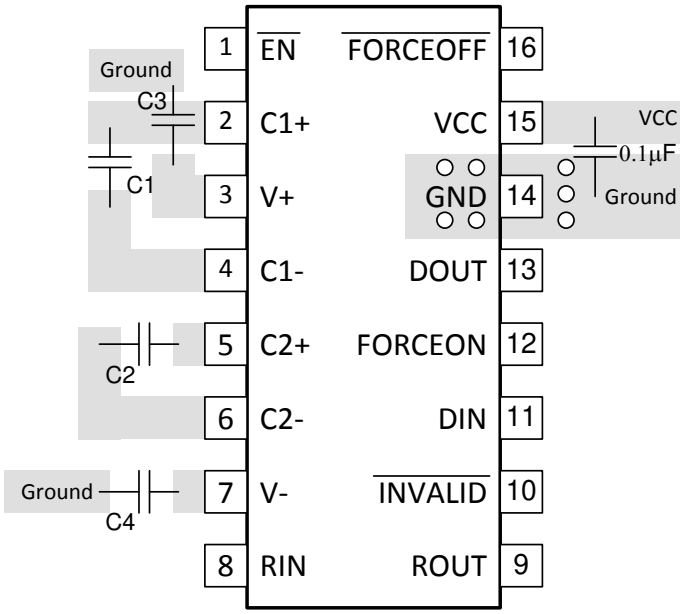


図 8-4. MAX3221E Layout Example

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (July 2021) to Revision D (July 2024) — **Page**

- 「製品情報」表を「パッケージ情報」表に変更 1
- Changed Pins 8 and 11 to Pins 8 and 13 in the *ESD Ratings* 4
- Changed Pins 8 and 11 to Pins 8 and 13 in the *ESD ratings IEC Specifications* 4

Changes from Revision B (March 2016) to Revision C (July 2021) — **Page**

- *「アプリケーション」*の一覧を変更 1
- Added *ESD ratings IEC Specifications* table and added a table note for the minimum requirement to meet the IEC ESD level 4
- Changed values in the *Thermal Information* table for DB and PW packages 5

Changes from Revision A (May 2006) to Revision B (March 2016) — **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 1
- *「注文情報」*表を削除 (このデータシートの末尾にある「製品オプションについての付録」を参照) 1

- Changed $R_{\theta JA}$ thermal values: 82 to 92 for DB package and 108 to 100.3 for PW Package..... 5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3221ECDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	Samples
MAX3221ECDBRG4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	Samples
MAX3221ECPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP221EC	Samples
MAX3221EIDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	Samples
MAX3221EIDBRG4	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	Samples
MAX3221EIPW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	MP221EI	
MAX3221EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	Samples
MAX3221EIPWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP221EI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

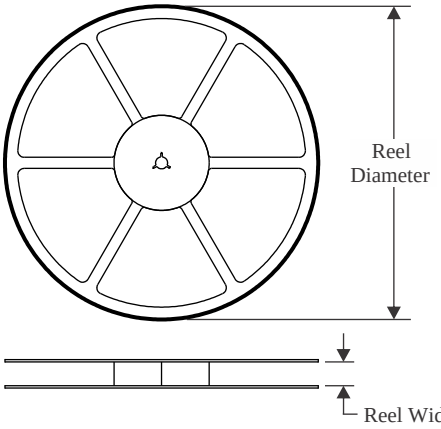
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

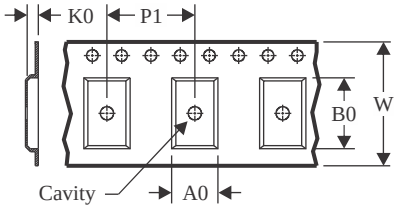
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

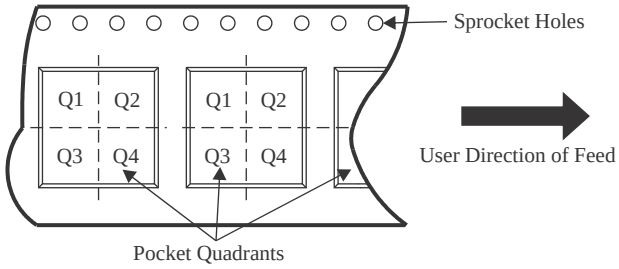


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

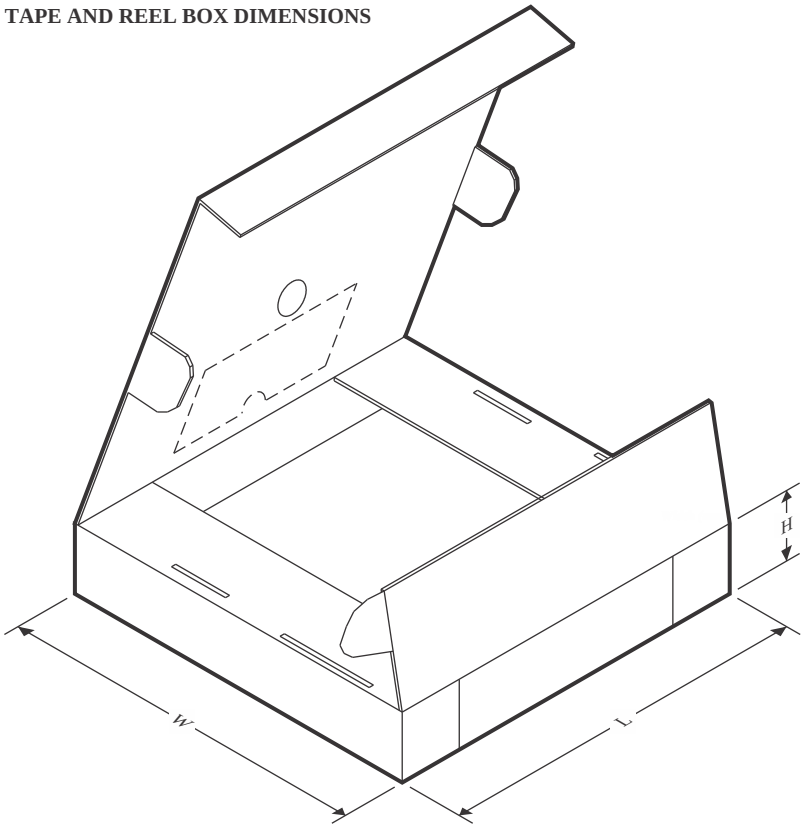
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
MAX3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MAX3221EIPWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

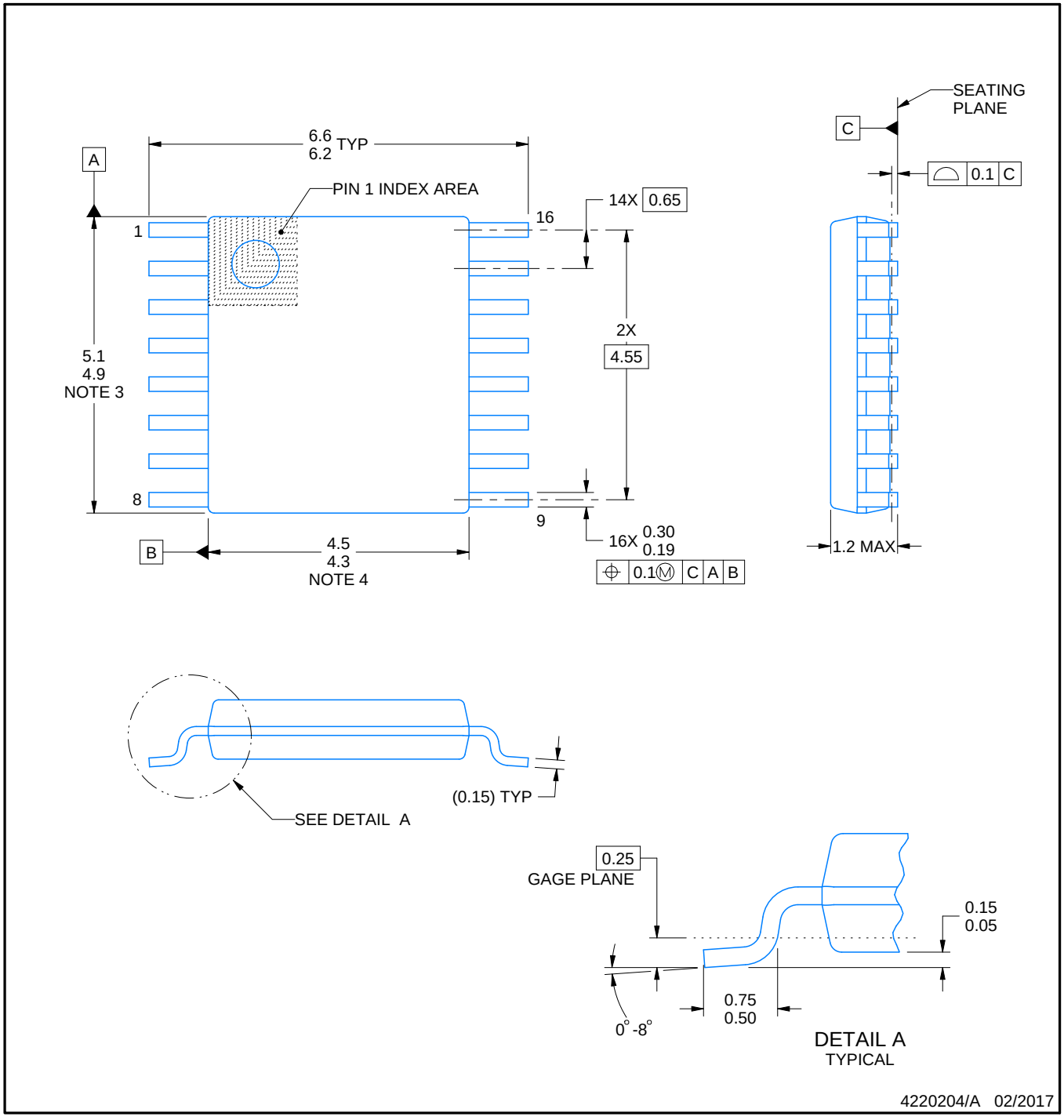
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3221ECDBR	SSOP	DB	16	2000	356.0	356.0	35.0
MAX3221ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3221EIDBR	SSOP	DB	16	2000	356.0	356.0	35.0
MAX3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3221EIPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
MAX3221EIPWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0016A

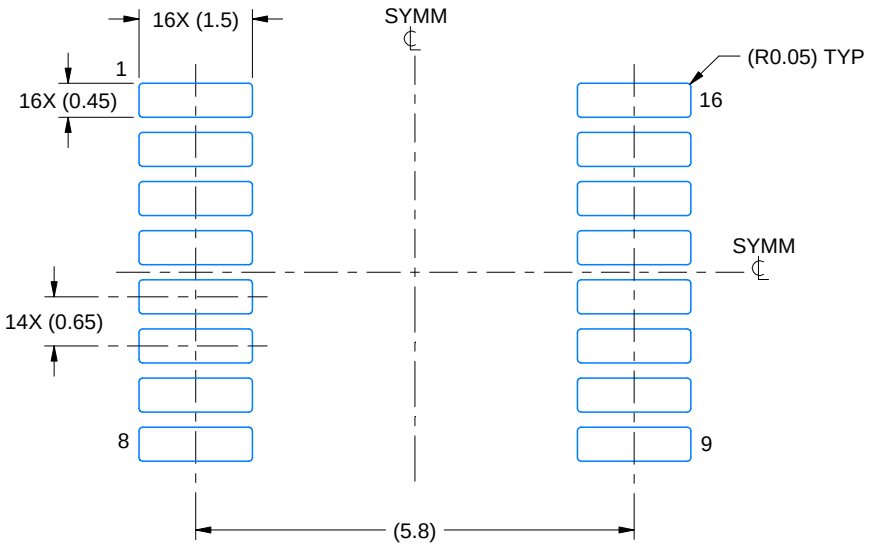
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

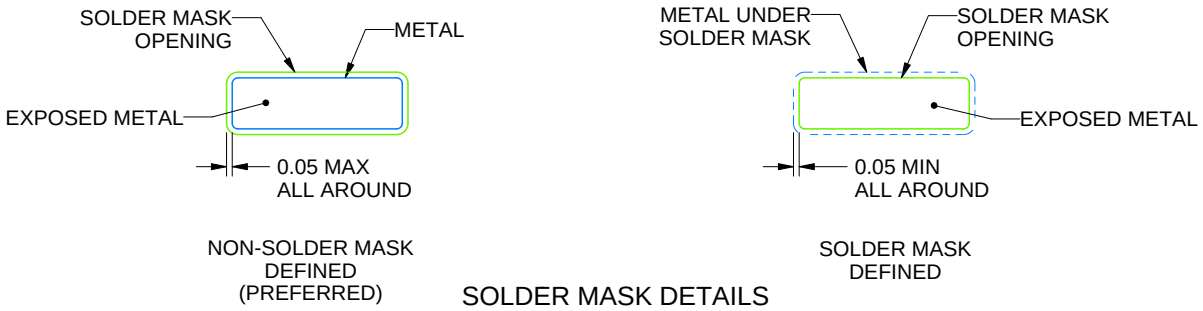


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

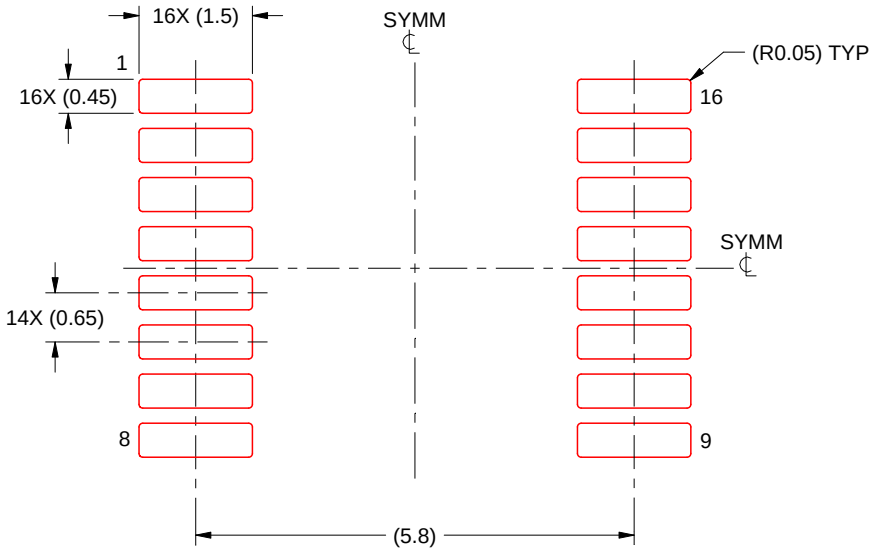


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

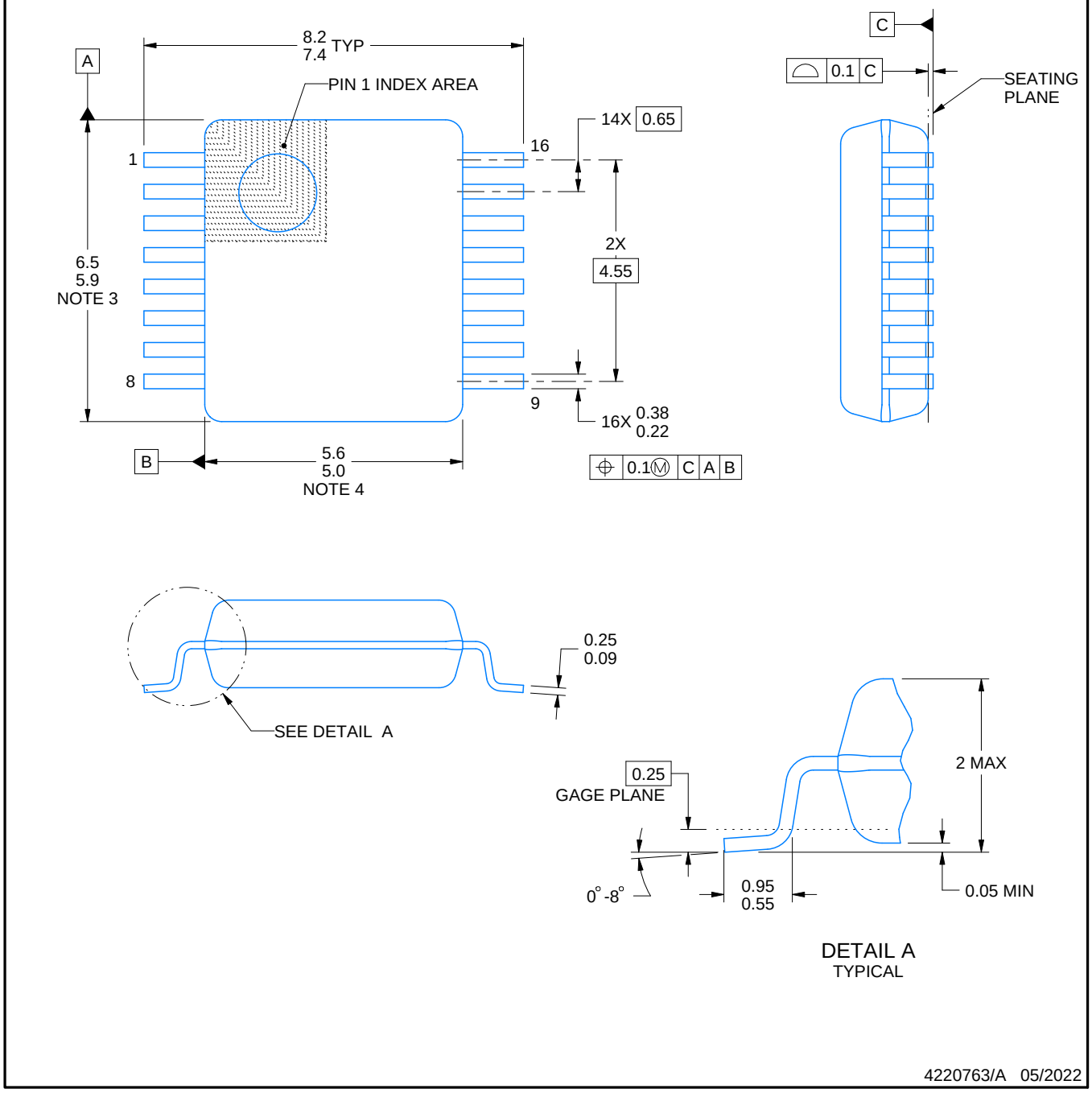
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DB0016A

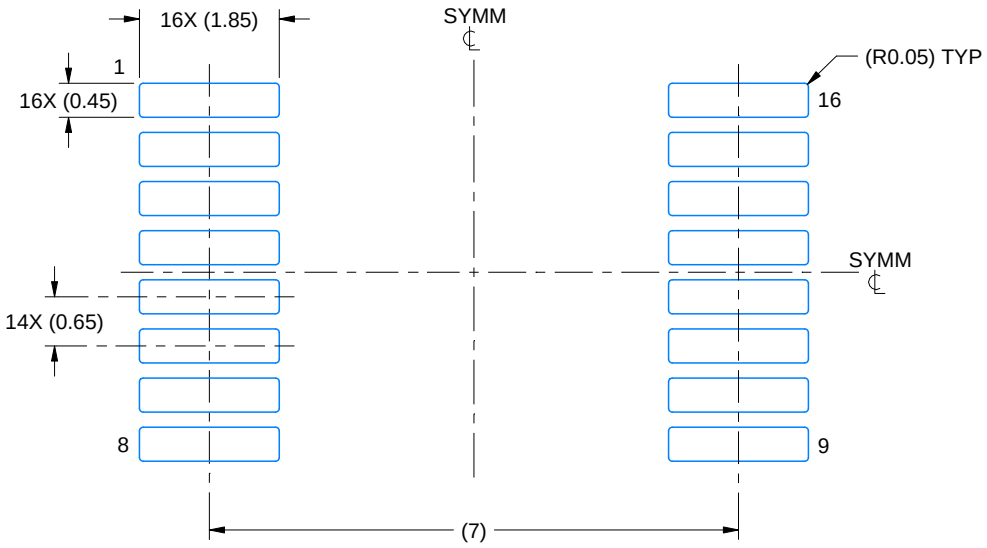
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

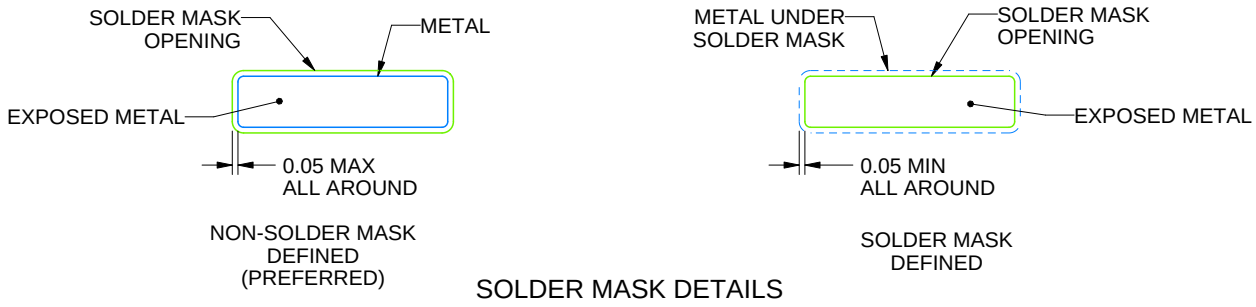


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

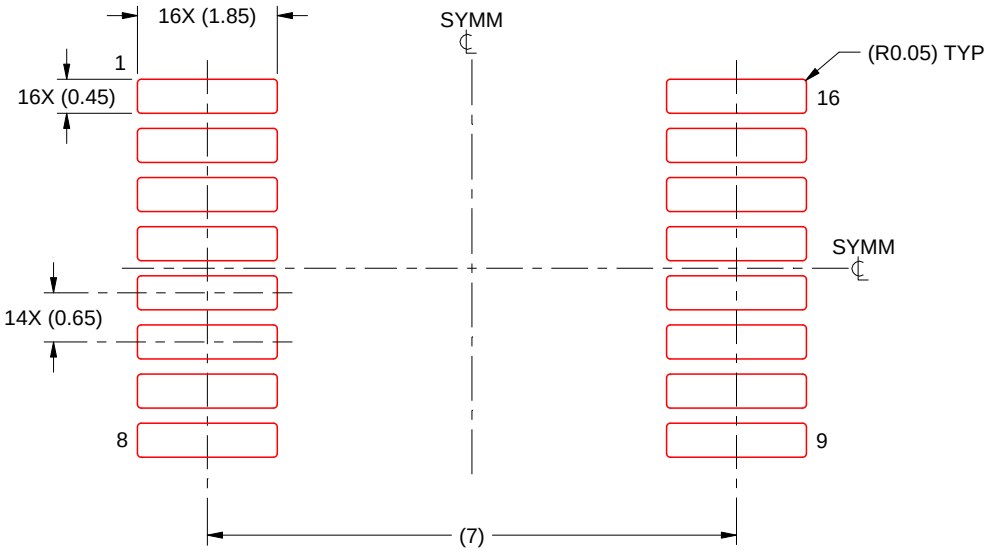


SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265