

PCF8574 リモート 8 ビット I/O エクスパンダ、I²C バス対応

1 特長

- 低いスタンバイ消費電流: 10 μ A 以下
- I²C からパラレルポートへのエクスパンダ
- オープンドレイン割り込み出力
- ほとんどのマイクロコントローラと互換
- 大電流の駆動能力を持つラッチ付き出力により、LED を直接駆動
- JEESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- テレコム シェルター: フィルタ ユニット
- サーバー
- ルーター (テレコム スイッチング機器)
- [パーソナル コンピュータ](#)
- [パーソナル エレクトロニクス](#)
- [産業用オートメーション](#)
- GPIO が制限されたプロセッサを使用する製品

3 概要

この 2 線式双方向バス (I²C) 用 8 ビット入出力 (I/O) エクスパンダは、2.5V~6V の V_{CC} で動作するように設計されています。

PCF8574 デバイスは、I²C インターフェイス [シリアル クロック (SCL)、シリアル データ (SDA)] により、ほとんどのマイクロコントローラ ファミリの汎用リモート I/O 拡張に使用できます。

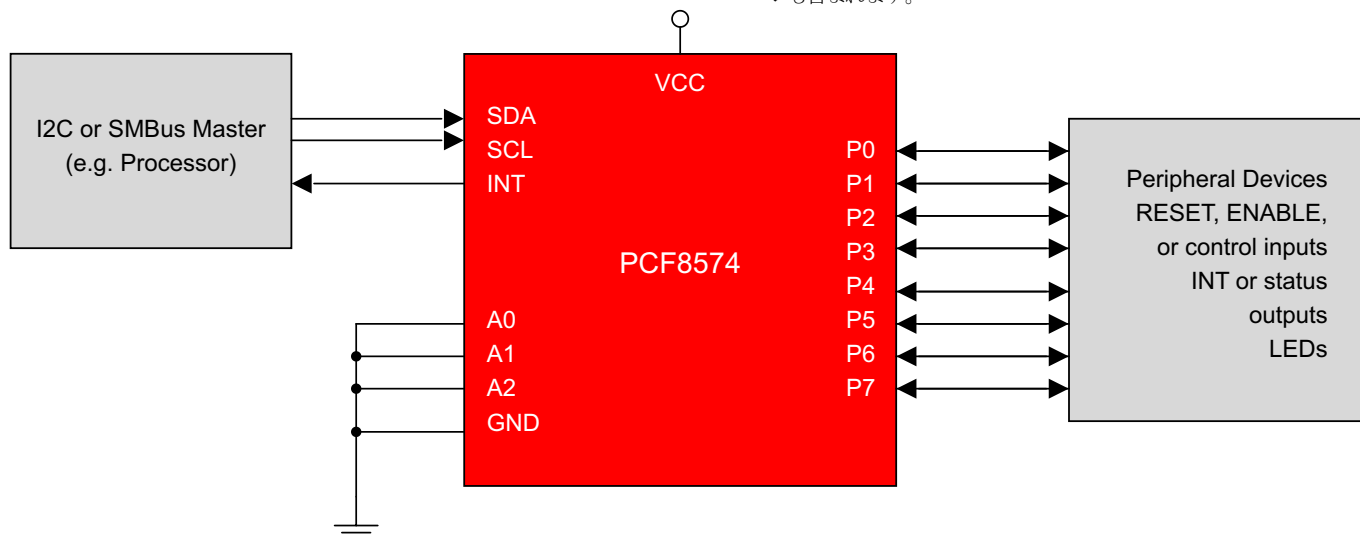
このデバイスには 8 ビット、疑似双方向の I/O ポート (P0~P7) があり、大電流駆動能力を持つラッチ付き出力により LED を直接駆動できます。それぞれの疑似双方向 I/O は、データ方向制御信号を使用せずに、入力または出力として使用できます。電源投入時、I/O は HIGH になります。このモードでは、V_{CC} への電流源のみがアクティブになります。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ サイズ ⁽²⁾
PCF8574	TVSOP (DGV) (20)	5mm × 6.40 mm
	SOIC (DW, 16)	10.3mm × 10.3mm
	PDIP (N, 16)	19.3mm × 9.4 mm
	TSSOP (PW, 20)	6.5mm × 6.4 mm
	VQFN (RGT, 16)	3mm × 3mm
	VQFN (RGY) (20)	4.5mm × 3.5 mm

(1) 詳細については、[セクション 11](#) を参照してください。

(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



Table of Contents

1 特長	1	7.3 Feature Description.....	13
2 アプリケーション	1	7.4 Device Functional Modes.....	14
3 概要	1	8 Application and Implementation	16
4 Pin Configuration and Functions	3	8.1 Application Information.....	16
5 Specifications	4	8.2 Typical Application.....	16
5.1 Absolute Maximum Ratings.....	4	8.3 Power Supply Recommendations.....	18
5.2 ESD Ratings.....	4	8.4 Layout.....	20
5.3 Recommended Operating Conditions.....	4	9 Device and Documentation Support	22
5.4 Thermal Information.....	4	9.1 Documentation Support.....	22
5.5 Electrical Characteristics.....	5	9.2 Receiving Notification of Documentation Updates....	22
5.6 I ² C Interface Timing Requirements.....	5	9.3 サポート・リソース.....	22
5.7 Switching Characteristics.....	6	9.4 Trademarks.....	22
5.8 Typical Characteristics.....	7	9.5 静電気放電に関する注意事項.....	22
6 Parameter Measurement Information	9	9.6 用語集.....	22
7 Detailed Description	12	10 Revision History	22
7.1 Overview.....	12	11 Mechanical, Packaging, and Orderable Information	23
7.2 Functional Block Diagram.....	12		

4 Pin Configuration and Functions

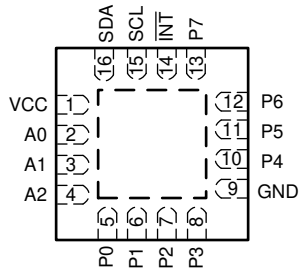


図 4-1. RGT Package, 16 Pins (Top View)

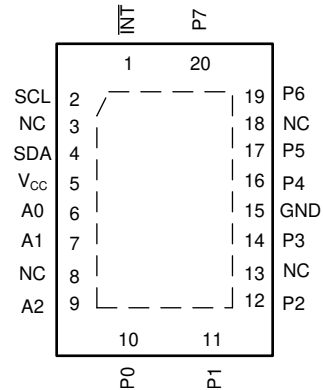


図 4-2. RGY Package, 20 Pins (Top View)

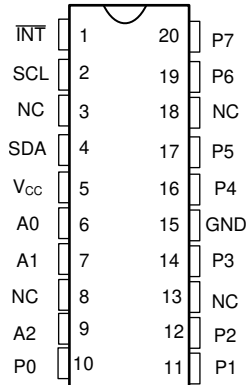


図 4-3. DGV or PW Package, 20 Pins (Top View)

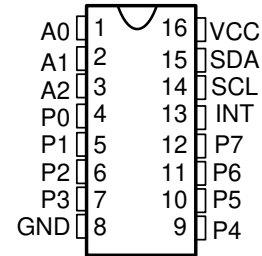


図 4-4. DW or N Package, 20 Pins, Top View

表 4-1. Pin Functions

NAME	PIN				TYPE	DESCRIPTION
	RGT	RGY	DGV or PW	DW or N		
A [0..2]	2, 3, 4	6, 7, 9	6, 7, 9	1, 2, 3	I	Address inputs 0 through 2. Connect directly to V _{CC} or ground. Pullup resistors are not needed.
GND	9	15	15	8	—	Ground
INT	14	1	1	13	O	Interrupt output. Connect to V _{CC} through a pullup resistor.
NC	-	3, 8, 13, 18	3, 8, 13, 18	-	—	Do not connect
P[0..7]	5, 6, 7, 8, 10, 11, 12, 13	10, 11, 12, 14, 16, 17, 19, 20	10, 11, 12, 14, 16, 17, 19, 20	4, 5, 6, 7, 9, 10, 11, 12	I/O	P-port input/output. Push-pull design structure.
SCL	15	2	2	14	I	Serial clock line. Connect to V _{CC} through a pullup resistor
SDA	16	4	4	15	I/O	Serial data line. Connect to V _{CC} through a pullup resistor.
V _{CC}	1	5	5	16	—	Voltage supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		-0.5	6.5	V
V _I	Input voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
V _O	Output voltage range ⁽²⁾		-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		-20	mA
I _{OK}	Output clamp current	V _O < 0		-20	mA
I _{OK}	Input/output clamp current	V _O < 0 or V _O > V _{CC}		±400	µA
I _{OL}	Continuous output low current	V _O = 0 to V _{CC}		50	mA
I _{OH}	Continuous output high current	V _O = 0 to V _{CC}		-4	mA
	Continuous current through V _{CC} or GND			±100	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature range		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	2000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.5	6	V
V _{IH}	High-level input voltage	0.7 × V _{CC}	V _{CC} + 0.5	V
V _{IL}	Low-level input voltage	-0.5	0.3 × V _{CC}	V
I _{OH}	High-level output current		-1	mA
I _{OL}	Low-level output current		25	mA
T _A	Operating free-air temperature	-40	85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		PCF8574						UNIT
		DGV	DW	N	PW	RGT	RGY	
		20 PINS	16 PINS	16 PINS	20 PINS	16 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	92	76.7	73.1	94.8	56.0	52.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	-	45.1	51.9	40.2	67.4	50.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	-	45.8	48.3	58.5	31.2	29.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	-	17.2	29.8	2.8	3.9	3.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	-	45.2	47.9	58.0	31.1	29.1	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	-	n/a	n/a	n/a	15.1	16.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	VCC	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input diode clamp voltage	I _I = -18 mA	2.5 V to 6 V	-1.2			V
V _{POR}	Power-on reset voltage	V _I = V _{CC} or GND, I _O = 0	6 V		1.3	2.4	V
I _{OH}	P port	V _O = GND	2.5 V to 6 V	-310		-30	μA
I _{OHT}	P port transient pullup current	High during acknowledge, V _{OH} = GND	2.5 V		-1		mA
I _{OL}	SDA	V _O = 0.4 V	2.5 V to 6 V		3		mA
	P port	V _O = 1 V	5 V		10	25	
	INT	V _O = 0.4 V	2.5 V to 6 V		1.6		
I _I	SCL, SDA	V _I = V _{CC} or GND	2.5 V to 6 V			±5	μA
	INT					±5	
	A0, A1, A2					±5	
I _{IHL}	P port	-250mV < V _I < GND	2.5 V to 6 V			±400	μA
I _{CC}	Operating mode	V _I = V _{CC} or GND, I _O = 0, f _{SCL} = 100 kHz	6 V		40	100	μA
	Standby mode	V _I = V _{CC} or GND, I _O = 0			2.5	10	
C _i	SCL	V _I = V _{CC} or GND	2.5 V to 6 V		1.5	7	pF
C _{io}	SDA	V _{IO} = V _{CC} or GND	2.5 V to 6 V		3	7	pF
	P port				4	10	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
f _{scl}	I ² C clock frequency		100	kHz
t _{sch}	I ² C clock high time	4		μs
t _{scl}	I ² C clock low time	4.7		μs
t _{sp}	I ² C spike time		70	ns
t _{sds}	I ² C serial data setup time	250		ns
t _{sdh}	I ² C serial data hold time	0		ns
t _{icr}	I ² C input rise time		1	μs
t _{icf}	I ² C input fall time		0.3	μs
t _{ocf}	I ² C output fall time (10-pF to 400-pF bus)		300	ns
t _{buf}	I ² C bus free time between stop and start	4.7		μs
t _{sts}	I ² C start or repeated start condition setup	4.7		μs
t _{sth}	I ² C start or repeated start condition hold	4		μs
t _{sps}	I ² C stop condition setup	4		μs
t _{vd}	Valid data time	SCL low to SDA output valid		3.4
C _b	I ² C bus capacitive load		400	pF

5.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pv}	Output data valid	SCL	P port		4	μ s
t_{su}	Input data setup time	P port	SCL	0		μ s
t_h	Input data hold time	P port	SCL	4		μ s
t_{iv}	Interrupt valid time	P port	INT		4	μ s
t_{ir}	Interrupt reset delay time	SCL	INT		4	μ s

5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

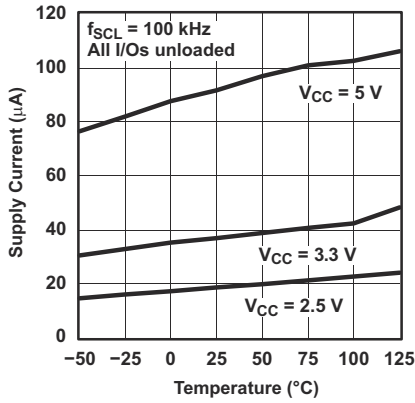


图 5-1. Supply Current vs Temperature

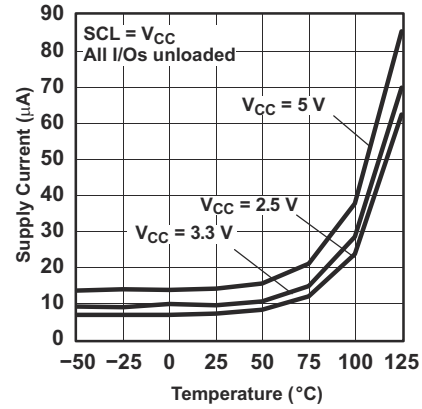


图 5-2. Standby Supply Current vs Temperature

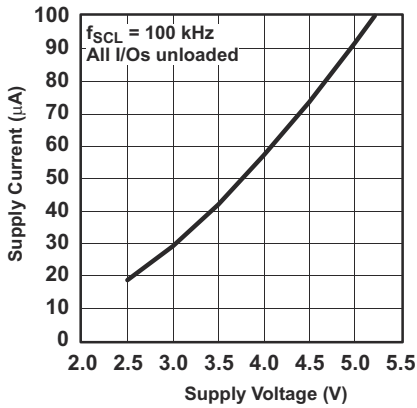


图 5-3. Supply Current vs Supply Voltage

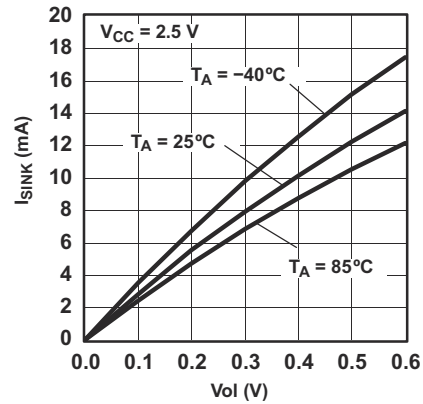


图 5-4. I/O Sink Current vs Output Low Voltage

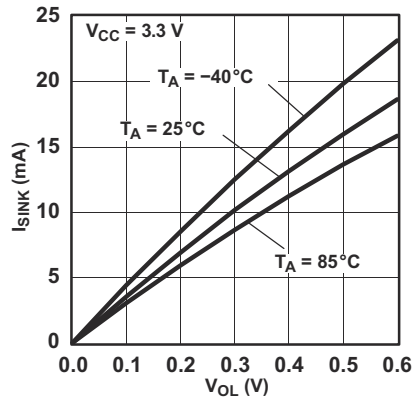


图 5-5. I/O Sink Current vs Output Low Voltage

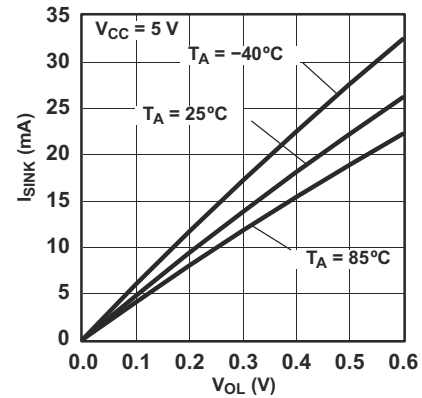


图 5-6. I/O Sink Current vs Output Low Voltage

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

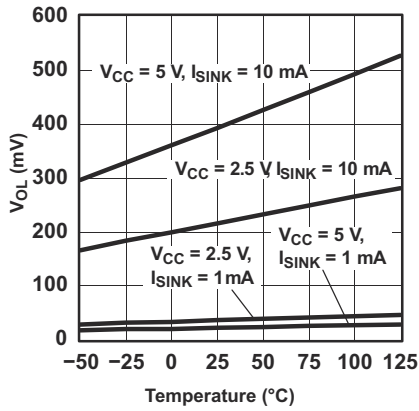


图 5-7. I/O Output Low Voltage vs Temperature

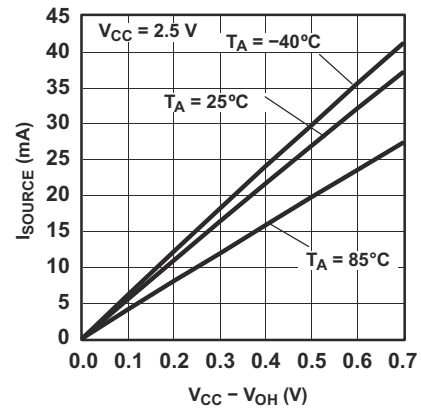


图 5-8. I/O Source Current vs Output High Voltage

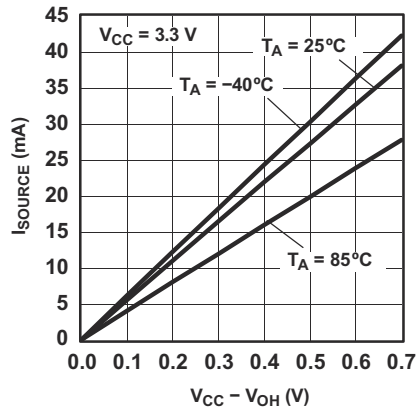


图 5-9. I/O Source Current vs Output High Voltage

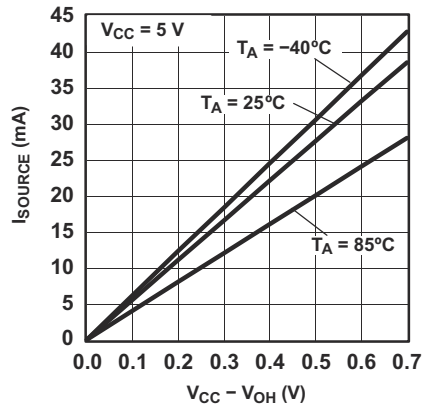


图 5-10. I/O Source Current vs Output High Voltage

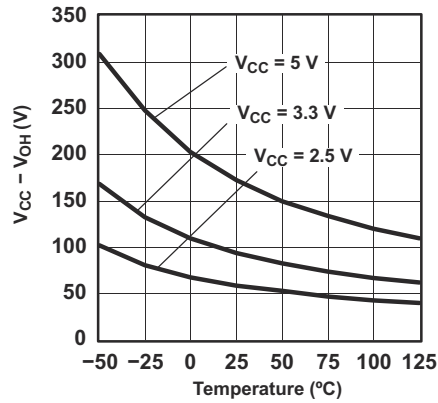
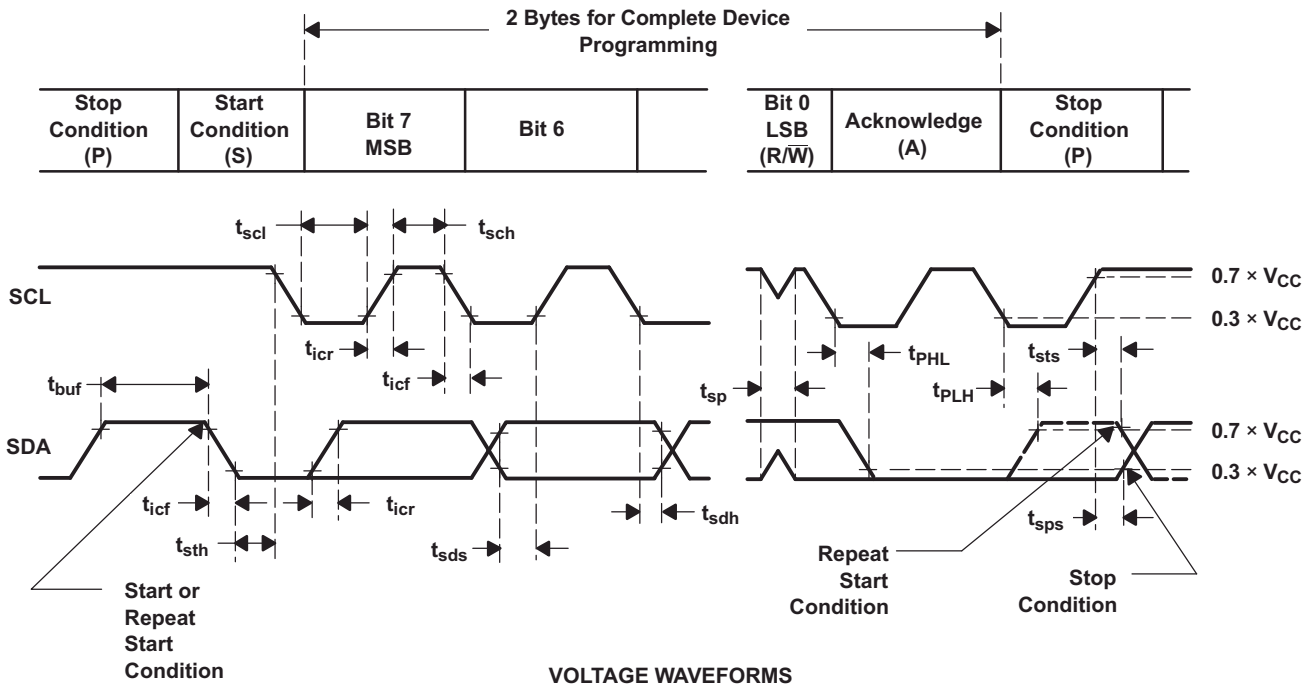
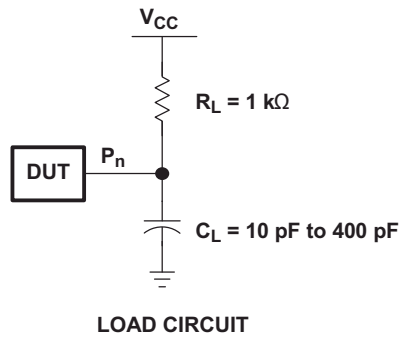
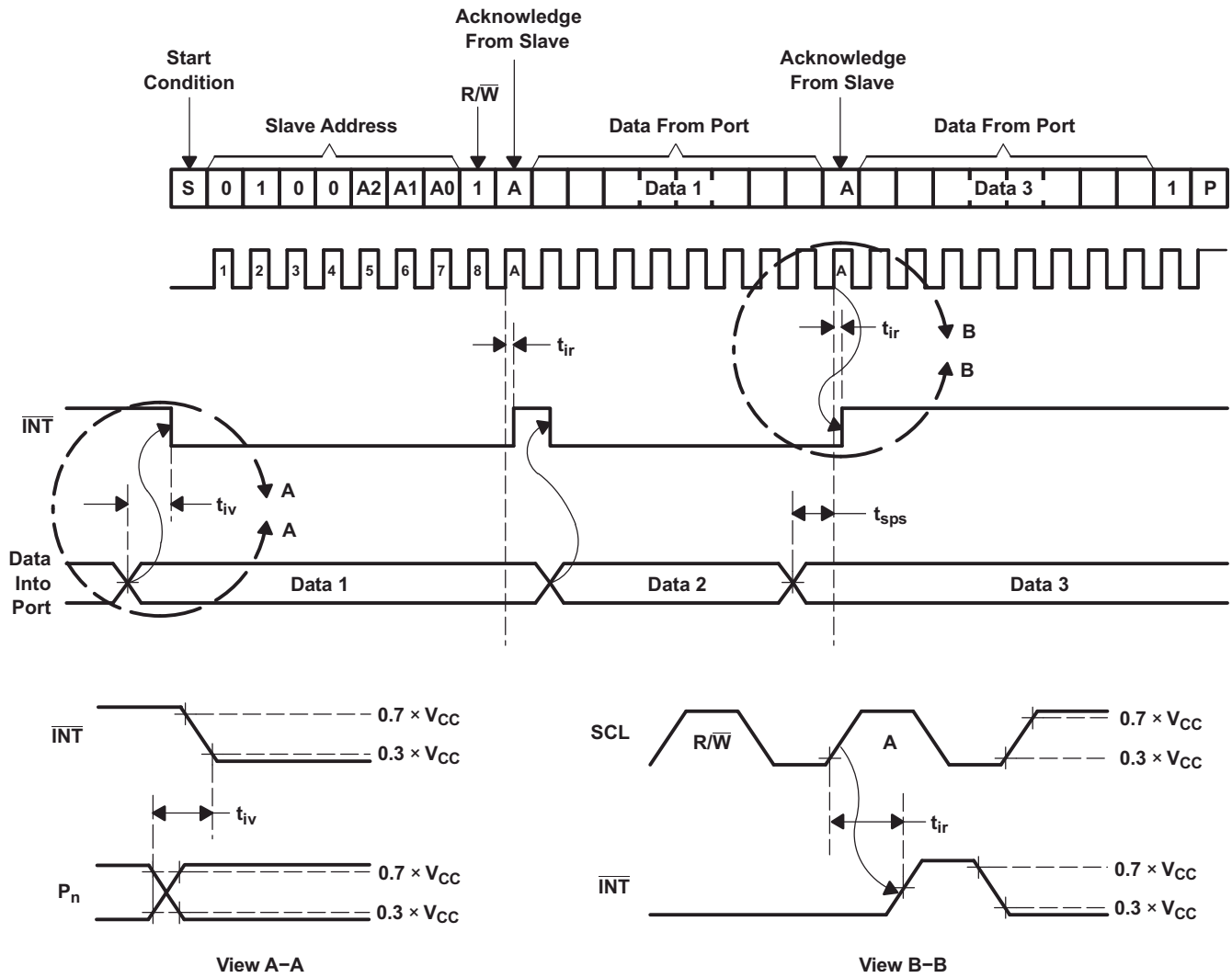


图 5-11. I/O High Voltage vs Temperature

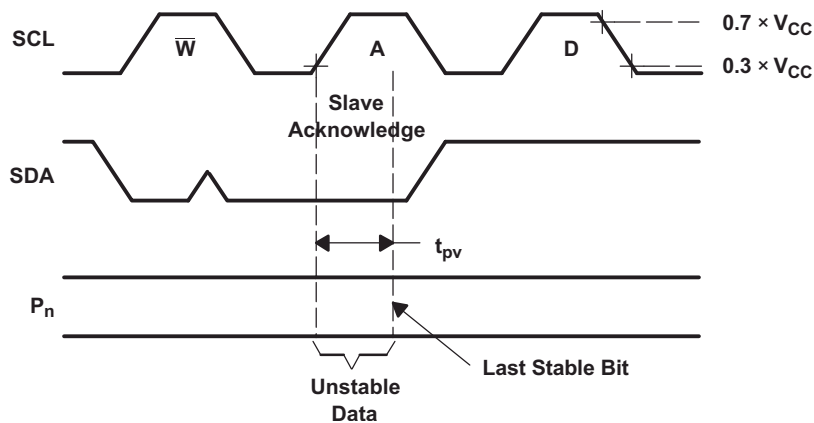
6 Parameter Measurement Information



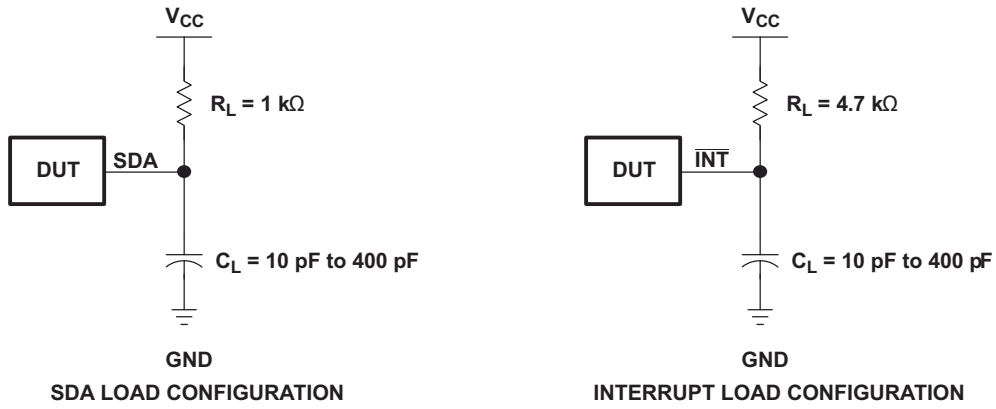
6-1. I²C Interface Load Circuit and Voltage Waveforms



6-2. Interrupt Voltage Waveforms



6-3. I²C Write Voltage Waveforms



6-4. Load Circuits

7 Detailed Description

7.1 Overview

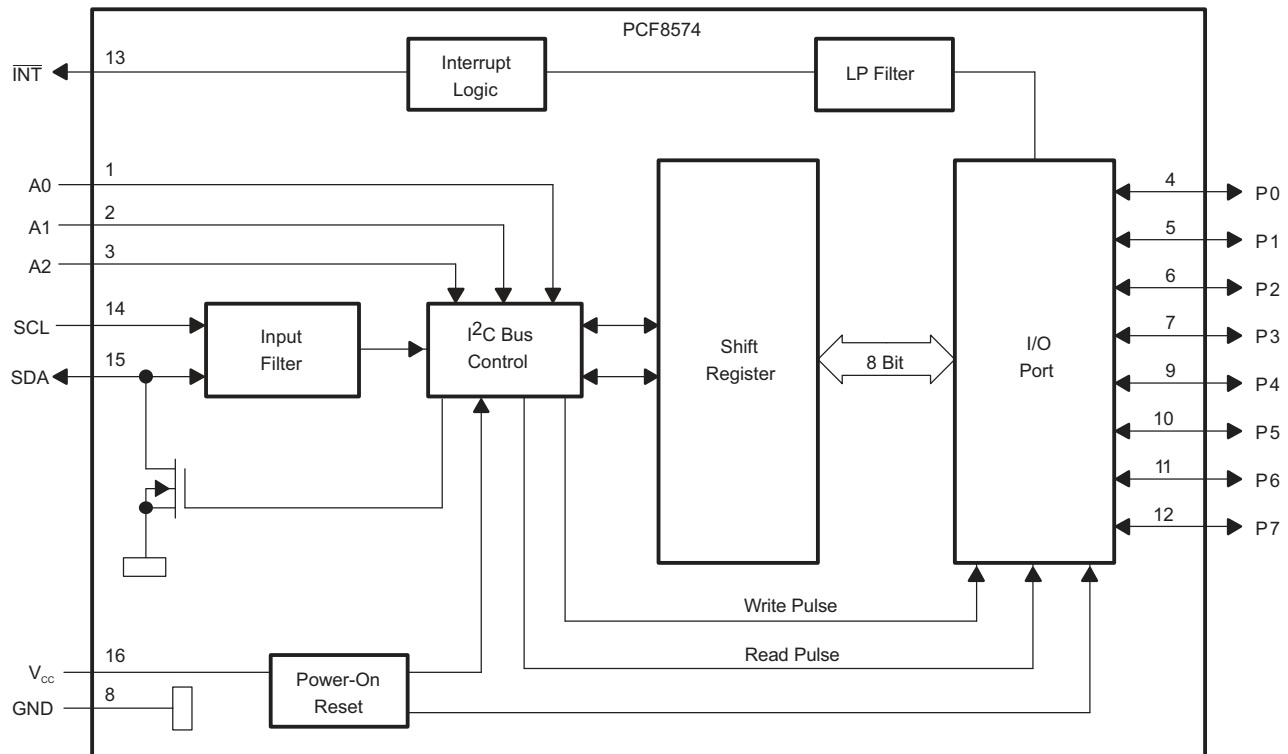
The PCF8574 device is an 8-bit I/O expander for the two-line bidirectional bus (I²C) is designed for 2.5-V to 6-V V_{CC} operation. It provides general-purpose remote I/O expansion for most micro-controller families via the I²C interface (serial clock, SCL, and serial data, SDA, pins).

The PCF8574 device provides an open-drain output (\overline{INT}) that can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv} , \overline{INT} is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from, or written to, the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge bit after the rising edge of the SCL signal, or in the write mode at the acknowledge bit after the high-to-low transition of the SCL signal. Interrupts that occur during the acknowledge clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and, after the next rising clock edge, is transmitted as \overline{INT} . Reading from, or writing to, another device does not affect the interrupt circuit. This device does not have internal configuration or status registers. Instead, read or write to the device I/Os directly after sending the device address (see [Figure 7-3](#) and [Figure 7-4](#)).

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate by way of the I²C bus. Therefore, PCF8574 can remain a simple target device.

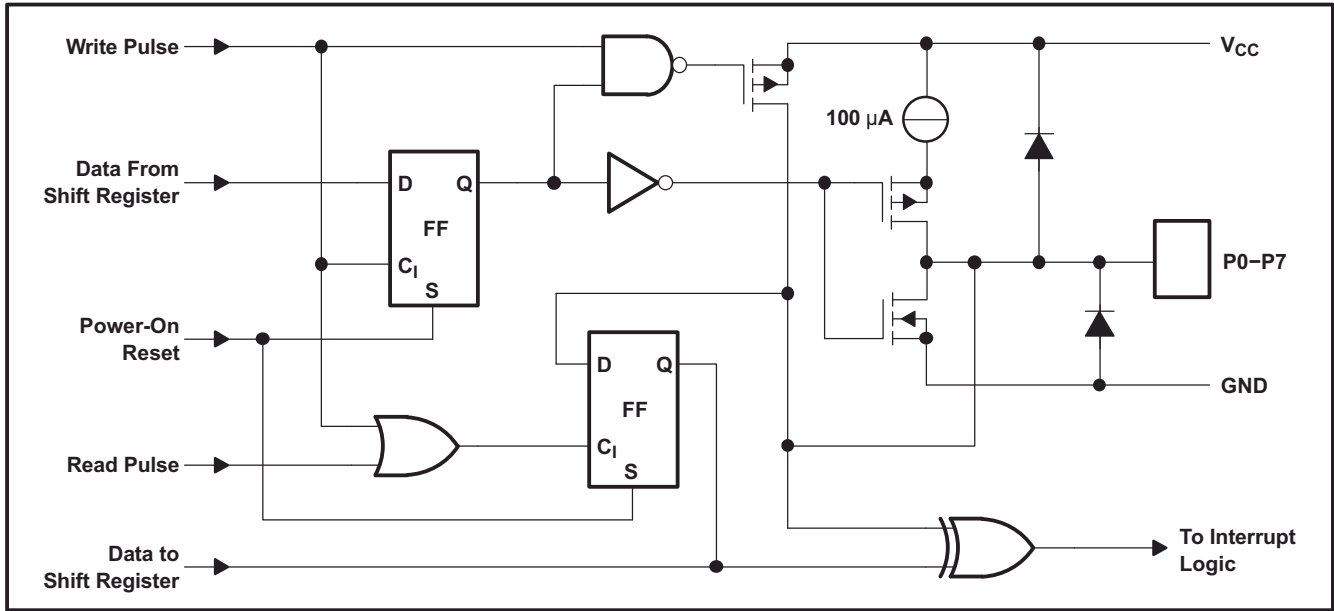
An additional strong pullup to V_{CC} allows fast rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs.

7.2 Functional Block Diagram



Pin numbers shown are for the DW and N packages.

Figure 7-1. Simplified Block Diagram of Device



7-2. Simplified Schematic Diagram of Each P-Port Input or Output

7.3 Feature Description

7.3.1 I²C Interface

I²C communication with this device is initiated by a controller sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/\bar{W}). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0–A2) of the target device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the R/\bar{W} bit is high, the data from this device are the values read from the P port. If the R/\bar{W} bit is low, the data are from the controller, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the controller, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time, t_{pv} , after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the controller.

7.3.2 Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I ² C target address	L	H	L	L	A2	A1	A0	R/\bar{W}
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

7.3.3 Address Reference

INPUTS			I ² C BUS TARGET 8-BIT READ ADDRESS	I ² C BUS TARGET 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	65 (decimal), 41 (hexadecimal)	64 (decimal), 40 (hexadecimal)
L	L	H	67 (decimal), 43 (hexadecimal)	66 (decimal), 42 (hexadecimal)
L	H	L	69 (decimal), 45 (hexadecimal)	68 (decimal), 44 (hexadecimal)
L	H	H	71 (decimal), 47 (hexadecimal)	70 (decimal), 46 (hexadecimal)
H	L	L	73 (decimal), 49 (hexadecimal)	72 (decimal), 48 (hexadecimal)
H	L	H	75 (decimal), 4B (hexadecimal)	74 (decimal), 4A (hexadecimal)
H	H	L	77 (decimal), 4D (hexadecimal)	76 (decimal), 4C (hexadecimal)
H	H	H	79 (decimal), 4F (hexadecimal)	78 (decimal), 4E (hexadecimal)

7.4 Device Functional Modes

Figure 7-3 and Figure 7-4 show the address and timing diagrams for the write and read modes, respectively.

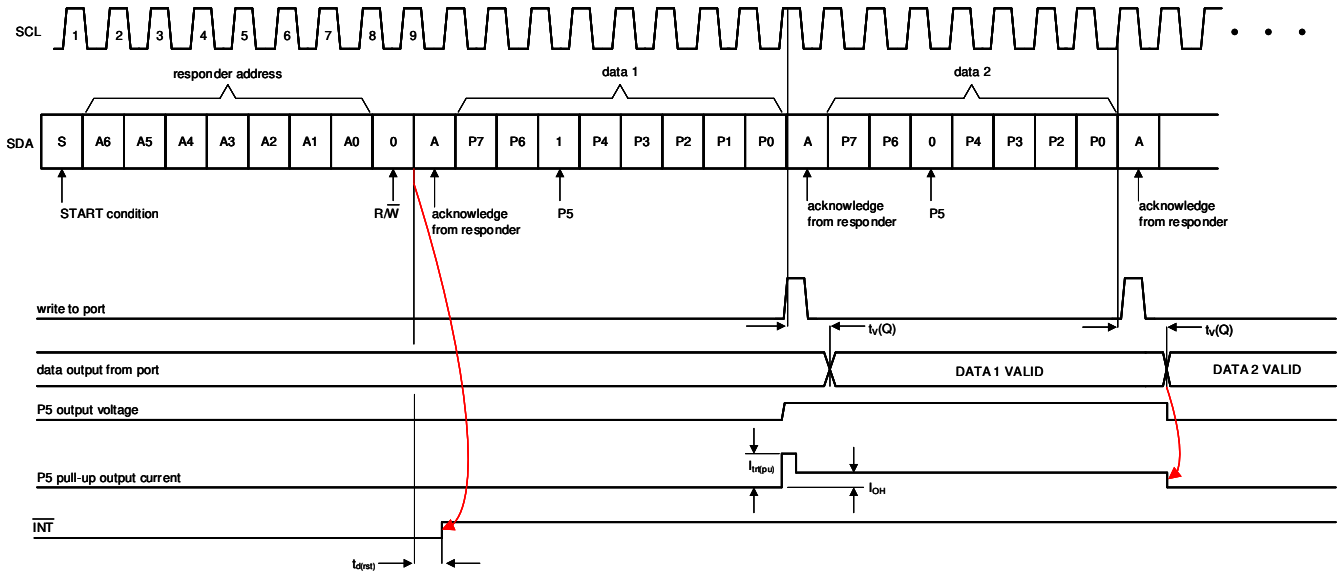
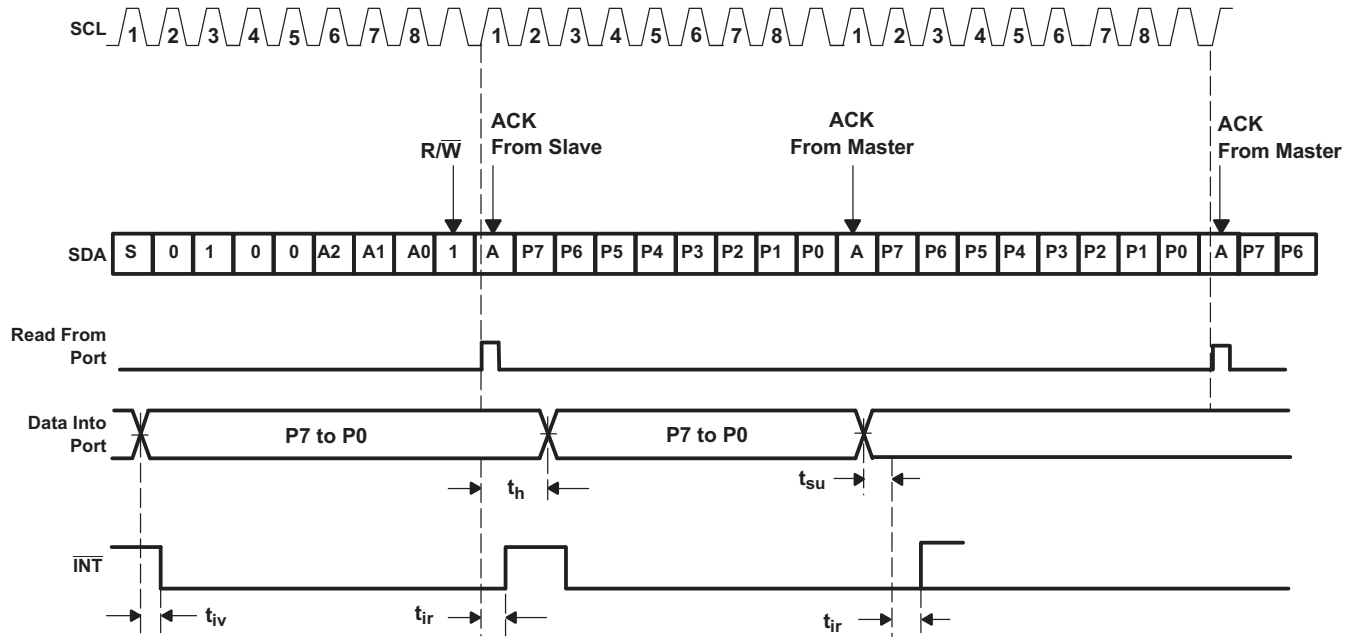


Figure 7-3. Write Mode (Output)



- A. A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

7-4. Read Mode (Input)

8 Application and Implementation

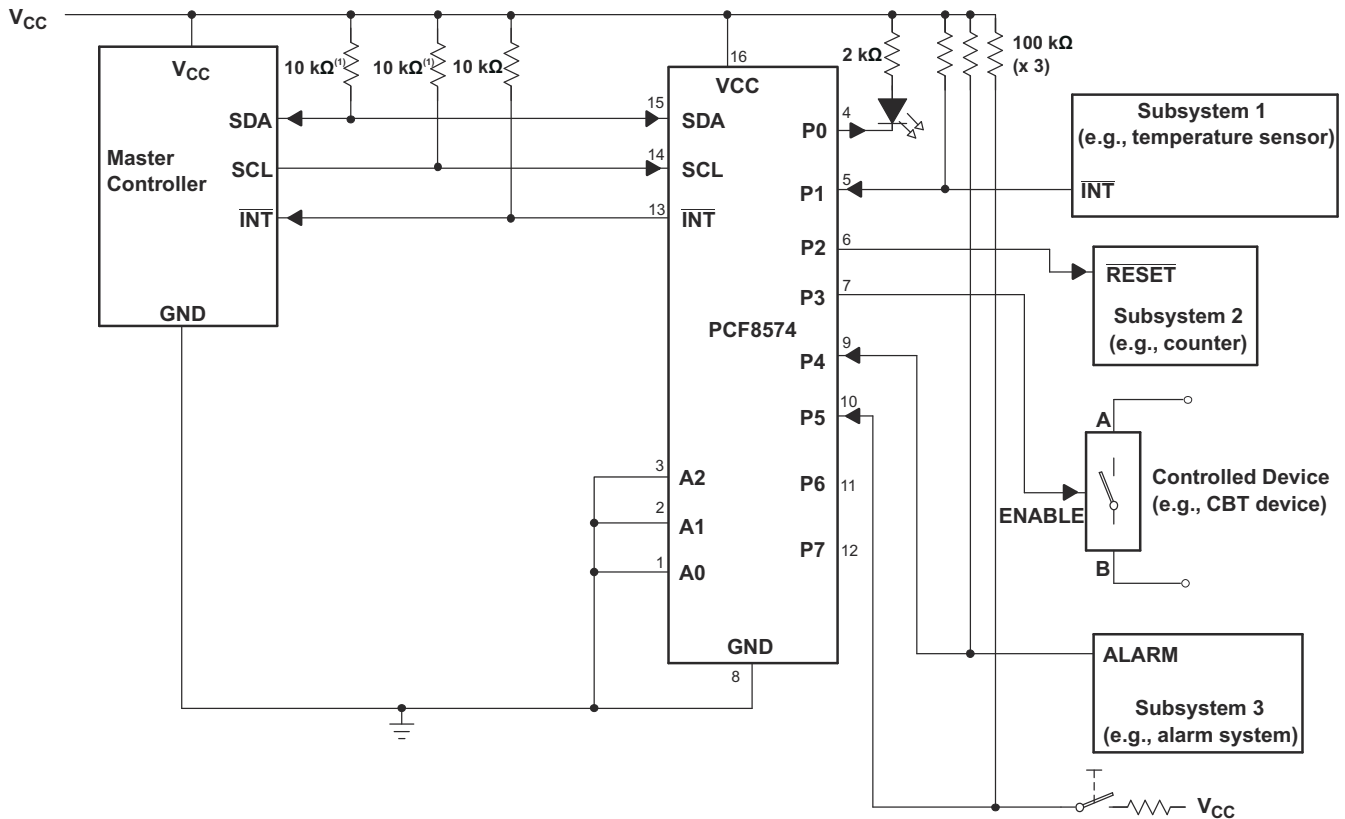
注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

図 8-1 shows an application in which the PCF8574 device can be used.

8.2 Typical Application



- The SCL and SDA pins must be tied directly to V_{CC} because if SCL and SDA are tied to an auxiliary power supply that could be powered on while V_{CC} is powered off, then the supply current, I_{CC}, will increase as a result.
- Device address is configured as 0100000 for this example.
- P0, P2, and P3 are configured as outputs.
- P1, P4, and P5 are configured as inputs.
- P6 and P7 are not used and must be configured as outputs.

図 8-1. Application Schematic

8.2.1 Design Requirements

8.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in [Figure 8-1](#). For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC} . The LED is a diode, with threshold voltage V_T , and when a P-port is configured as an input the LED will be off but V_I is a V_T drop below V_{CC} .

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. [Figure 8-2](#) shows a high-value resistor in parallel with the LED. [Figure 8-3](#) shows V_{CC} less than the LED supply voltage by at least V_T . Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

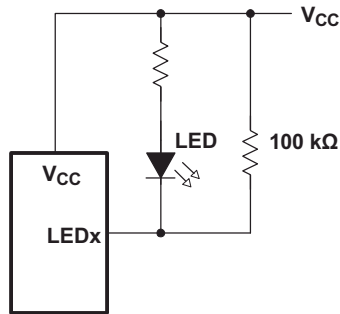


Figure 8-2. High-Value Resistor in Parallel With LED

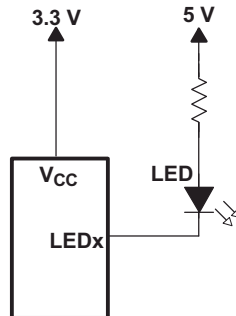


Figure 8-3. Device Supplied by a Lower Voltage

8.2.2 Detailed Design Procedure

The pull-up resistors, R_p , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I²C bus. The minimum pull-up resistance is a function of V_{CC} , $V_{OL(max)}$, and I_{OL} :

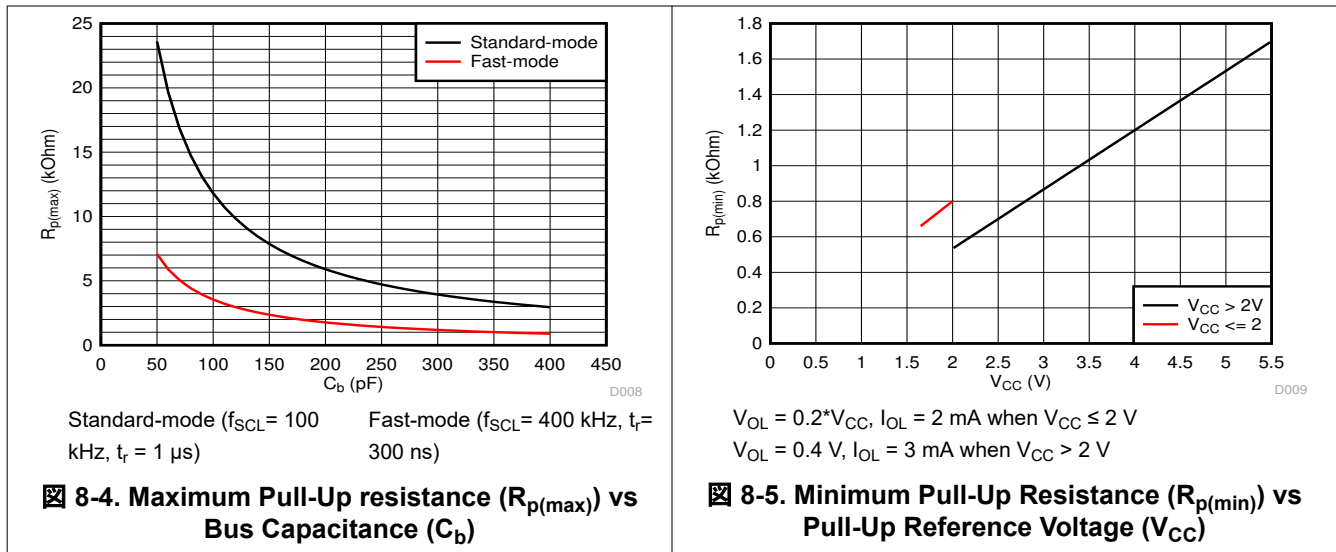
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, $f_{SCL} = 400$ kHz) and bus capacitance, C_b :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I²C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8574 device, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional targets on the bus.

8.2.3 Application Curves



8.3 Power Supply Recommendations

8.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, the PCF8574 device can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 8-6](#) and [Figure 8-7](#).

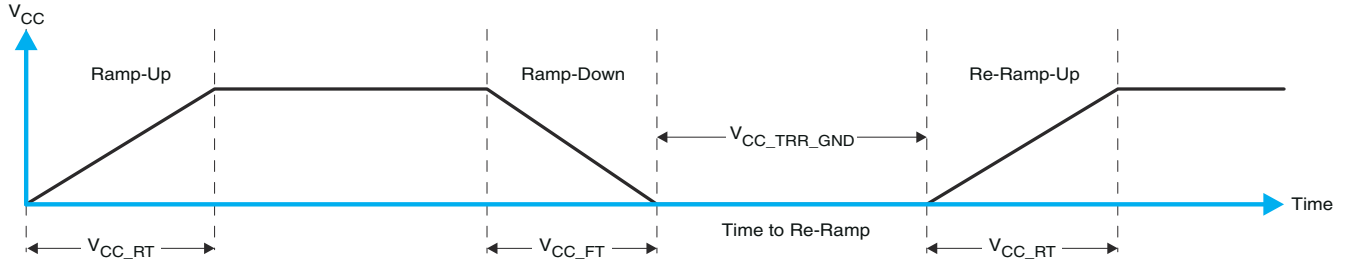


図 8-6. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

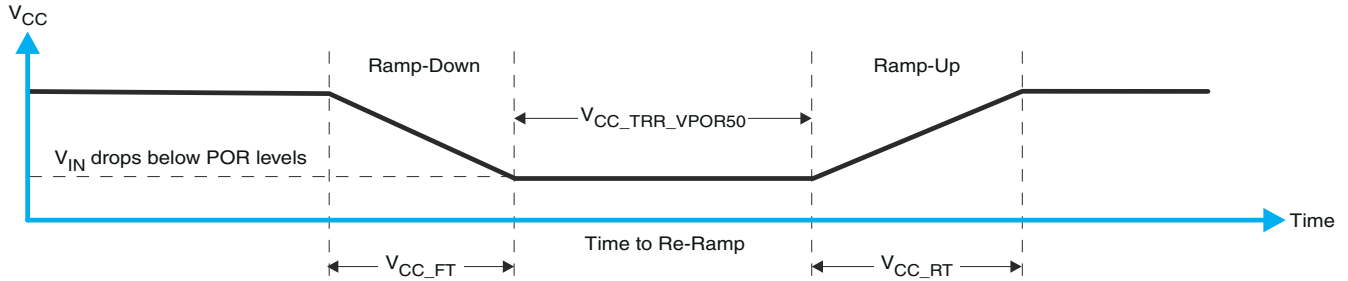


図 8-7. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

表 8-1 specifies the performance of the power-on reset feature for PCF8574 for both types of power-on reset.

表 8-1. Recommended Supply Sequencing and Ramp Rates ⁽¹⁾

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 図 8-6	1		100	ms
V_{CC_RT}	Rise rate	See 図 8-6	0.01		100	ms
$V_{CC_TRR_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 図 8-6	0.001			ms
$V_{CC_TRR_VPOR50}$	Time to re-ramp (when V_{CC} drops to $V_{POR_MIN} - 50$ mV)	See 図 8-7	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when $V_{CCX_GW} = 1$ μ s	See 図 8-8			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when $V_{CCX_GH} = 0.5 \times V_{CCx}$	See 図 8-8				μ s
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.99		1.28	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.190		1.410	V

(1) $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. 図 8-8 and 表 8-1 provide more information on how to measure these specifications.

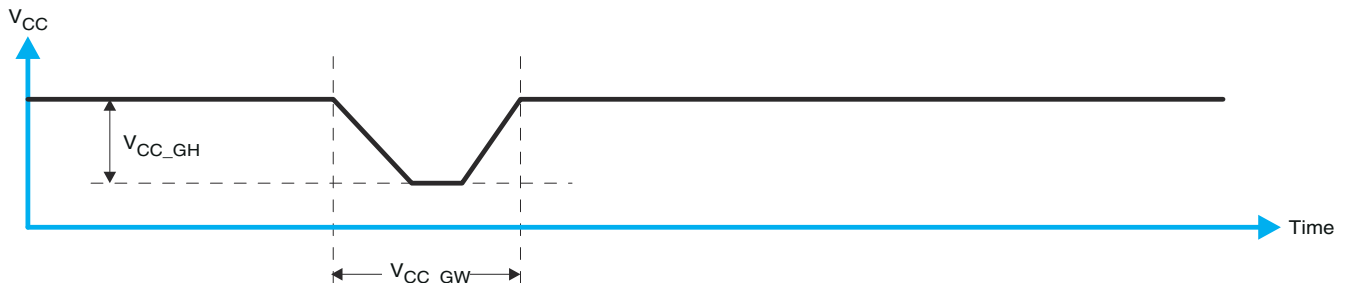


図 8-8. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 図 8-9 and 表 8-1 provide more details on this specification.

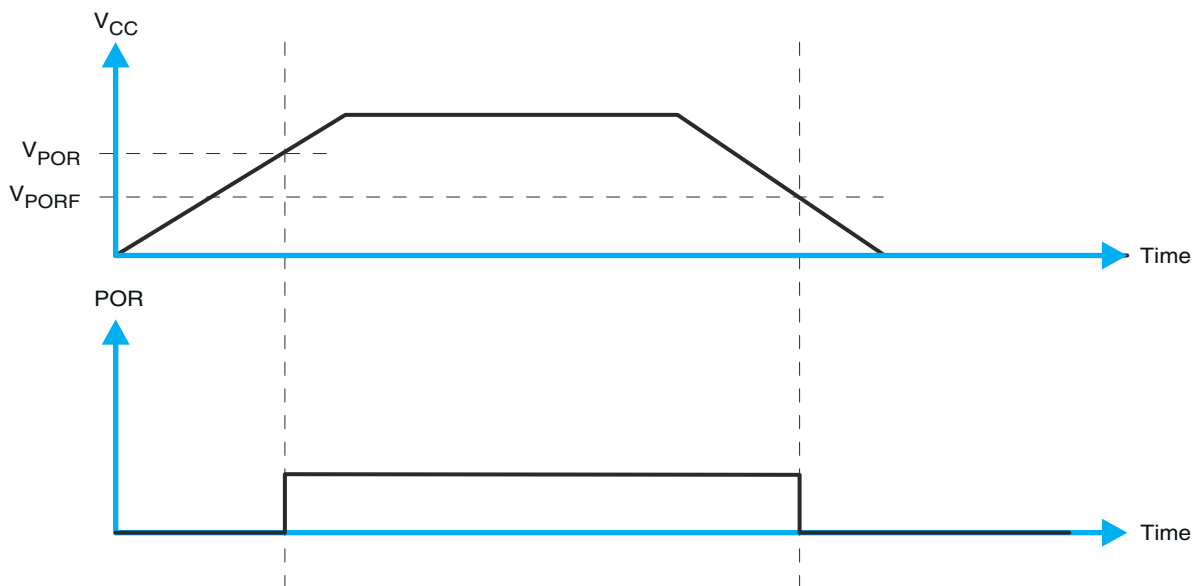


図 8-9. V_{POR}

8.4 Layout

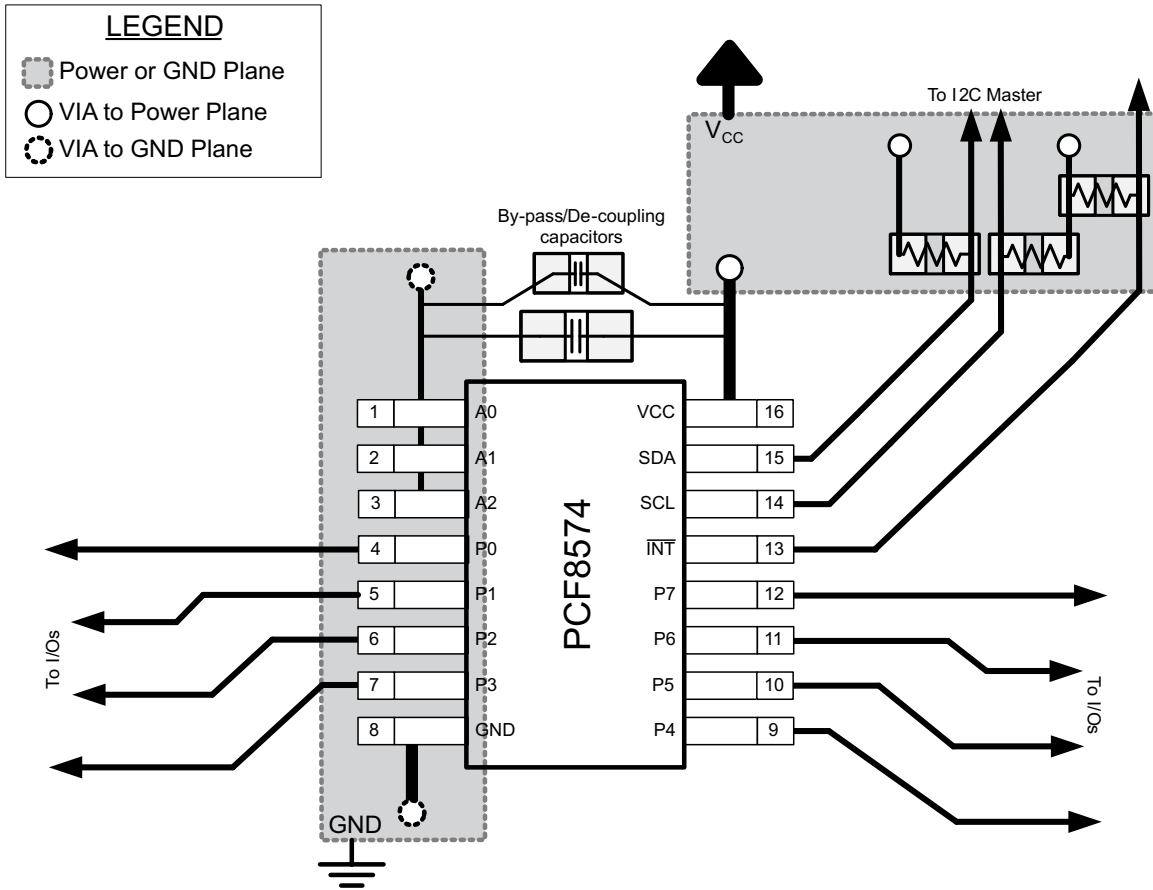
8.4.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCF8574 device, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8574 device as possible. These best practices are shown in 図 8-10.

For the layout example provided in 図 8-10, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (VCC) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to VCC or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in 図 8-10.

8.4.2 Layout Example



☒ 8-10. Layout Example for PCF8574

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms and definitions.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

9.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from Revision J (March 2016) to Revision K (September 2024)	Page
• I ² C に言及している場合、すべての旧式の用語をコントローラおよびターゲットに変更.....	1
• 「製品情報」表を「パッケージ情報」表に変更.....	1
• Update <i>Absolute Max Voltage</i> from 7V to 6.5V.....	4
• Update <i>Thermal Information</i> for RGY, PW, RGT, N and DW packages.....	4
• Update I _{OH} polarity and increase limit from -300μA to -310μA.....	5
• Removed footnote #2 from <i>Electrical Characteristics</i>	5
• Updated I _{IHL} test condition.....	5
• Changed Spike filter limit from 100ns to 70ns max.....	5
• Changed 図 7-3	14
• Updated VPORF and VPORR values.....	18

Changes from Revision I (November 2015) to Revision J (March 2016)**Page**

- 「製品情報」表の部品番号を修正 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8574DGVR	ACTIVE	TVSOP	DGV	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574	Samples
PCF8574DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574	Samples
PCF8574N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574N	Samples
PCF8574NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	PCF8574N	Samples
PCF8574PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 85	PF574	
PCF8574PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574	Samples
PCF8574RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZWJ	Samples
PCF8574RGYR	ACTIVE	VQFN	RGY	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

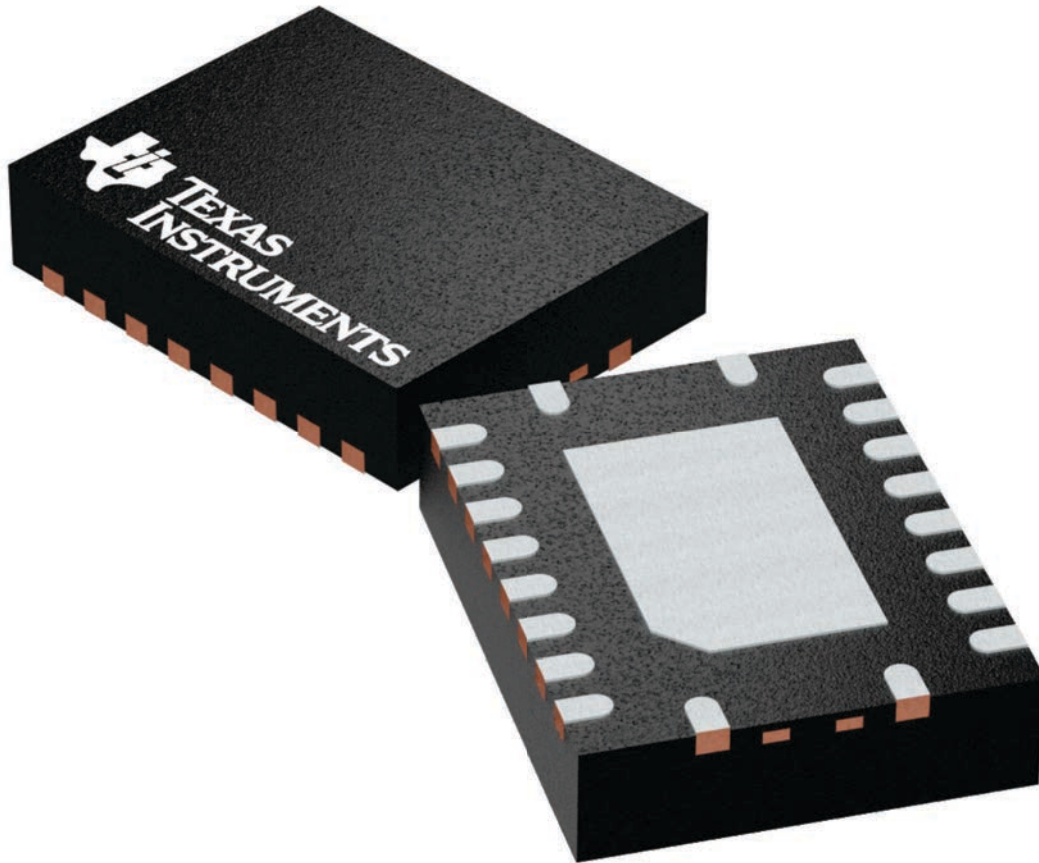
RGY 20

VQFN - 1 mm max height

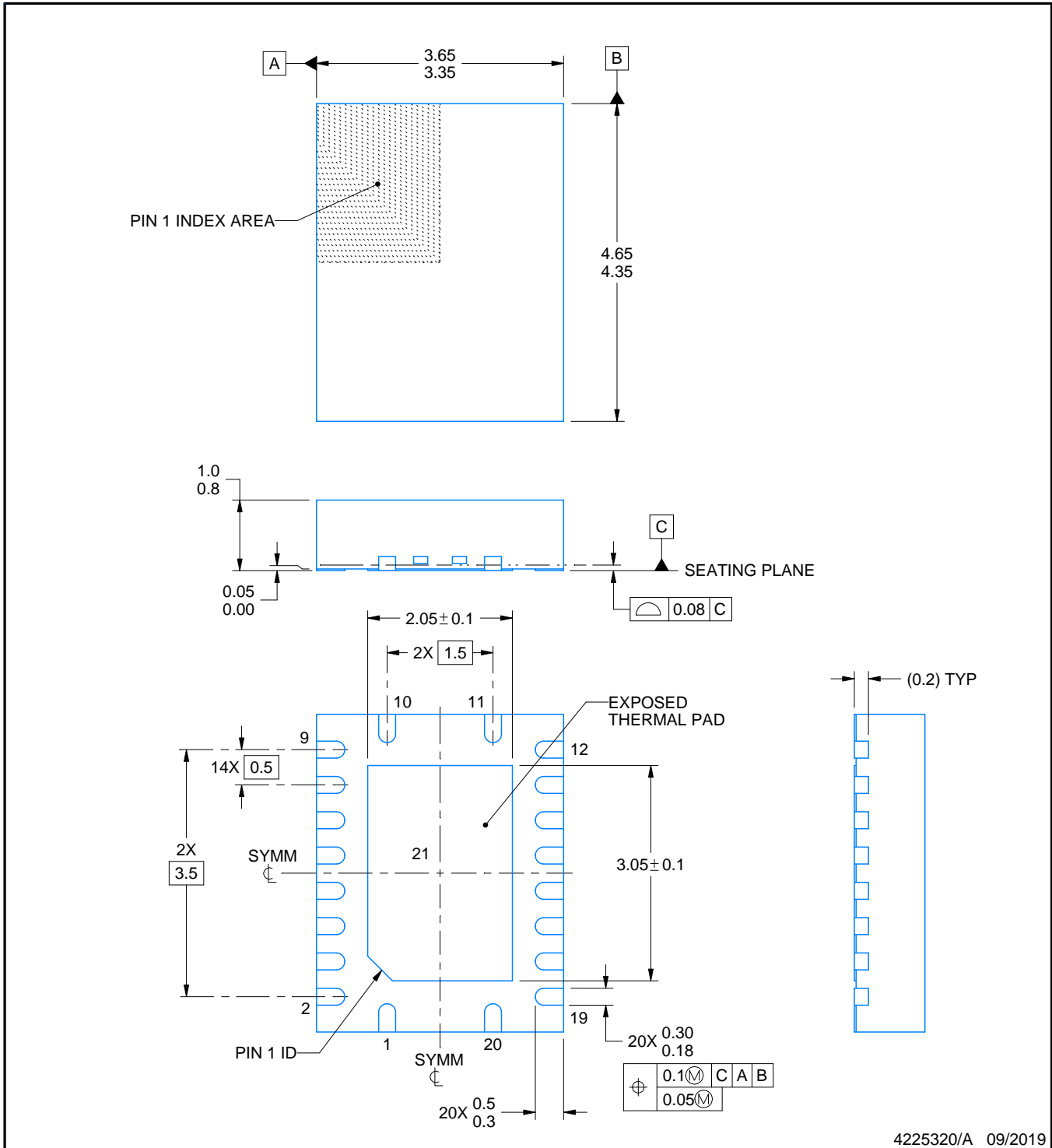
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4225320/A 09/2019

NOTES: (continued)

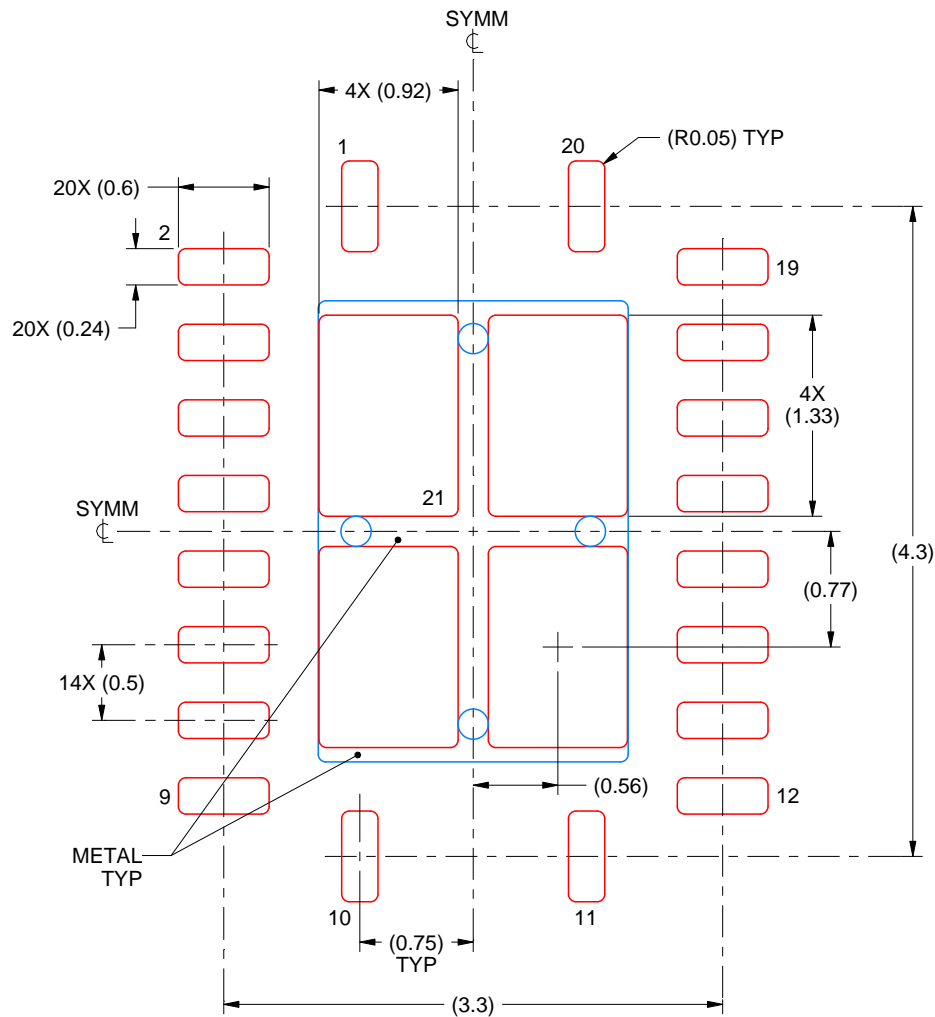
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

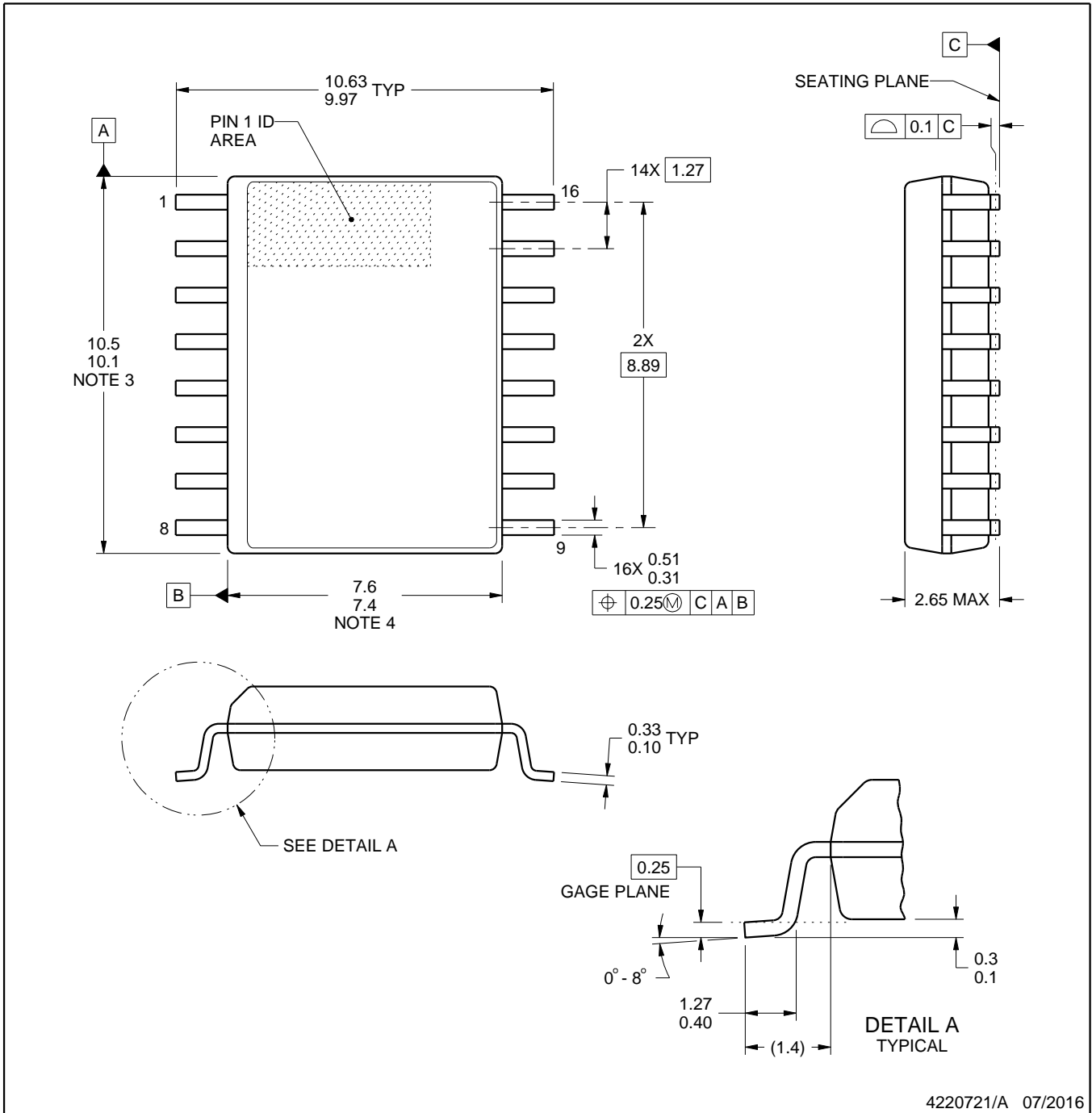


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

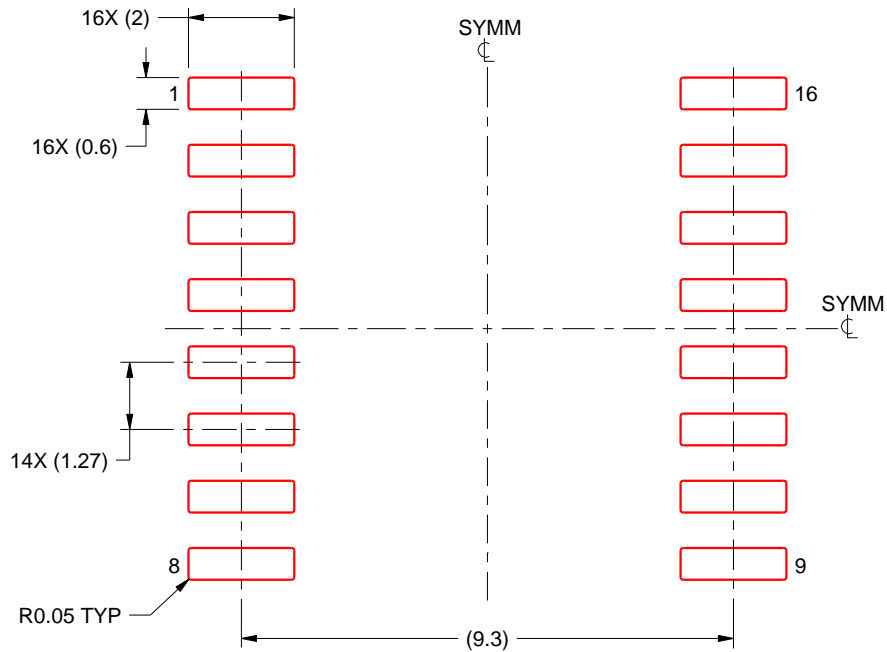
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

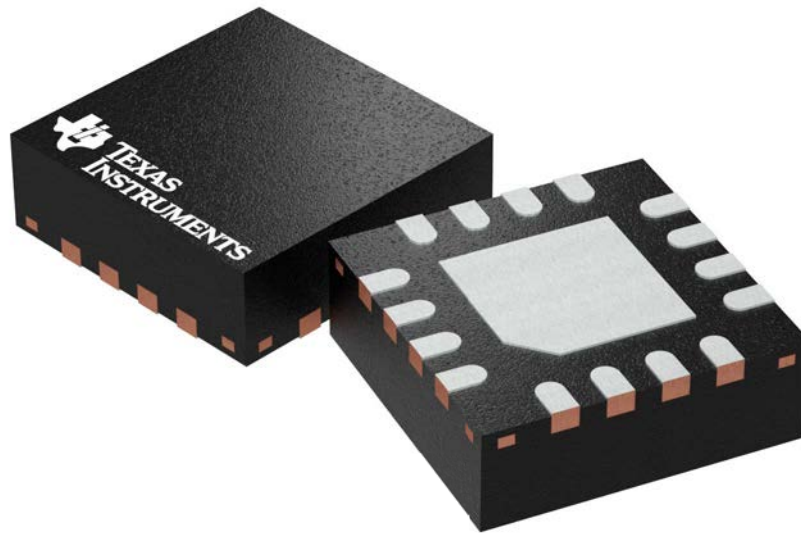
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGT 16

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

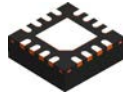
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1

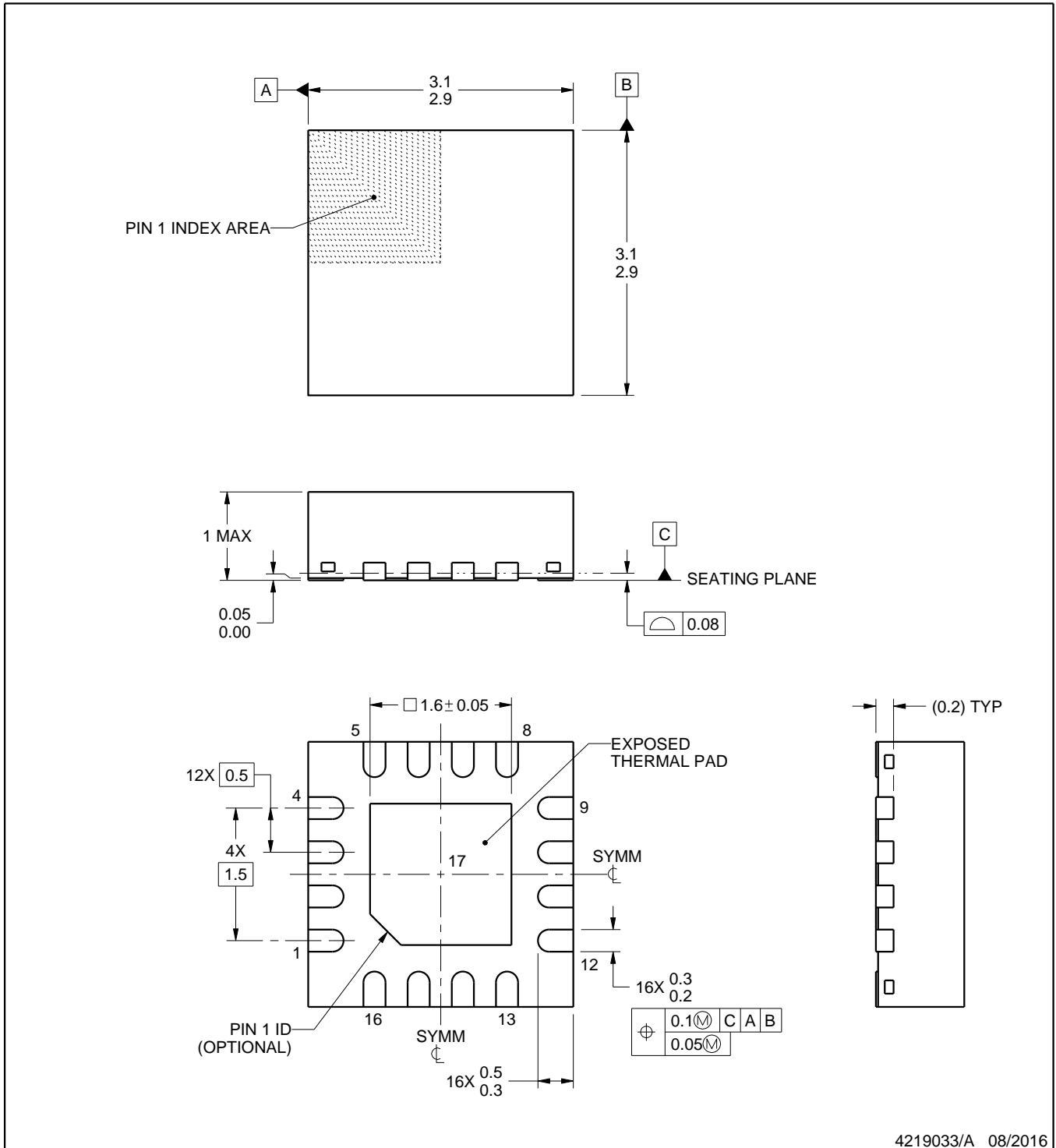
RGT0016B



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

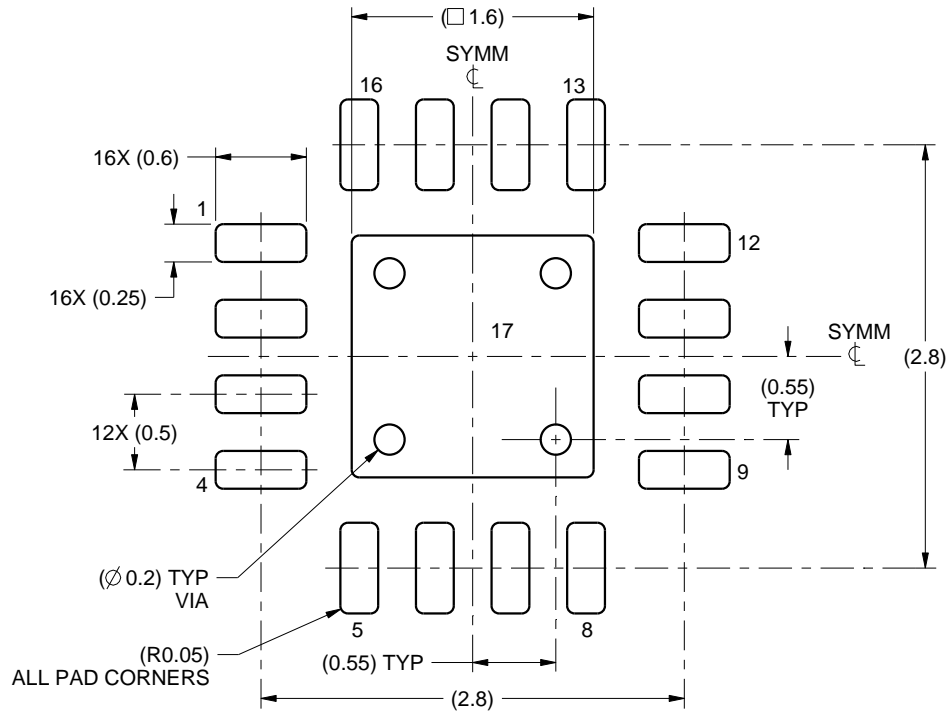
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

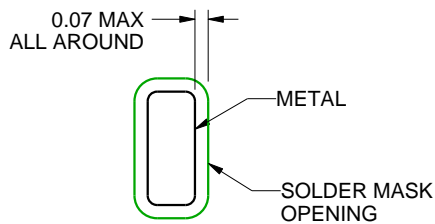
RGT0016B

VQFN - 1 mm max height

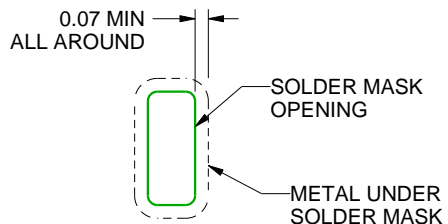
PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4219033/A 08/2016

NOTES: (continued)

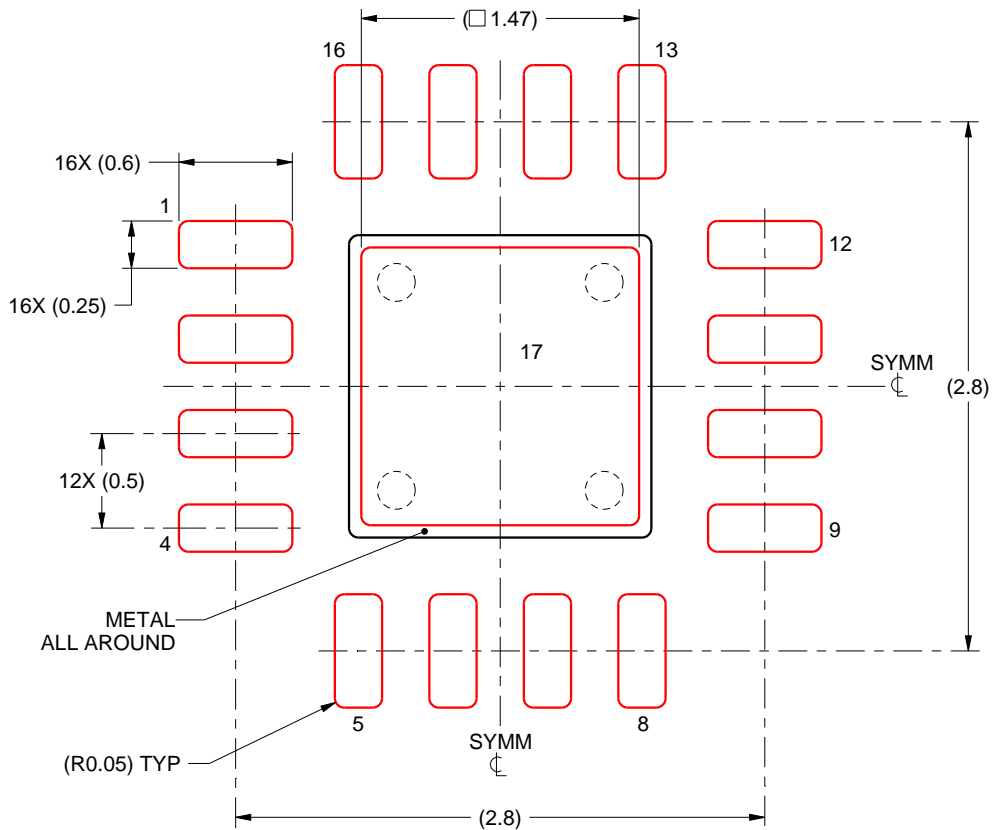
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sl原因271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219033/A 08/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス・デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所 : Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated