

SN54ALS563B, SN74ALS563B OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS163B – DECEMBER 1982 – REVISED NOVEMBER 2004

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

description/ordering information

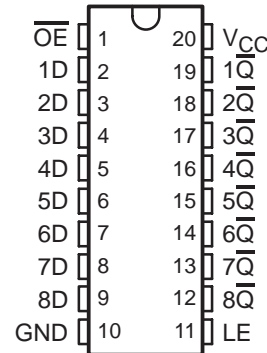
These 8-bit D-type transparent latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the complements of data (D) inputs. When LE is taken low, the outputs are latched at the inverse of the levels set up at the D inputs.

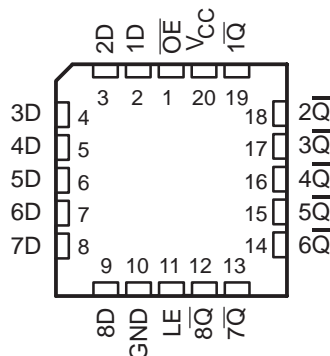
A buffered output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high logic level provide the capability to drive bus lines without interface or pullup components.

\overline{OE} does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54ALS563B . . . J OR W PACKAGE
SN74ALS563B . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS563B . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	SN74ALS563BN	SN74ALS563BN
	SOIC – DW	Tube of 25	SN74ALS563BDW	ALS563B
		Reel of 2000	SN74ALS563BDWR	
	SOP – NS	Reel of 2000	SN74ALS563BNSR	ALS563B
–55°C to 125°C	CDIP – J	Tube of 20	SNJ54ALS563BJ	SNJ54ALS563BJ
	CFP – W	Tube of 85	SNJ54ALS563BW	SNJ54ALS563BW
	LCCC – FK	Tube of 55	SNJ54ALS563BFK	SNJ54ALS563BFK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2004, Texas Instruments Incorporated

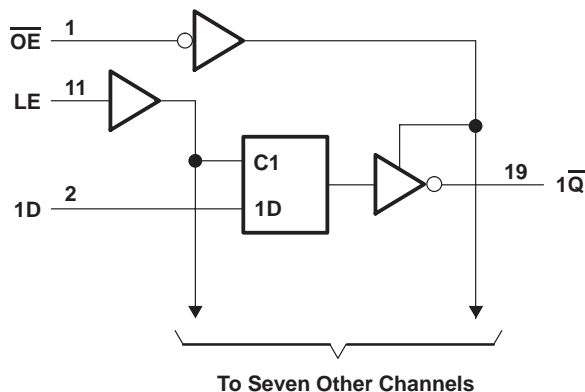
SN54ALS563B, SN74ALS563B OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS163B – DECEMBER 1982 – REVISED NOVEMBER 2004

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	\overline{Q}
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Package thermal impedance, θ_{JA} (see Notes 2):	
DW package	58°C/W
N package	69°C/W
NS package	60°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

SN54ALS563B, SN74ALS563B OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS163B – DECEMBER 1982 – REVISED NOVEMBER 2004

recommended operating conditions (see Note 3)

		SN54ALS563B			SN74ALS563B			UNIT		
		MIN	NOM	MAX	MIN	NOM	MAX			
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V		
V _{IH}	High-level input voltage	2			2			V		
V _{IL}	Low-level input voltage	0.7			0.8			V		
I _{OH}	High-level output current	-1			-2.6			mA		
I _{OL}	Low-level output current	12			24			mA		
t _w	Pulse duration, LE high	15			15			ns		
t _{su}	Setup time, data before LE↓	20			10			ns		
t _h	Hold time, data after LE↓	12			10			ns		
T _A	Operating free-air temperature	-55			125			0	70	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS563B			SN74ALS563B			UNIT	
		MIN	TYP†	MAX	MIN	TYP†	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA	-1.2			-1.2			V	
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -0.4 mA	V _{CC} - 2			V _{CC} - 2			V	
	V _{CC} = 4.5 V	I _{OH} = -1 mA			2.4				3.3
		I _{OH} = -2.6 mA			2.4				
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 12 mA			0.25			0.4	
		I _{OL} = 24 mA			0.35			0.5	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V	20			20			μA	
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V	-20			-20			μA	
I _I	V _{CC} = 5.5 V, V _I = 7 V	0.1			0.1			mA	
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V	20			20			μA	
I _{IL}	V _{CC} = 5.5 V, V _I = 0.4 V	-0.1			-0.1			mA	
I _{O‡}	V _{CC} = 5.5 V, V _O = 2.25 V	-20		-112	-30		-112	mA	
I _{CC}	V _{CC} = 5.5 V	Outputs high			10		17	mA	
		Outputs low			16		26		
		Outputs disabled			17		29		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

SN54ALS563B, SN74ALS563B
OCTAL D-TYPE TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

SDAS163B – DECEMBER 1982 – REVISED NOVEMBER 2004

switching characteristics (see Figure 1)

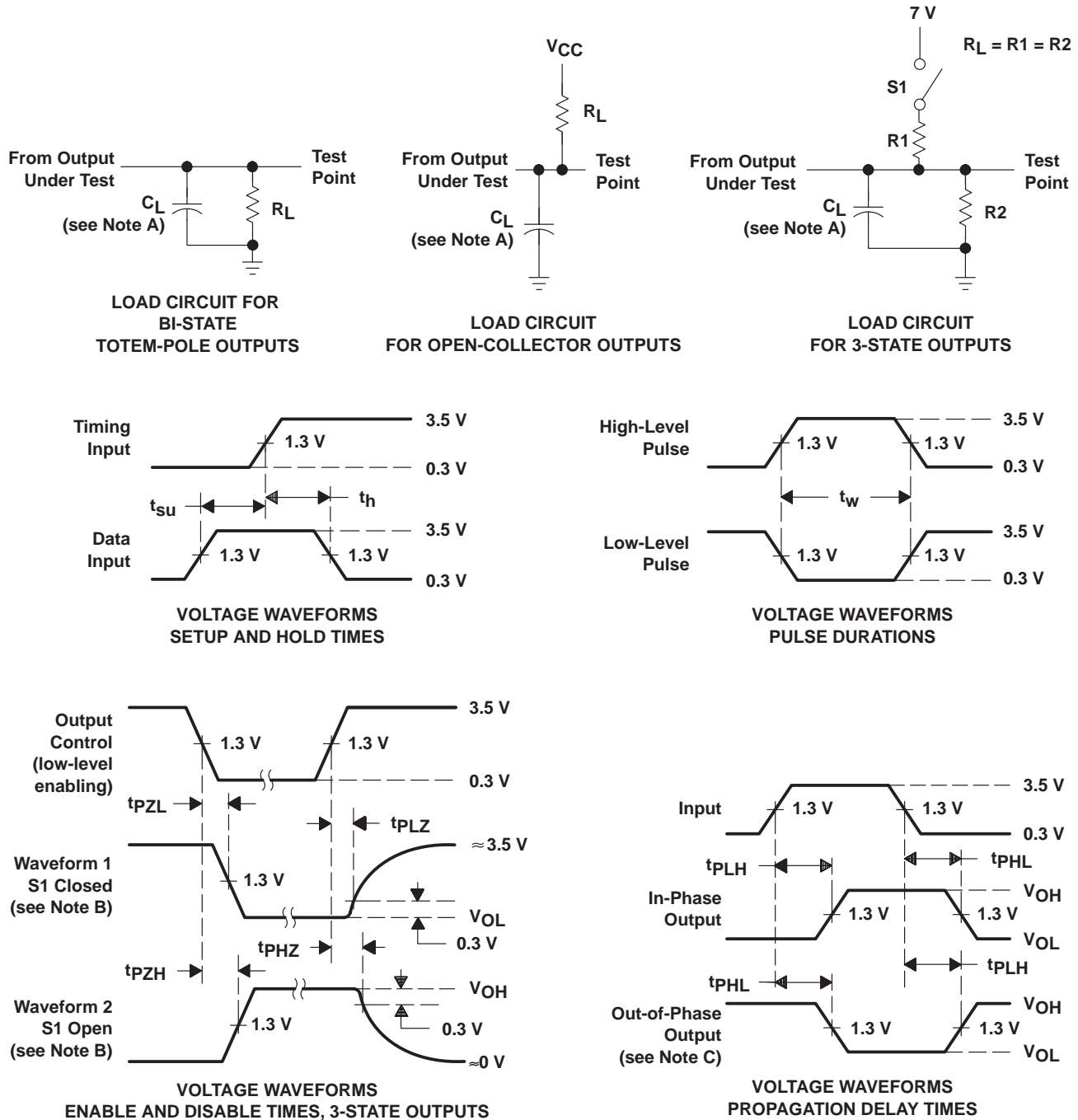
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V C _L = 50 pF R1 = 500 Ω R2 = 500 Ω T _A = MIN to MAX†				UNIT
			SN54ALS563B		SN74ALS563B		
			MIN	MAX	MIN	MAX	
t _{PLH}	D	Q ₁	3	26	3	18	ns
t _{PHL}			3	15	3	14	
t _{PLH}	LE	Q ₁	8	29	6	22	ns
t _{PHL}			4	22	6	21	
t _{PZH}	\overline{OE}	Q ₁	4	25	3	18	ns
t _{PZL}			4	21	4	18	
t _{PHZ}	\overline{OE}	Q ₁	2	12	1	10	ns
t _{PLZ}			3	22	1	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN54ALS563B, SN74ALS563B OCTAL D-TYPE TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

SDAS163B – DECEMBER 1982 – REVISED NOVEMBER 2004

PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1$ MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8870001RA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8870001RA SNJ54ALS563BJ	Samples
SN74ALS563BDW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS563B	Samples
SN74ALS563BN	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74ALS563BN	Samples
SN74ALS563BNSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS563B	Samples
SN74ALS563BNSRG4	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS563B	Samples
SNJ54ALS563BJ	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8870001RA SNJ54ALS563BJ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

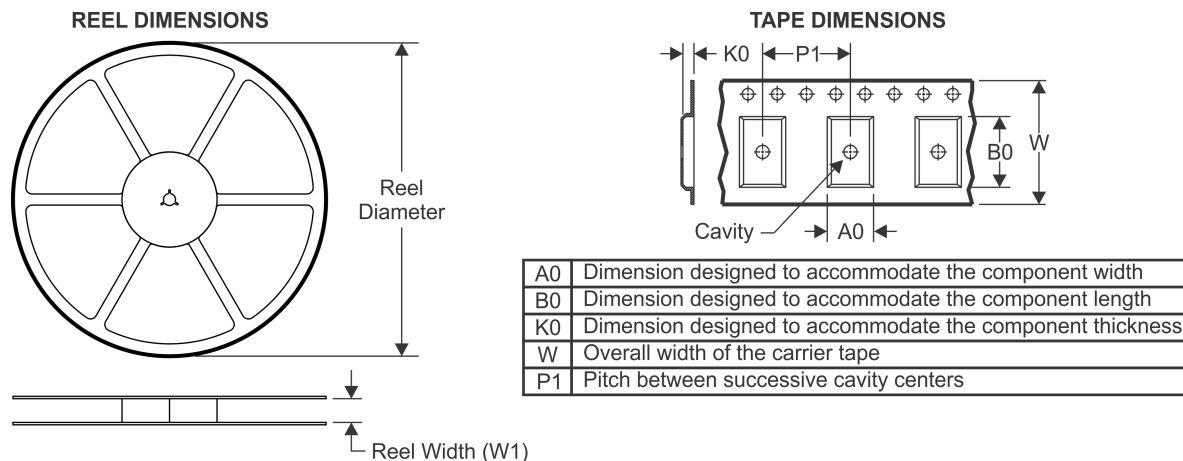
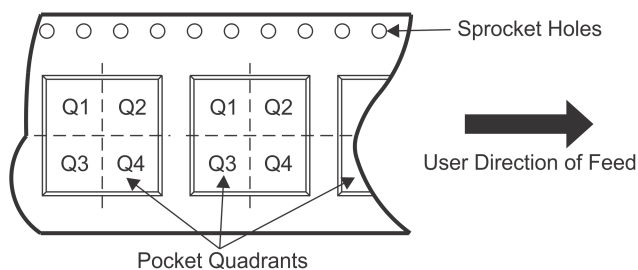
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS563B, SN74ALS563B :

- Catalog : [SN74ALS563B](#)
- Military : [SN54ALS563B](#)

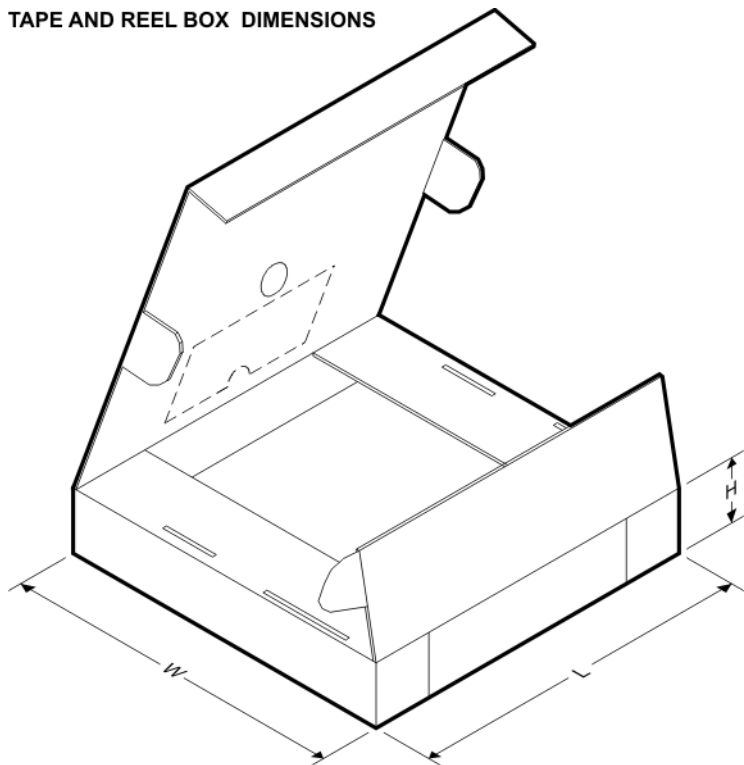
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


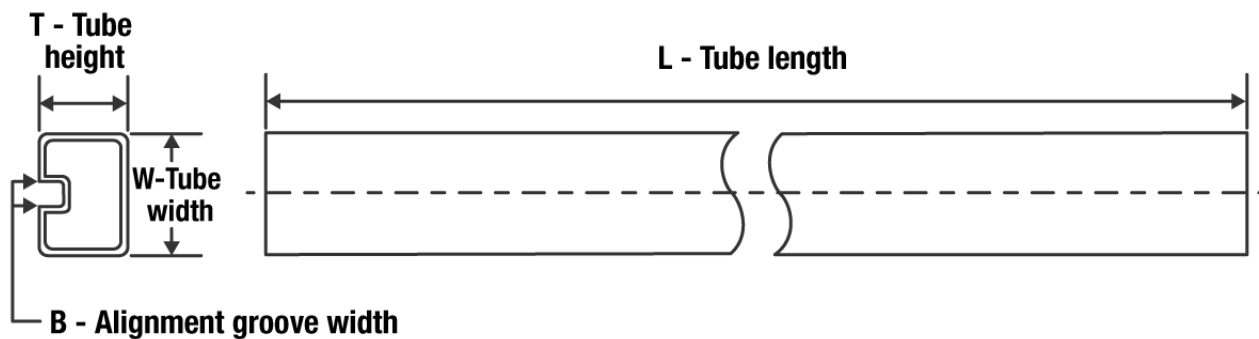
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS563BNSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS563BNSR	SO	NS	20	2000	367.0	367.0	45.0

TUBE


*All dimensions are nominal

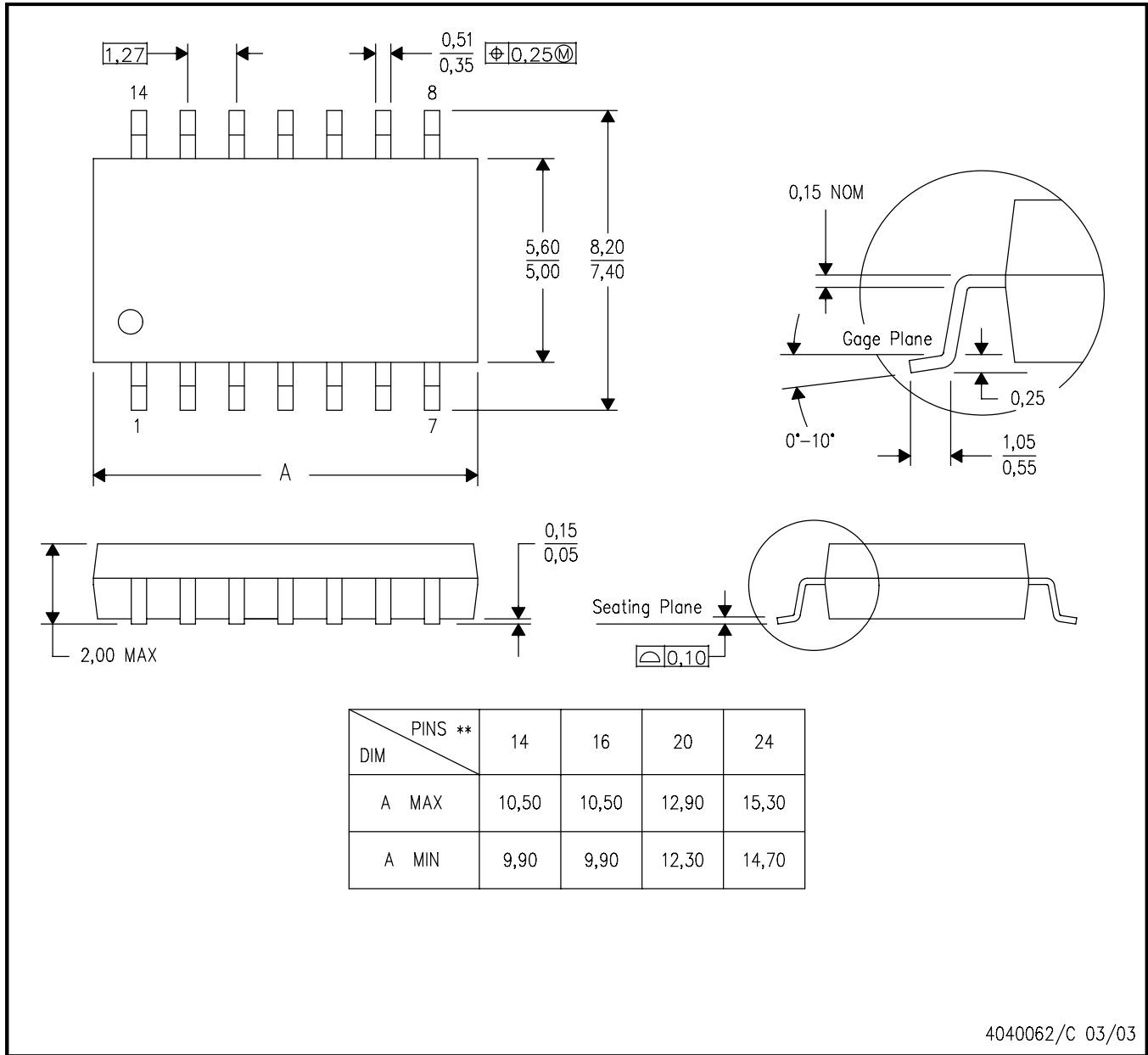
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ALS563BDW	DW	SOIC	20	25	507	12.83	5080	6.6
SN74ALS563BN	N	PDIP	20	20	506	13.97	11230	4.32

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

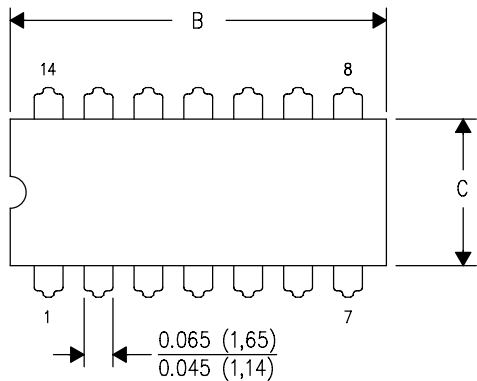


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

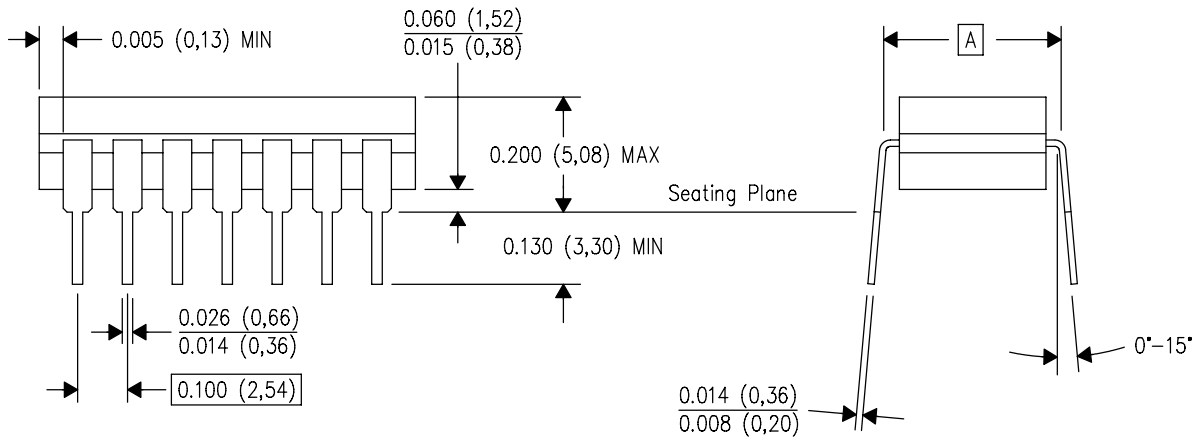
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



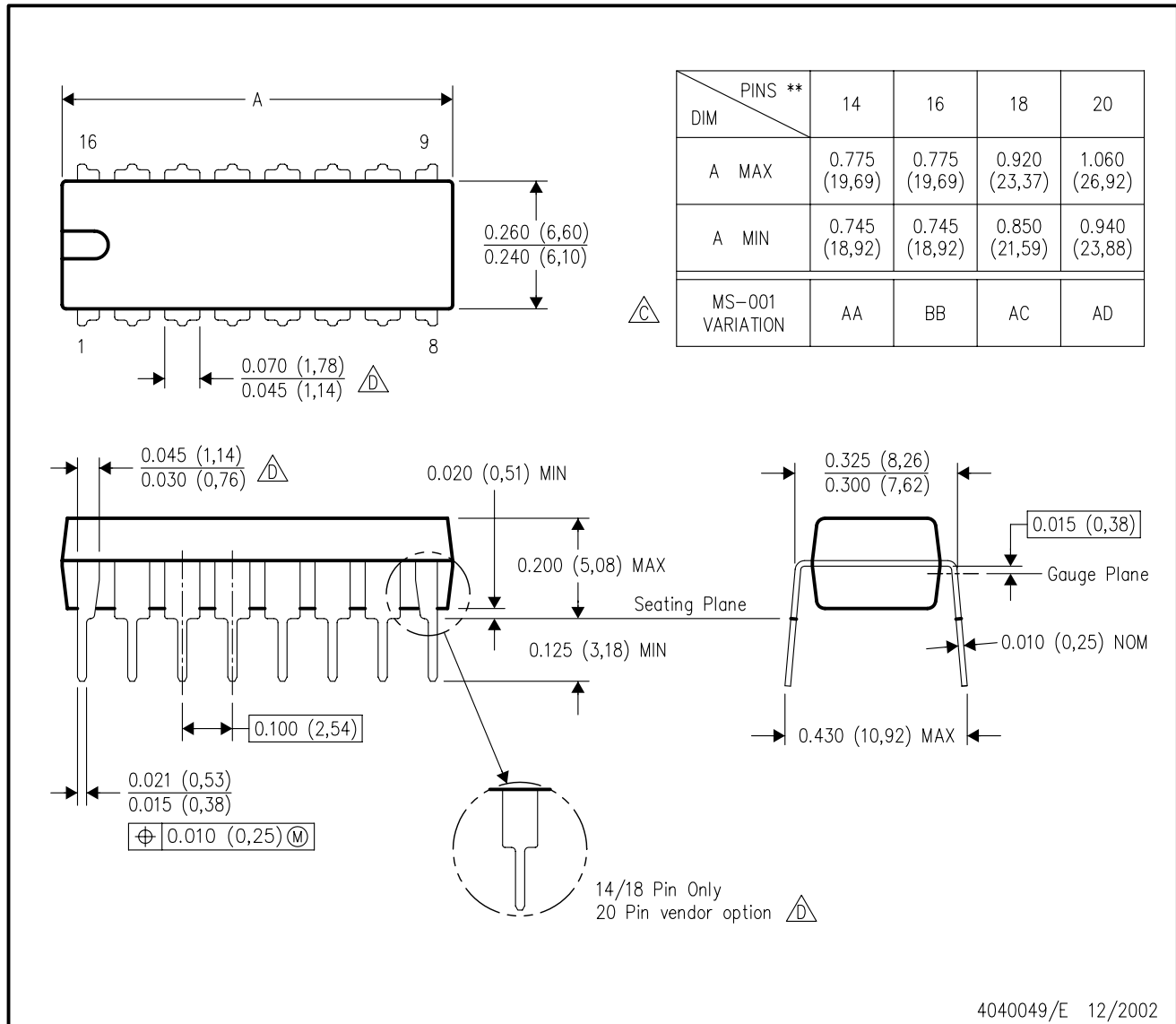
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

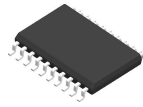
16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

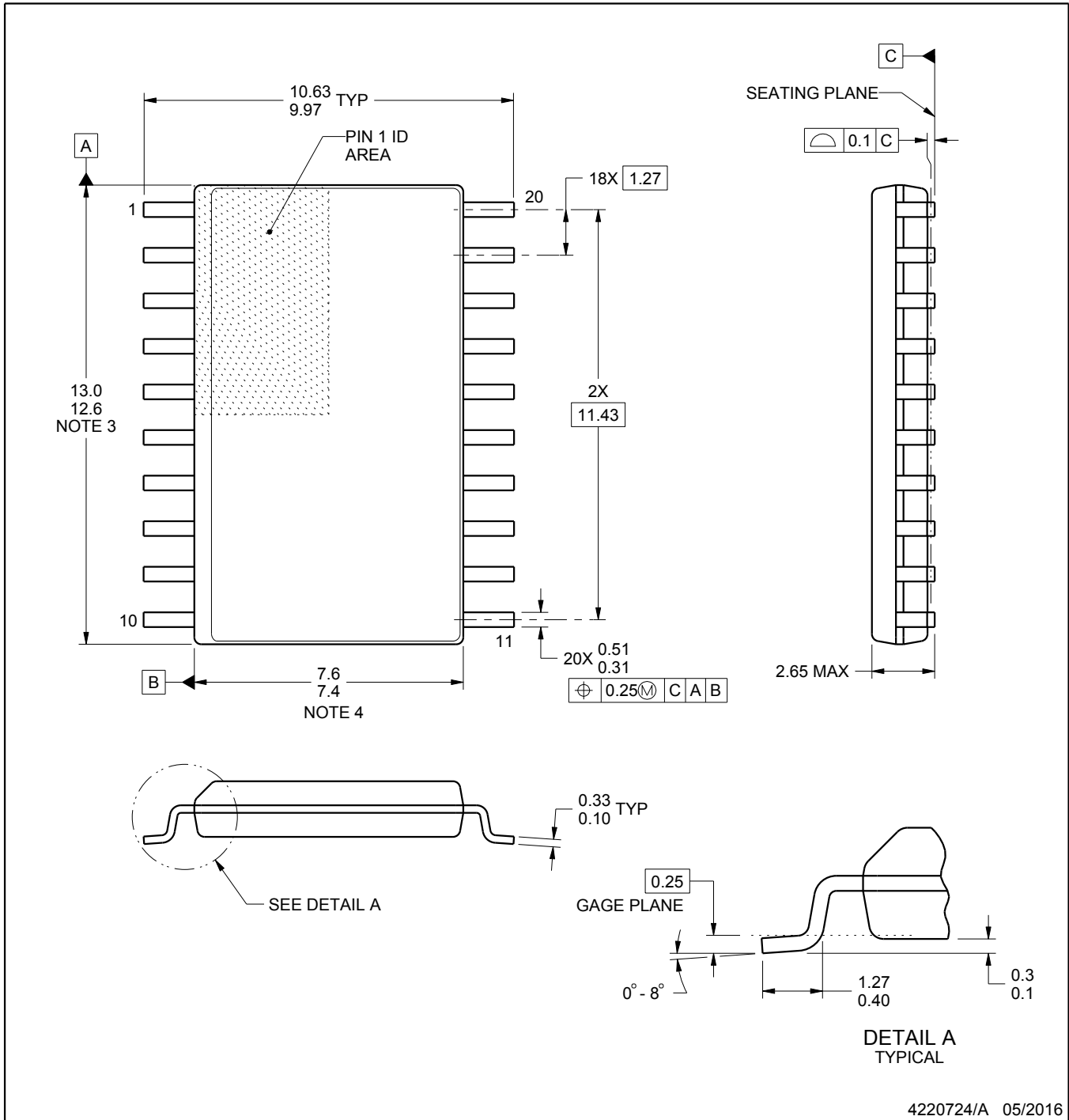
DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

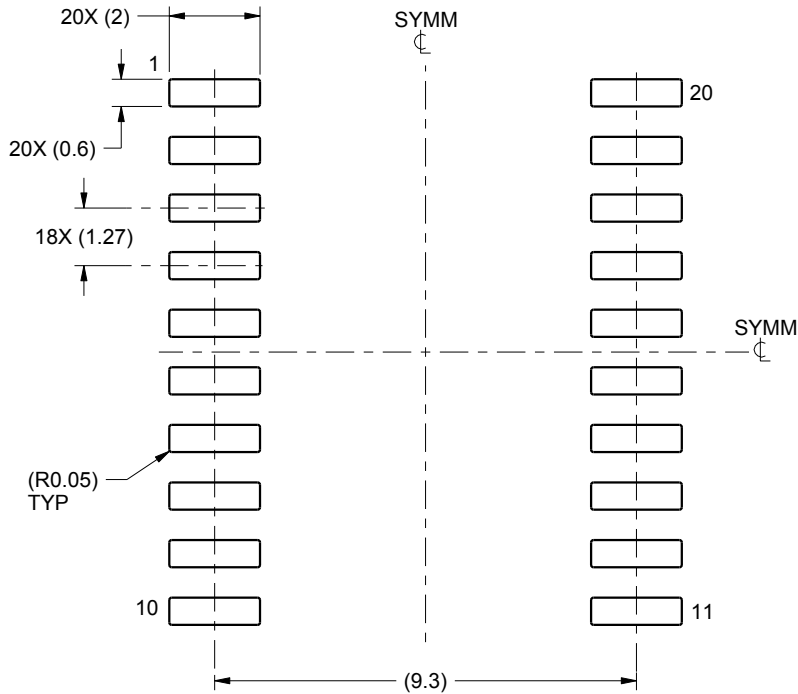
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

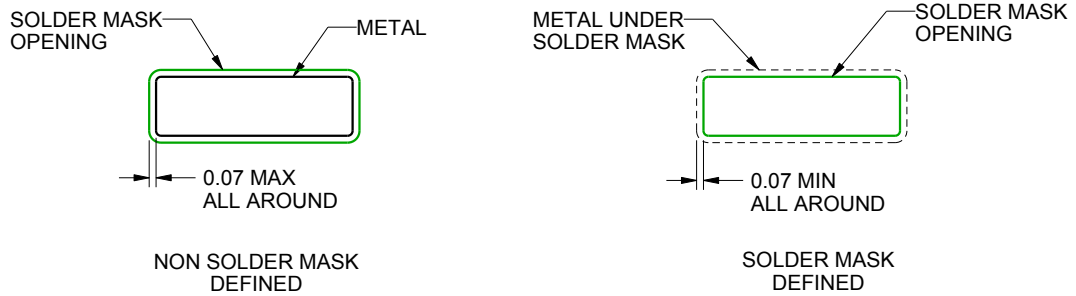
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

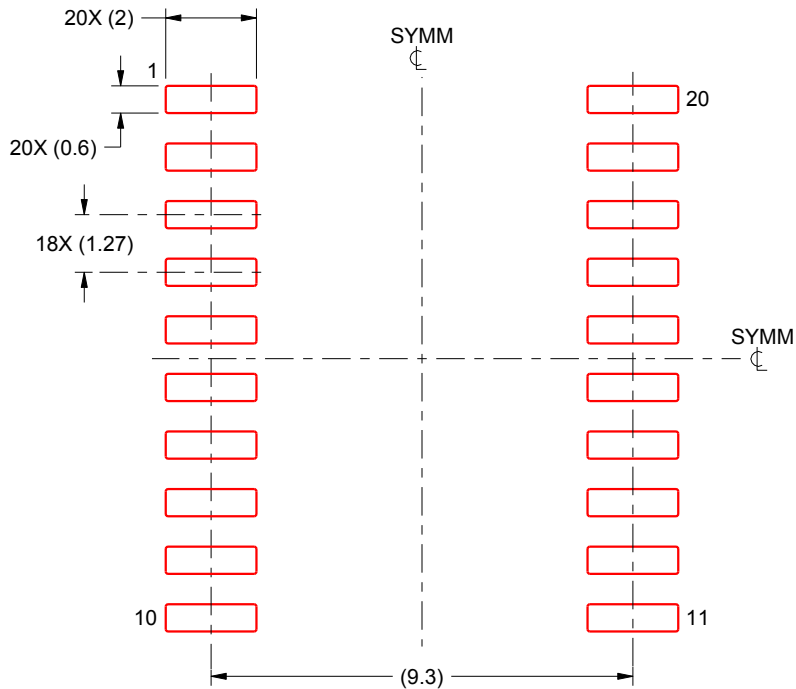
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated