

# TCAN1044AEV-Q1 グレード 0、フォルト保護、1.8V I/O 対応、CAN FD トランシーバ

## 1 特長

- 車載アプリケーション用に AEC-Q100 (グレード 0) 認定済み
- ISO 11898-2:2016 物理層規格の要件に適合
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- Classical CAN のサポートと最適化された CAN FD 性能 (2、5、8Mbps)
  - 短く対称的な伝搬遅延時間によりタイミング・マージンを強化
- I/O 電圧範囲: 1.7V~5.5V
- 12V および 24V バッテリー・アプリケーションに対応
- トランシーバの同相入力電圧:  $\pm 12V$
- 保護機能:
  - バス・フォルト保護:  $\pm 58V$
  - 低電圧保護
  - TXD ドミナント・タイムアウト (DTO)
    - 最小 9.2kbps のデータ・レート
  - サーマル・シャットダウン保護 (TSD)
- 動作モード:
  - 通常モード
  - リモート・ウェイクアップ要求をサポートする、低消費電力スタンバイ・モード
- 電源非接続時の最適化された挙動
  - バスおよびロジック・ピンは高インピーダンス (動作中のバス、アプリケーションに対して無負荷)
  - ホットプラグ対応: 電源オン / オフ時のバスおよび RXD 出力のグリッチ・フリー動作
- 8ピン SOIC および小型フットプリント SOT-23 パッケージ

## 2 アプリケーション

- 自動車および輸送システム
  - 車体制御モジュール
  - 車載ゲートウェイ
  - 先進運転支援システム (ADAS)
  - インフォテインメント

## 3 概要

TCAN1044AEV-Q1 は、ISO 11898-2:2016 High-speed CAN (Controller Area Network) 仕様の物理層要件を満たす High-speed CAN トランシーバです。

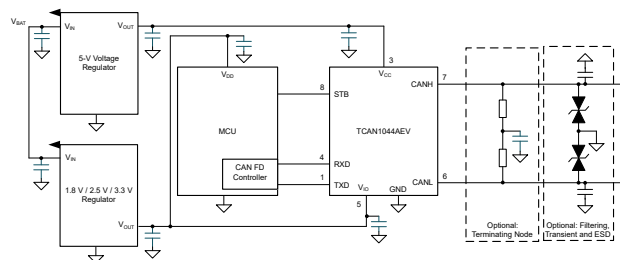
このトランシーバは、電磁両立性 (EMC) 認証済みであり、最高 5 メガビット/秒 (Mbps) の Classical CAN および CAN FD ネットワークに最適です。これらのデバイスを使用すると、シンプルなネットワークで最大 8Mbps の動作を実現できます。本デバイスは  $V_{IO}$  ピンによる内部ロジック・レベル変換機能を備えているため、トランシーバの I/O を 1.8V、2.5V、3.3V、5V のロジック・レベルに直接接続できます。このトランシーバは、低消費電力スタンバイ・モードと、ISO 11898-2:2016 に規定されたウェイクアップ・パターン (WUP) に準拠した「CAN によるウェイク」をサポートしています。

このトランシーバは、サーマル・シャットダウン (TSD)、TXD ドミナント・タイムアウト (DTO)、電源低電圧検出、 $\pm 58V$  バス・フォルト保護も備えています。これらのデバイスには、電源電圧低下またはフローティング・ピン発生時のフェイルセーフ動作が定義されています。

### 製品情報

部品番号	パッケージ <sup>(1)</sup>	本体サイズ (公称)
TCAN1044AEV-Q1	SOIC (D)	4.90mm × 3.91mm
	SOT-23 (DDF)	2.90mm × 1.60mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2021	*	Initial Release

## 5 Pin Configuration and Functions

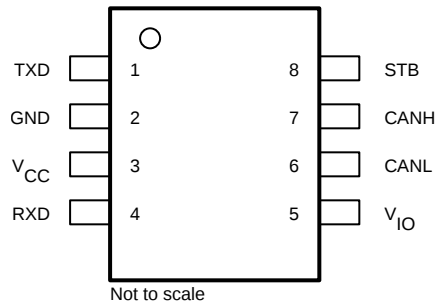


图 5-1. DDF (SOT) and D (SOIC), 8-Pin Package, Top View

表 5-1. Pin Functions

Pins		Type	Description
No.	Name		
1	TXD	Digital Input	CAN transmit data input; integrated pull-up
2	GND	GND	Ground connection
3	V <sub>CC</sub>	Supply	5-V supply voltage
4	RXD	Digital Output	CAN receive data output, tri-stated when device powered off
5	V <sub>IO</sub>	Supply	I/O supply voltage
6	CANL	Bus IO	Low-level CAN bus input/output line
7	CANH	Bus IO	High-level CAN bus input/output line
8	STB	Digital Input	Standby input for mode control; integrated pull-up

## 6 Specifications

### 6.1 Absolute Maximum Ratings

(1) (2)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.3	6	V
V <sub>IO</sub>	Supply voltage I/O level shifter	-0.3	6	V
V <sub>BUS</sub>	CAN Bus I/O voltage	-58	58	V
V <sub>DIFF</sub>	Max differential voltage between CANH and CANL	-45	45	V
V <sub>Logic_Input</sub>	Logic input terminal voltage	-0.3	6	V
V <sub>RXD</sub>	RXD output terminal voltage range	-0.3	6	V
I <sub>O(RXD)</sub>	RXD output current	-8	8	mA
T <sub>J</sub>	Junction temperature	-40	175	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>ESD</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000	V
			HBM classification level 3A for all pins	
			HBM classification level 3B for global pins CANH and CANL with respect to GND	±10000
		Charged-device model (CDM), per AEC Q100-011 CDM classification level C5 for all pins	±750	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 ESD Ratings - IEC Specifications

			VALUE	UNIT	
V <sub>ESD</sub>	System level Electrostatic discharge	CAN bus terminals to GND	Unpowered contact discharge per ISO 10605 <sup>(1)</sup>	±8000	V
			SAE J2962-2 per ISO 10605 Powered Contact Discharge <sup>(2)</sup>	±8000	V
			SAE J2962-2 per ISO 10605 Powered Air Discharge <sup>(2)</sup>	±15000	V
V <sub>Tran</sub>	Transient voltage per ISO 7637-2 <sup>(3)</sup>		Pulse 1	-100	V
			Pulse 2a	75	V
			Pulse 3a	-150	V
			Pulse 3b	100	V
			Transient voltage per ISO 7637-3 <sup>(4)</sup>	DCC slow transient pulse	±30

- (1) Tested according to IEC 62228-3:2019 CAN Transceivers.
- (2) Results given here are specific to the SAE J2962-2 Communication Transceivers Qualification Requirements - CAN. Testing performed by OEM approved independent third party, EMC report available upon request.
- (3) Tested according to IEC 62228-3:2019 CAN Transceivers.
- (4) Tested according to SAE J2962-2.

## 6.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	V
V <sub>IO</sub>	Supply voltage for I/O level shifter	1.7		5.5	V
I <sub>OH(RXD)</sub>	RXD terminal high-level output current	-1.5			mA
I <sub>OL(RXD)</sub>	RXD terminal low-level output current			1.5	mA
T <sub>A</sub>	Operating ambient temperature	-40		150	°C

## 6.5 Thermal Characteristics

THERMAL METRIC <sup>(1)</sup>		TCAN1044AEV-Q1		UNIT
		D (SOIC)	DDF (SOT)	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	127.5	122	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	67.6	63	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	70.9	42.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	19.3	2.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	70.2	42.2	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	--	--	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.6 Supply Characteristics

Over recommended operating conditions with T<sub>A</sub> = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I <sub>CC</sub>	Supply current Normal mode	Dominant	STB = 0 V, TXD = 0 V R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open See <a href="#">7-1</a>		45	70	mA
			STB = 0 V, TXD = 0 V R <sub>L</sub> = 50 Ω, C <sub>L</sub> = open See <a href="#">7-1</a>		49	80	mA
		Recessive	STB = 0 V, TXD = V <sub>CC</sub> or V <sub>IO</sub> R <sub>L</sub> = 50 Ω, C <sub>L</sub> = open See <a href="#">7-1</a>		4.5	7.5	mA
		Dominant with bus fault	STB = 0 V, TXD = 0 V CANH = CANL = ±25 V R <sub>L</sub> = open, C <sub>L</sub> = open See <a href="#">7-1</a>			130	mA
	Supply current Standby mode		STB = TXD = V <sub>IO</sub> R <sub>L</sub> = 50 Ω, C <sub>L</sub> = open See <a href="#">7-1</a>			1.5	μA
I <sub>IO</sub>	I/O supply current Normal mode	Dominant	STB = 0 V, TXD = 0 V RXD floating		125	300	μA
	I/O supply current Normal mode	Recessive	STB = 0 V, TXD = 0 V RXD floating		25	48	μA
	I/O supply current Standby mode		STB = V <sub>IO</sub> , TXD = 0 V RXD floating		8.5	14	μA
UV <sub>CC</sub>	Rising undervoltage detection on V <sub>CC</sub> for protected mode				4.2	4.4	V
	Falling undervoltage detection on V <sub>CC</sub> for protected mode			3.5	4	4.25	V
V <sub>HYS(UVCC)</sub>	Hysteresis voltage on UV <sub>CC</sub>				200		mV
UV <sub>VIO</sub>	Rising undervoltage detection on V <sub>IO</sub>				1.56	1.65	V
	Falling undervoltage detection on V <sub>IO</sub>			1.4	1.51	1.59	V
V <sub>HYS(UVIO)</sub>	Hysteresis voltage on UV <sub>IO</sub>				40		mV

## 6.7 Dissipation Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P <sub>D</sub>	Average power dissipation Normal mode	V <sub>CC</sub> = 5 V, V <sub>IO</sub> = 1.8 V, T <sub>J</sub> = 27°C, R <sub>L</sub> = 60 Ω, C <sub>L_RXD</sub> = 15 pF TXD input = 250 kHz 50% duty cycle square wave		95		mW
		V <sub>CC</sub> = 5 V, V <sub>IO</sub> = 3.3 V, T <sub>J</sub> = 27°C, R <sub>L</sub> = 60 Ω, C <sub>L_RXD</sub> = 15 pF TXD input = 250 kHz 50% duty cycle square wave		95		mW
		V <sub>CC</sub> = 5 V, V <sub>IO</sub> = 5 V, T <sub>J</sub> = 27°C, R <sub>L</sub> = 60 Ω, C <sub>L_RXD</sub> = 15 pF TXD input = 250 kHz 50% duty cycle square wave		95		mW
		V <sub>CC</sub> = 5.5 V, V <sub>IO</sub> = 1.8 V, T <sub>J</sub> = 150°C, R <sub>L</sub> = 60 Ω, C <sub>L_RXD</sub> = 15 pF TXD input = 2.5 MHz 50% duty cycle square wave		120		mW
		V <sub>CC</sub> = 5.5 V, V <sub>IO</sub> = 3.3 V, T <sub>J</sub> = 150°C, R <sub>L</sub> = 60 Ω, C <sub>L_RXD</sub> = 15 pF TXD input = 2.5 MHz 50% duty cycle square wave		120		mW
		V <sub>CC</sub> = 5.5 V, V <sub>IO</sub> = 5 V, T <sub>J</sub> = 150°C, R <sub>L</sub> = 60 Ω, C <sub>L_RXD</sub> = 15 pF TXD input = 2.5 MHz 50% duty cycle square wave		120		mW
T <sub>TSD</sub>	Thermal shutdown temperature		175	195	210	°C
T <sub>TSD(HYS)</sub>	Thermal shutdown hysteresis			12		

## 6.8 Electrical Characteristics

Over recommended operating conditions with T<sub>A</sub> = -40°C to 150°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT		
<b>Driver Electrical Characteristics</b>								
V <sub>O(DOM)</sub>	Dominant output voltage Normal mode	CANH	STB = 0 V, TXD = 0 V 50 Ω ≤ R <sub>L</sub> ≤ 65 Ω, C <sub>L</sub> = open, R <sub>CM</sub> = open See <a href="#">7-2</a> and <a href="#">8-3</a>		2.75	4.5	V	
		CANL			0.5	2.25	V	
V <sub>O(REC)</sub>	Recessive output voltage Normal mode	CANH and CANL	STB = 0 V, TXD = V <sub>IO</sub> R <sub>L</sub> = open (no load), R <sub>CM</sub> = open See <a href="#">7-2</a> and <a href="#">8-3</a>		2	0.5 V <sub>CC</sub>	3	V
V <sub>SYM</sub>	Driver symmetry (V <sub>O(CANH)</sub> + V <sub>O(CANL)</sub> )/V <sub>CC</sub>		STB = 0 V, TXD = 250 kHz, 1 MHz, 2.5 MHz R <sub>L</sub> = 60 Ω, C <sub>SPLIT</sub> = 4.7 nF, C <sub>L</sub> = open, R <sub>CM</sub> = open See <a href="#">7-2</a> and <a href="#">9-2</a>		0.9		1.1	V/V
V <sub>SYM_DC</sub>	DC output symmetry (V <sub>CC</sub> - V <sub>O(CANH)</sub> - V <sub>O(CANL)</sub> )		STB = 0 V R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open See <a href="#">7-2</a> and <a href="#">8-3</a>		-400		400	mV
V <sub>OD(DOM)</sub>	Differential output voltage Normal mode Dominant	CANH - CANL	STB = 0 V, TXD = 0 V 50 Ω ≤ R <sub>L</sub> ≤ 65 Ω, C <sub>L</sub> = open See <a href="#">7-2</a> and <a href="#">8-3</a>		1.5		3	V
			STB = 0 V, TXD = 0 V 45 Ω ≤ R <sub>L</sub> ≤ 70 Ω, C <sub>L</sub> = open See <a href="#">7-2</a> and <a href="#">8-3</a>		1.4		3.3	V
			STB = 0 V, TXD = 0 V R <sub>L</sub> = 2240 Ω, C <sub>L</sub> = open See <a href="#">7-2</a> and <a href="#">8-3</a>		1.5		5	V
V <sub>OD(REC)</sub>	Differential output voltage Normal mode Recessive	CANH - CANL	STB = 0 V, TXD = V <sub>IO</sub> R <sub>L</sub> = 60 Ω, C <sub>L</sub> = open See <a href="#">7-2</a> and <a href="#">8-3</a>		-120		12	mV
			STB = 0 V, TXD = V <sub>IO</sub> R <sub>L</sub> = open, C <sub>L</sub> = open See <a href="#">7-2</a> and <a href="#">8-3</a>		-50		50	mV

## 6.8 Electrical Characteristics (continued)

Over recommended operating conditions with  $T_A = -40^{\circ}\text{C}$  to  $150^{\circ}\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$V_{O(STB)}$	Bus output voltage Standby mode	CANH	STB = $V_{IO}$ $R_L = \text{open}$ See <a href="#">7-2</a> and <a href="#">8-3</a>	-0.1		0.1	V
		CANL		-0.1		0.1	V
		CANH - CANL		-0.2		0.2	V
$I_{OS(SS\_DOM)}$	Short-circuit steady-state output current, dominant Normal mode	STB = 0 V, TXD = 0 V $V_{(CANH)} = -15\text{ V to }40\text{ V}$ , CANL = open See <a href="#">7-7</a> and <a href="#">8-3</a>	-115			mA	
		STB = 0 V, TXD = 0 V $V_{(CANL)} = -15\text{ V to }40\text{ V}$ , CANH = open See <a href="#">7-7</a> and <a href="#">8-3</a>			115	mA	
$I_{OS(SS\_REC)}$	Short-circuit steady-state output current, recessive Normal mode	STB = 0 V, TXD = $V_{IO}$ $-27\text{ V} \leq V_{BUS} \leq 32\text{ V}$ , where $V_{BUS} = \text{CANH} = \text{CANL}$ See <a href="#">7-7</a> and <a href="#">8-3</a>	-5		5	mA	
<b>Receiver Electrical Characteristics</b>							
$V_{IT}$	Input threshold voltage Normal mode	STB = 0 V $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ See <a href="#">7-3</a> and <a href="#">8-5</a>	500		900	mV	
$V_{IT(STB)}$	Input threshold Standby mode	STB = $V_{IO}$ $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ See <a href="#">7-3</a> and <a href="#">8-5</a>	400		1150	mV	
$V_{DOM}$	Dominant state differential input voltage range Normal mode	STB = 0 V $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ See <a href="#">7-3</a> and <a href="#">8-5</a>	0.9		9	V	
$V_{REC}$	Recessive state differential input voltage range Normal mode	STB = 0 V $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ See <a href="#">7-3</a> and <a href="#">8-5</a>	-4		0.5	V	
$V_{DOM(STB)}$	Dominant state differential input voltage range Standby mode	STB = $V_{IO}$ $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ See <a href="#">7-3</a> and <a href="#">8-5</a>	1.15		9	V	
$V_{REC(STB)}$	Recessive state differential input voltage range Standby mode	STB = $V_{IO}$ $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ See <a href="#">7-3</a> and <a href="#">8-5</a>	-4		0.4	V	
$V_{HYS}$	Hysteresis voltage for input threshold Normal mode	STB = 0 V $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$ See <a href="#">7-3</a> and <a href="#">8-5</a>		115		mV	
$V_{CM}$	Common-mode range Normal and standby modes	See <a href="#">7-3</a> and <a href="#">8-5</a>	-12		12	V	
$I_{LKG(OFF)}$	Unpowered bus input leakage current	CANH = CANL = 5 V, $V_{CC} = V_{IO} = \text{GND}$			5	$\mu\text{A}$	
$C_I$	Input capacitance to ground (CANH or CANL)	TXD = $V_{IO}$			20	pF	
$C_{ID}$	Differential input capacitance				10	pF	
$R_{ID}$	Differential input resistance	STB = 0 V, TXD = $V_{IO}$ $-12\text{ V} \leq V_{CM} \leq 12\text{ V}$	40		90	k $\Omega$	
$R_{IN}$	Single-ended input resistance (CANH or CANL)		20		45	k $\Omega$	
$R_{IN(M)}$	Input resistance matching $[1 - (R_{IN(CANH)} / R_{IN(CANL)})] \times 100\%$	$V_{(CAN\_H)} = V_{(CAN\_L)} = 5\text{ V}$	-1		1	%	
<b>TXD Terminal (CAN Transmit Data Input)</b>							
$V_{IH}$	High-level input voltage		0.7 $V_{IO}$			V	
$V_{IL}$	Low-level input voltage				0.3 $V_{IO}$	V	
$I_{IH}$	High-level input leakage current	TXD = $V_{CC} = V_{IO} = 5.5\text{ V}$	-2.5	0	1	$\mu\text{A}$	
$I_{IL}$	Low-level input leakage current	TXD = 0 V $V_{CC} = V_{IO} = 5.5\text{ V}$	-200	-100	-20	$\mu\text{A}$	
$I_{LKG(OFF)}$	Unpowered leakage current	TXD = 5.5 V $V_{CC} = V_{IO} = 0\text{ V}$	-1	0	1	$\mu\text{A}$	
$C_I$	Input capacitance	$V_{IN} = 0.4 \times \sin(2 \times \pi \times 2 \times 10^6 \times t) + 2.5\text{ V}$		5		pF	
<b>RXD Terminal (CAN Receive Data Output)</b>							
$V_{OH}$	High-level output voltage	$I_O = -1.5\text{ mA}$ See <a href="#">7-3</a>	0.8 $V_{IO}$			V	

## 6.8 Electrical Characteristics (continued)

Over recommended operating conditions with  $T_A = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL}$	Low-level output voltage	$I_O = 1.5\text{mA}$ See <a href="#">7-3</a>			$0.2 V_{IO}$	V
$I_{LKG(OFF)}$	Unpowered leakage current	$RXD = 5.5\text{V}$ $V_{CC} = V_{IO} = 0\text{V}$	-1	0	1	$\mu\text{A}$
<b>STB Terminal (Standby Mode Input)</b>						
$V_{IH}$	High-level input voltage		$0.7 V_{IO}$			V
$V_{IL}$	Low-level input voltage				$0.3 V_{IO}$	V
$I_{IH}$	High-level input leakage current	$V_{CC} = V_{IO} = \text{STB} = 5.5\text{V}$	-2		2	$\mu\text{A}$
$I_{IL}$	Low-level input leakage current	$\text{STB} = 0\text{V}$ $V_{CC} = V_{IO} = 5.5\text{V}$ ,	-20		-2	$\mu\text{A}$
$I_{LKG(OFF)}$	Unpowered leakage current	$\text{STB} = 5.5\text{V}$ $V_{CC} = V_{IO} = 0\text{V}$	-1	0	1	$\mu\text{A}$

## 6.9 Switching Characteristics

Over recommended operating conditions with  $T_A = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Device Switching Characteristics</b>						
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	$\text{STB} = 0\text{V}$ , $V_{IO} = 2.8\text{V}$ to $5.5\text{V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{pF}$ , $C_{L(RXD)} = 15\text{pF}$ See <a href="#">7-4</a>		125	210	ns
$t_{PROP(LOOP1)}$	Total loop delay Driver input (TXD) to receiver output (RXD), recessive to dominant	$\text{STB} = 0\text{V}$ , $V_{IO} = 1.7\text{V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{pF}$ , $C_{L(RXD)} = 15\text{pF}$ See <a href="#">7-4</a>		165	255	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	$\text{STB} = 0\text{V}$ , $V_{IO} = 2.8\text{V}$ to $5.5\text{V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{pF}$ , $C_{L(RXD)} = 15\text{pF}$ See <a href="#">7-4</a>		150	210	ns
$t_{PROP(LOOP2)}$	Total loop delay Driver input (TXD) to receiver output (RXD), dominant to recessive	$\text{STB} = 0\text{V}$ , $V_{IO} = 1.7\text{V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{pF}$ , $C_{L(RXD)} = 15\text{pF}$ See <a href="#">7-4</a>		180	255	ns
$t_{MODE}$	Mode change time, from normal to standby or from standby to normal	See <a href="#">7-5</a>			20	$\mu\text{s}$
$t_{WK\_FILTER}$	Filter time for a valid wake-up pattern	See <a href="#">8-5</a>	0.5		1.8	$\mu\text{s}$
$t_{WK\_TIMEOUT}$	Bus wake-up timeout		0.8		6	ms
<b>Driver Switching Characteristics</b>						
$t_{pHR}$	Propagation delay time, high TXD to driver recessive (dominant to recessive)			80		ns
$t_{pLD}$	Propagation delay time, low TXD to driver dominant (recessive to dominant)	$\text{STB} = 0\text{V}$ $R_L = 60\ \Omega$ , $C_L = 100\text{pF}$ See <a href="#">7-2</a>		70		ns
$t_{sk(p)}$	Pulse skew ( $ t_{pHR} - t_{pLD} $ )			14		ns
$t_R$	Differential output signal rise time			28		ns
$t_F$	Differential output signal fall time			50		ns
$t_{TXD\_DTO}$	Dominant timeout	See <a href="#">7-6</a>	1.2		4.0	ms
<b>Receiver Switching Characteristics</b>						
$t_{pRH}$	Propagation delay time, bus recessive input to high output (dominant to recessive)			81		ns
$t_{pDL}$	Propagation delay time, bus dominant input to low output (recessive to dominant)	$\text{STB} = 0\text{V}$ $C_{L(RXD)} = 15\text{pF}$ See <a href="#">7-3</a>		66		ns
$t_R$	RXD output signal rise time			10		ns
$t_F$	RXD output signal fall time			10		ns
<b>FD Timing Characteristics</b>						



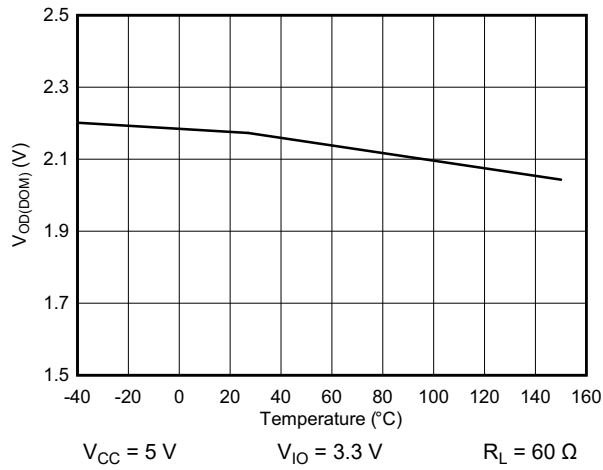
## 6.9 Switching Characteristics (continued)

Over recommended operating conditions with  $T_A = -40^\circ\text{C}$  to  $150^\circ\text{C}$  (unless otherwise noted).

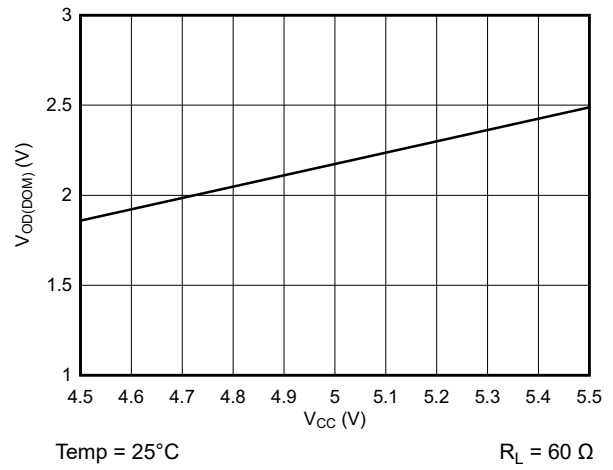
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{\text{BIT(BUS)}}$	Bit time on CAN bus output pins $t_{\text{BIT(TXD)}} = 500 \text{ ns}$	STB = 0 V $R_L = 60 \Omega$ , $C_L = 100 \text{ pF}$ , $C_{L(\text{RXD})} = 15 \text{ pF}$ $\Delta t_{\text{REC}} = t_{\text{BIT(RXD)}} - t_{\text{BIT(BUS)}}$ See <a href="#">Fig 7-4</a>	450		525	ns
	Bit time on CAN bus output pins $t_{\text{BIT(TXD)}} = 200 \text{ ns}$		160		205	ns
	Bit time on CAN bus output pins $t_{\text{BIT(TXD)}} = 125 \text{ ns}^{(1)}$		85		130	ns
$t_{\text{BIT(RXD)}}$	Bit time on RXD output pins $t_{\text{BIT(TXD)}} = 500 \text{ ns}$		410		540	ns
	Bit time on RXD output pins $t_{\text{BIT(TXD)}} = 200 \text{ ns}$		130		210	ns
	Bit time on RXD output pins $t_{\text{BIT(TXD)}} = 125 \text{ ns}^{(1)}$		75		135	ns
$\Delta t_{\text{REC}}$	Receiver timing symmetry $t_{\text{BIT(TXD)}} = 500 \text{ ns}$		-50		20	ns
	Receiver timing symmetry $t_{\text{BIT(TXD)}} = 200 \text{ ns}$		-40		10	ns
	Receiver timing symmetry $t_{\text{BIT(TXD)}} = 125 \text{ ns}^{(1)}$		-40		10	ns

(1) Measured during characterization and not an ISO 11898-2:2016 parameter.

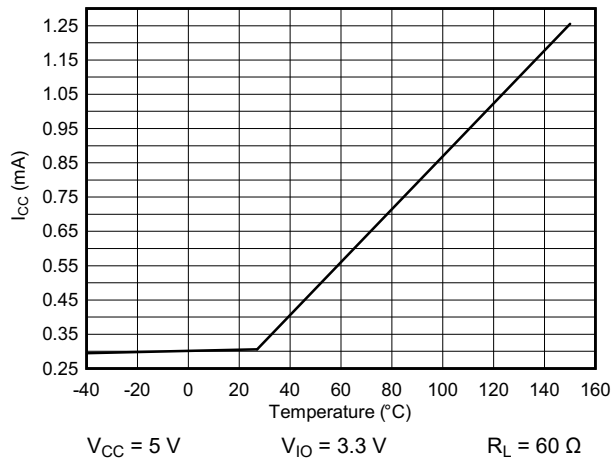
## 6.10 Typical Characteristics



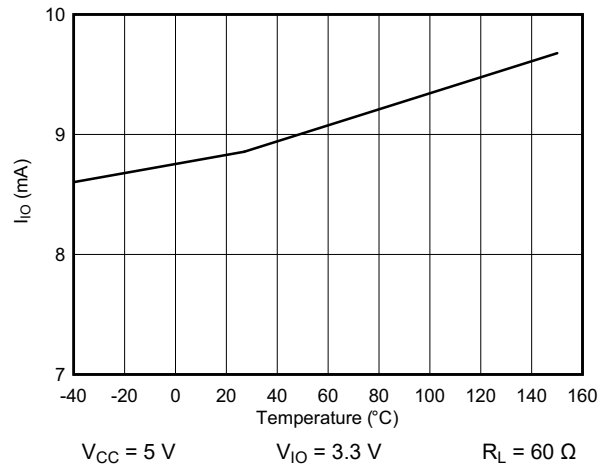
6-1.  $V_{OD(DOM)}$  vs Temperature



6-2.  $V_{OD(DOM)}$  vs  $V_{CC}$

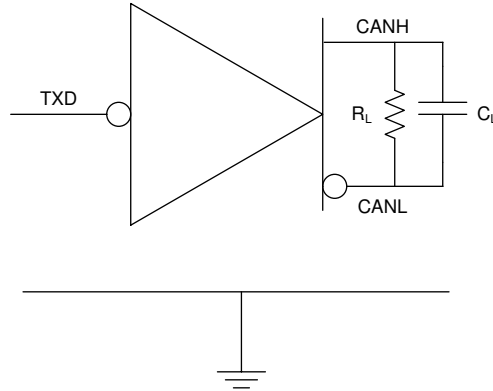


6-3.  $I_{CC}$  Standby vs Temperature

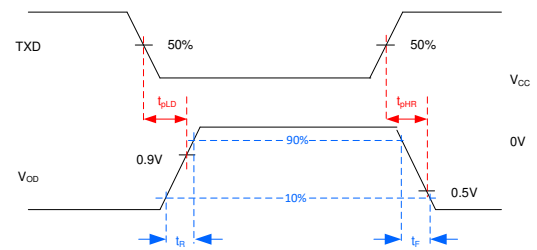
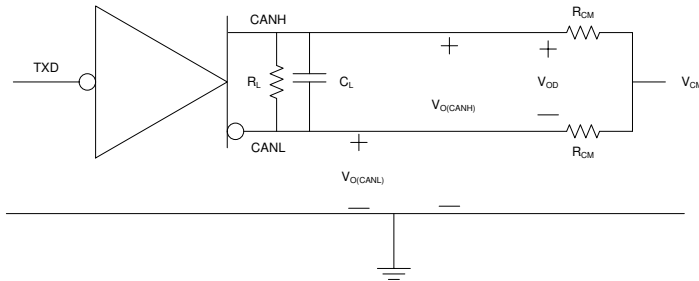


6-4.  $I_{IO}$  Standby vs Temperature

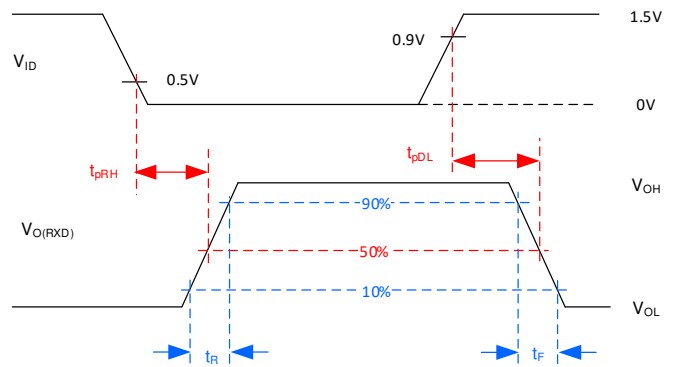
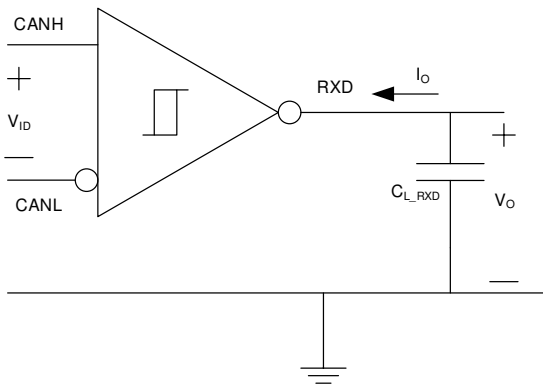
## 7 Parameter Measurement Information



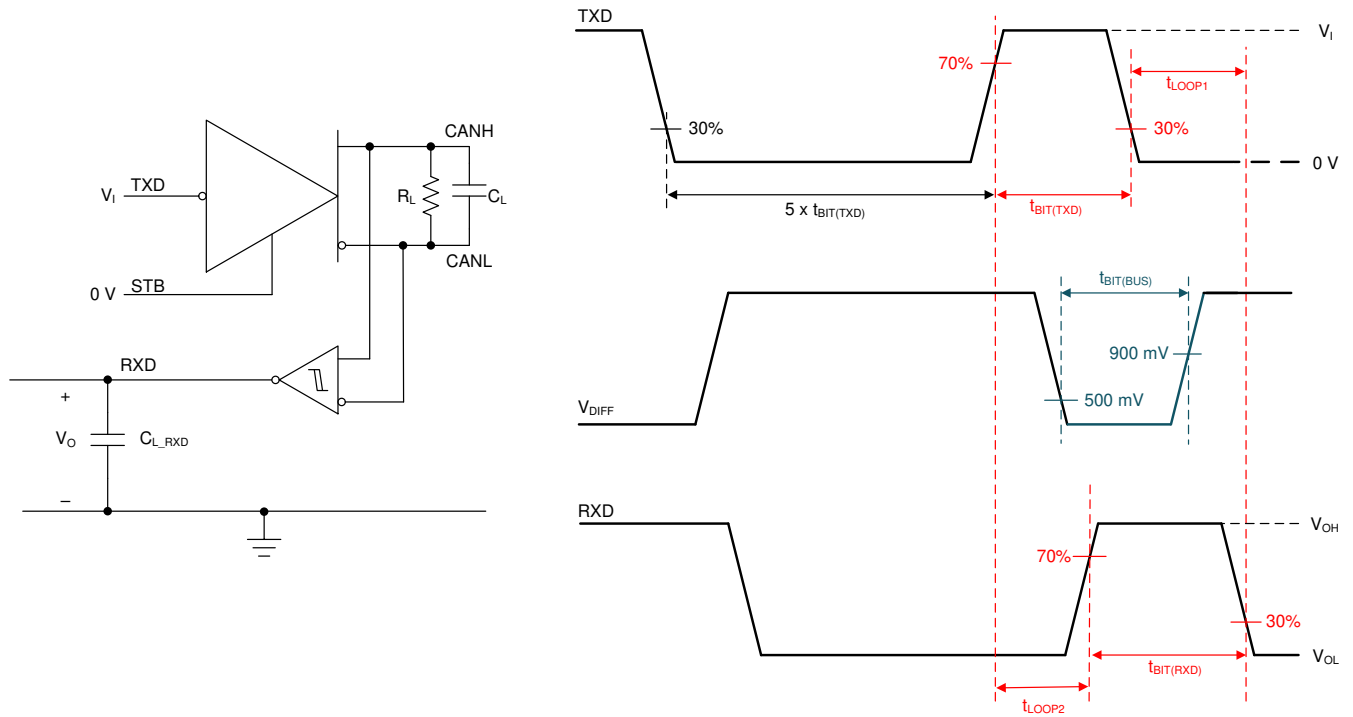
7-1.  $I_{CC}$  Test Circuit



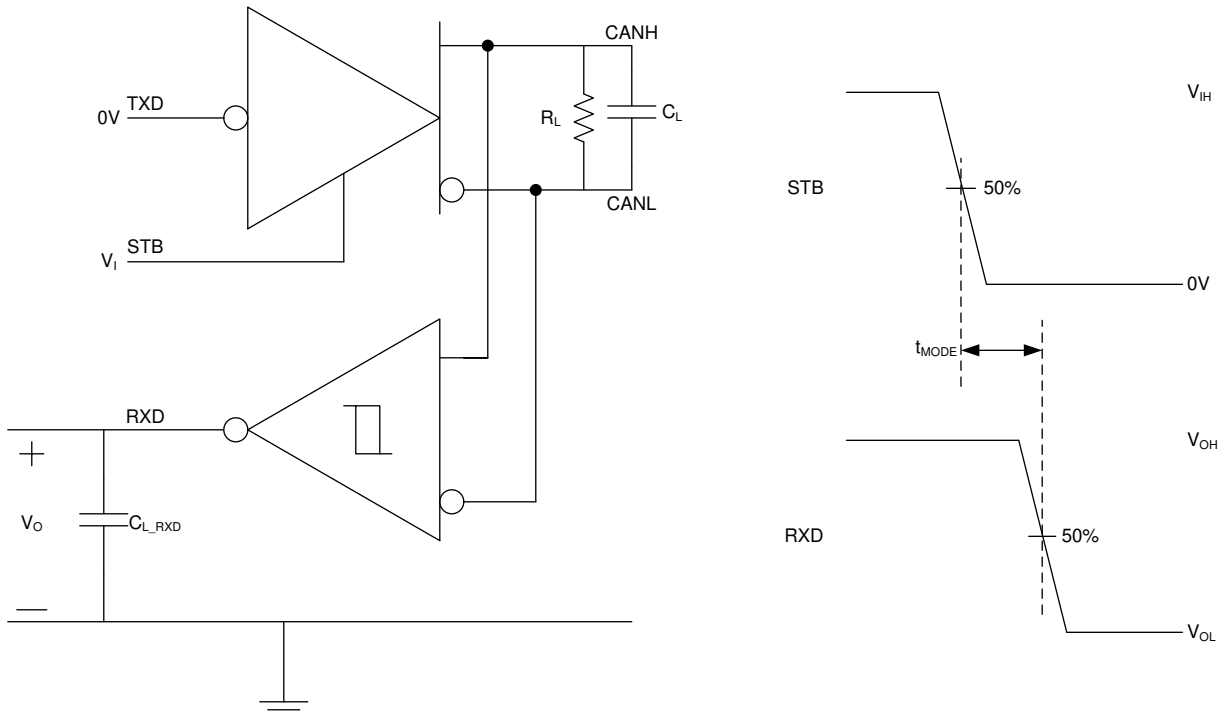
7-2. Driver Test Circuit and Measurement



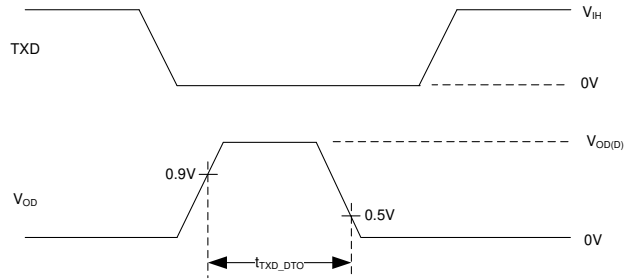
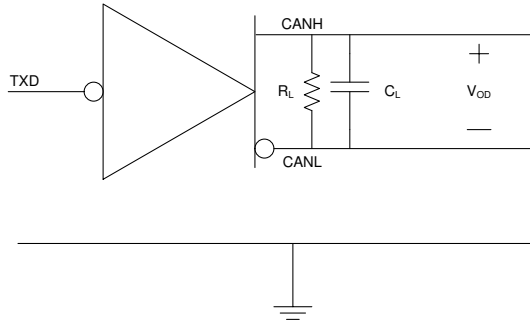
7-3. Receiver Test Circuit and Measurement



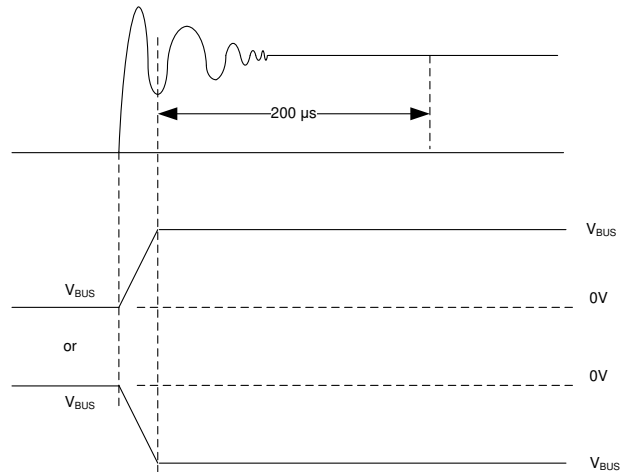
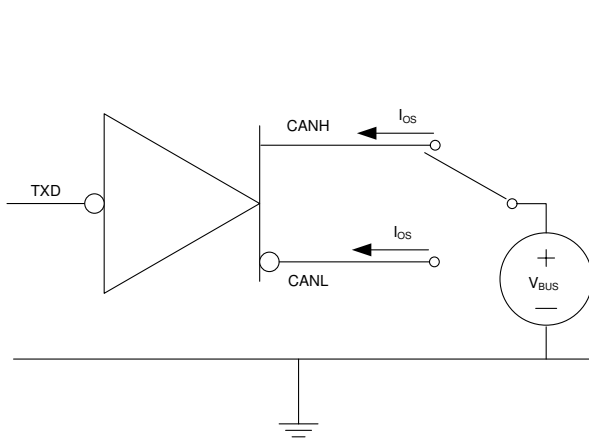
**图 7-4. Transmitter and Receiver Timing Test Circuit and Measurement**



**图 7-5.  $t_{MODE}$  Test Circuit and Measurement**



**7-6. TXD Dominant Timeout Test Circuit and Measurement**



**7-7. Driver Short-Circuit Current Test and Measurement**

## 8 Detailed Description

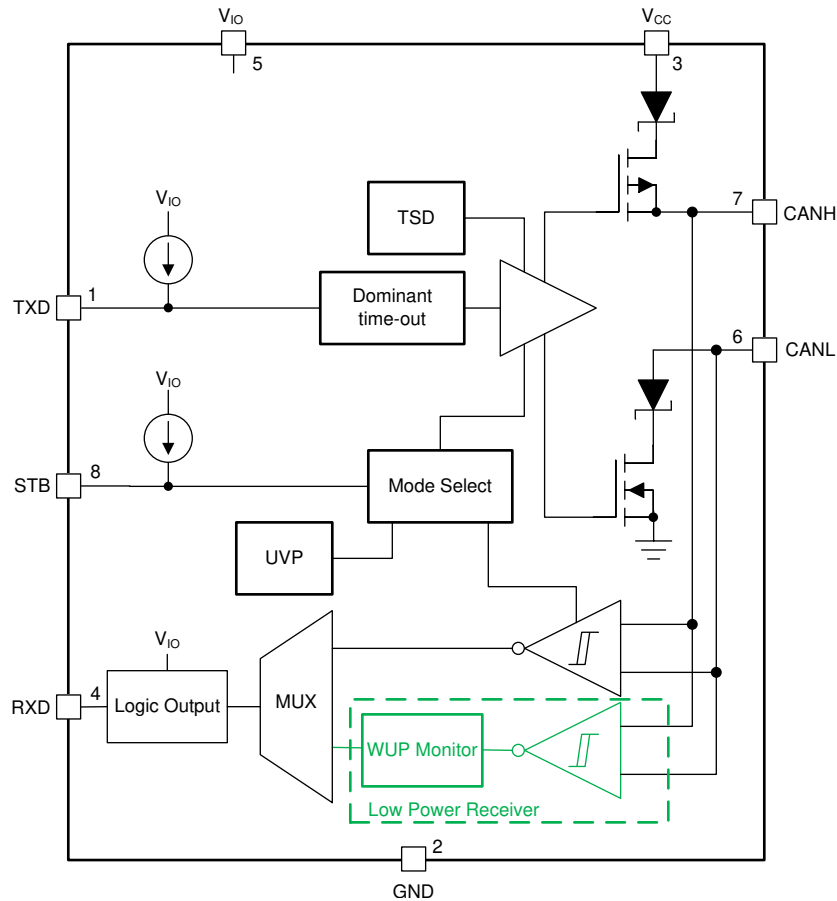
### 8.1 Overview

The TCAN1044AEV-Q1 meets or exceeds the specifications of the ISO 11898-2:2016 high-speed CAN (Controller Area Network) physical layer standard. The devices have been certified to the requirements of ISO 11898-2:2016 physical layer requirements according to the GIFT/ICT high speed CAN test specification. The transceivers provide a number of different protection features making it ideal for the stringent automotive system requirements while also supporting CAN FD data rates up to 8 Mbps.

The TCAN1044AEV-Q1 supports the following CAN and CAN FD standards:

- Physical layer:
  - ISO 11898-2:2016 High-speed medium access unit
  - ISO 11898-5:2007 High-speed medium access unit with low-power mode
  - SAE J2284-1: High-Speed CAN (HSC) for Vehicle Applications at 125 kbps
  - SAE J2284-2: High-Speed CAN (HSC) for Vehicle Applications at 250 kbps
  - SAE J2284-3: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps
  - SAE J2284-4: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 2 Mbps
  - SAE J2284-5: High-Speed CAN (HSC) for Vehicle Applications at 500 kbps with CAN FD Data at 5 Mbps
- EMC Requirements
  - IEC 62228-3 EMC evaluation of transceivers - CAN transceivers
  - VeLIO (Vehicle LAN Interoperability and Optimization) CAN and CAN-FD Transceiver Requirements
  - SAE J2962-2 Communication Transceivers Qualification Requirements – CAN
- Conformance test requirements:
  - ISO 16845-2 Road vehicles – Controller area network (CAN) conformance test plan Part 2: High-speed medium access unit conformance test plan

## 8.2 Functional Block Diagram



**8-1. Block Diagram**

## 8.3 Feature Description

### 8.3.1 Pin Description

#### 8.3.1.1 TXD

The TXD input is a logic-level signal, referenced to  $V_{IO}$  from a CAN controller to the transceiver.

#### 8.3.1.2 GND

GND is the ground pin of the transceiver. The pin must be connected to the PCB ground.

#### 8.3.1.3 $V_{CC}$

$V_{CC}$  provides the 5-V power supply to the CAN transceiver.

#### 8.3.1.4 RXD

RXD is the logic-level signal, referenced to  $V_{IO}$ , from the TCAN1044AEV-Q1 to a CAN controller. This pin is only driven once  $V_{IO}$  is present.

#### 8.3.1.5 $V_{IO}$

The  $V_{IO}$  pin provides the digital I/O voltage to match the CAN controller voltage thus avoiding the requirement for a level shifter. It supports voltages from 1.7 V to 5.5 V providing the widest range of controller support.

#### 8.3.1.6 CANH and CANL

The CANH and CANL pins are the CAN high and CAN low differential bus pins. These pins are internally connected to the CAN transmitter, receiver and the low-power wake-up receiver.

### 8.3.1.7 STB (Standby)

The STB pin is an input pin used for mode control of the transceiver. The STB pin can be supplied from either the system processor or from a static system voltage source. If normal mode is the only intended mode of operation, the STB pin can be tied directly to GND.

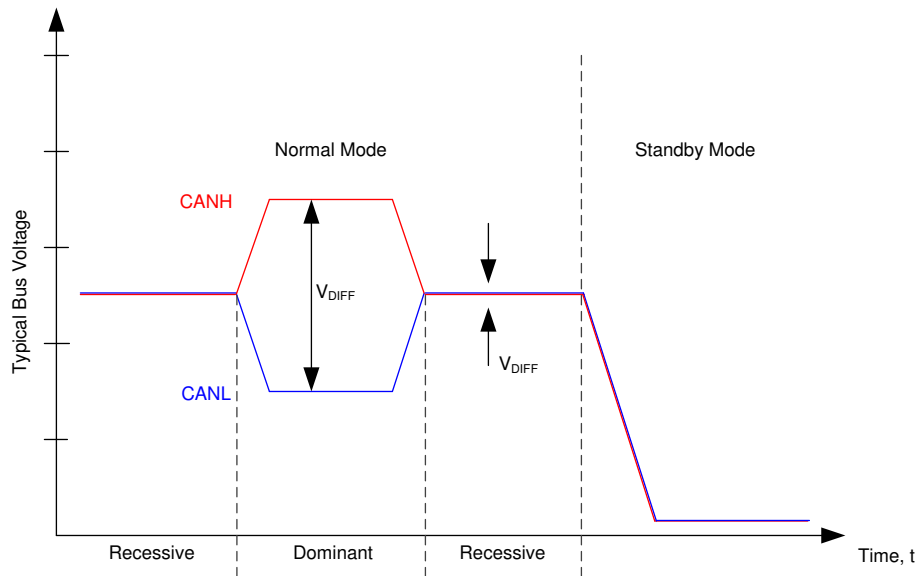
### 8.3.2 CAN Bus States

The CAN bus has two logical states during operation: recessive and dominant. See [8-2](#) and [8-3](#).

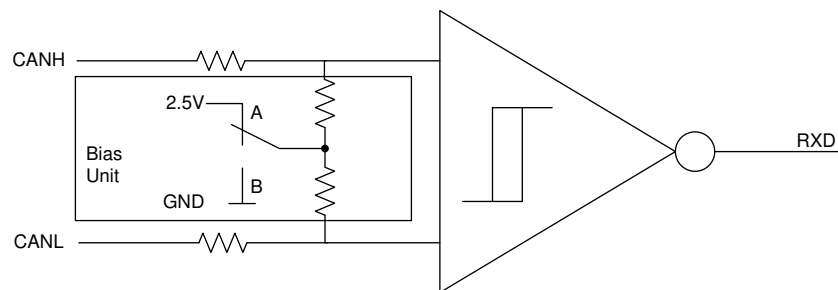
A dominant bus state occurs when the bus is driven differentially and corresponds to a logic low on the TXD and RXD pins. A recessive bus state occurs when the bus is biased to  $V_{CC}/2$  via the high-resistance internal input resistors ( $R_{IN}$ ) of the receiver and corresponds to a logic high on the TXD and RXD pins.

A dominant state overwrites the recessive state during arbitration. Multiple CAN nodes may be transmitting a dominant bit at the same time during arbitration, and in this case the differential voltage of the bus is greater than the differential voltage of a single driver.

The TCAN1044AEV-Q1 transceiver implements a low-power standby (STB) mode which enables a third bus state where the bus pins are weakly biased to ground via the high resistance internal resistors of the receiver. See [8-2](#) and [8-3](#).



**8-2. Bus States**



A. A - Normal Mode B - Standby Mode

**8-3. Simplified Recessive Common Mode Bias Unit and Receiver**



### 8.3.3 TXD Dominant Timeout (DTO)

During normal mode, the only mode where the CAN driver is active, the TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the timeout period  $t_{TXD\_DTO}$ . The TXD DTO circuit is triggered by a falling edge on TXD. If no rising edge is seen before the timeout period of the circuit,  $t_{TXD\_DTO}$ , the CAN driver is disabled. This frees the bus for communication between other nodes on the network. The CAN driver is reactivated when a recessive signal is seen on the TXD pin, thus clearing the dominant time out. The receiver remains active and biased to  $V_{CC}/2$  and the RXD output reflects the activity on the CAN bus during the TXD DTO fault.

The minimum dominant TXD time allowed by the TXD DTO circuit limits the minimum possible transmitted data rate of the device. The CAN protocol allows a maximum of eleven successive dominant bits (on TXD) for the worst case, where five successive dominant bits are followed immediately by an error frame. The minimum transmitted data rate may be calculated using 式 1.

$$\text{Minimum Data Rate} = 11 \text{ bits} / t_{TXD\_DTO} = 11 \text{ bits} / 1.2 \text{ ms} = 9.2 \text{ kbps} \quad (1)$$

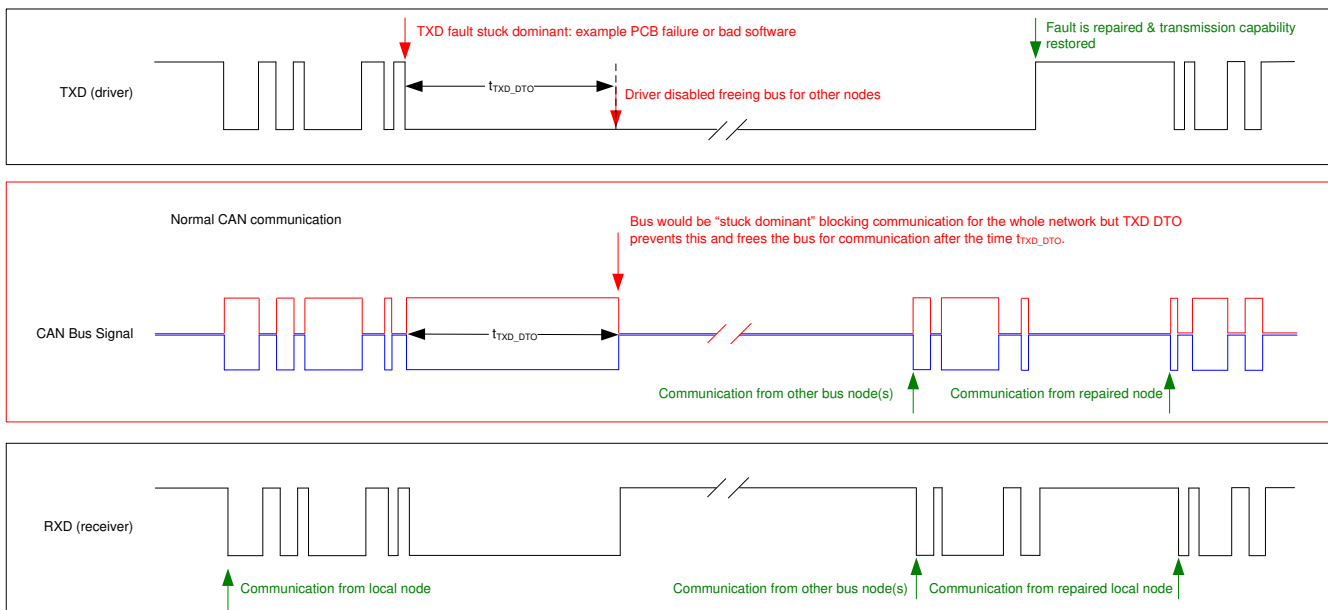


图 8-4. Example Timing Diagram for TXD Dominant Timeout

### 8.3.4 CAN Bus Short-Circuit Current Limiting

The TCAN1044AEV-Q1 has several protection features that limit the short-circuit current when a CAN bus line is shorted. These include CAN driver current limiting in the dominant and recessive states and TXD dominant state timeout which prevents permanently having the higher short-circuit current of a dominant state in case of a system fault. During CAN communication the bus switches between the dominant and recessive states, thus the short-circuit current may be viewed as either the current during each bus state or as a DC average current. When selecting termination resistors or a common-mode choke for the CAN design the average power rating,  $I_{OS(AVG)}$ , should be used. The percentage dominant is limited by the TXD DTO and the CAN protocol which has forced state changes and recessive bits due to bit stuffing, control fields, and interframe space. These ensure there is a minimum amount of recessive time on the bus even if the data field contains a high percentage of dominant bits.

The average short-circuit current of the bus depends on the ratio of recessive to dominant bits and their respective short-circuit currents. The average short-circuit current may be calculated using 式 2.

$$I_{OS(AVG)} = \% \text{ Transmit} \times [(\% \text{ REC\_Bits} \times I_{OS(SS\_REC)}) + (\% \text{ DOM\_Bits} \times I_{OS(SS\_DOM)})] + [\% \text{ Receive} \times I_{OS(SS\_REC)}] \quad (2)$$

Where:

- $I_{OS(AVG)}$  is the average short-circuit current
- % Transmit is the percentage the node is transmitting CAN messages
- % Receive is the percentage the node is receiving CAN messages
- % REC\_Bits is the percentage of recessive bits in the transmitted CAN messages
- % DOM\_Bits is the percentage of dominant bits in the transmitted CAN messages
- $I_{OS(SS)_REC}$  is the recessive steady state short-circuit current
- $I_{OS(SS)_DOM}$  is the dominant steady state short-circuit current

This short-circuit current and the possible fault cases of the network should be taken into consideration when sizing the power supply used to generate the transceivers  $V_{CC}$  supply.

### 8.3.5 Thermal Shutdown (TSD)

If the junction temperature of the TCAN1044AEV-Q1 exceeds the thermal shutdown threshold,  $T_{TSD}$ , the device turns off the CAN driver circuitry and blocks the TXD to bus transmission path. The shutdown condition is cleared when the junction temperature of the device drops below  $T_{TSD}$ . The CAN bus pins are biased to  $V_{CC}/2$  during a TSD fault and the receiver to RXD path remains operational. The TCAN1044AEV-Q1 TSD circuit includes hysteresis which prevents the CAN driver output from oscillating during a TSD fault.

### 8.3.6 Undervoltage Lockout

The supply pins,  $V_{CC}$  and  $V_{IO}$ , have undervoltage detection that places the device into a protected state. This protects the bus during an undervoltage event on either supply pin.

**表 8-1. Undervoltage Lockout - TCAN1044AEV-Q1**

$V_{CC}$	$V_{IO}$	DEVICE STATE	BUS	RXD PIN
$> UV_{VCC}$	$> UV_{VIO}$	Normal	Per TXD	Mirrors bus
$< UV_{VCC}$	$> UV_{VIO}$	STB = High: Standby Mode	Weak biased to GND	$V_{IO}$ : Remote wake request See <a href="#">Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode</a>
		STB =Low: Protected Mode	High impedance	Recessive
$> UV_{VCC}$	$< UV_{VIO}$	Protected	High impedance	High impedance
$< UV_{VCC}$	$< UV_{VIO}$	Protected	High impedance	High impedance

Once the undervoltage condition is cleared and  $t_{MODE}$  has expired the TCAN1044AEV-Q1 will transition to normal mode and the host controller can send and receive CAN traffic again

### 8.3.7 Unpowered Device

The TCAN1044AEV-Q1 is designed to be an ideal passive or no load to the CAN bus if the device is unpowered. The bus pins were designed to have low leakage currents when the device is unpowered, so they do not load the bus. This is critical if some nodes of the network are unpowered while the rest of the of network remains operational.

The logic pins also have low leakage currents when the device is unpowered, so they do not load other circuits which may remain powered.

### 8.3.8 Floating pins

The TCAN1044AEV-Q1 has internal pull-ups on critical pins which place the device into known states if the pin floats. This internal bias should not be relied upon by design though, especially in noisy environments, but instead should be considered a failsafe protection feature.

When a CAN controller supporting open-drain outputs is used an adequate external pull-up resistor must be chosen. This ensures that the TXD output of the CAN controller maintains acceptable bit time to the input of the CAN transceiver. See [表 8-2](#) for details on pin bias conditions.

**表 8-2. Pin Bias**

Pin	Pull-up or Pull-down	Comment
TXD	Pull-up	Weakly biases TXD towards recessive to prevent bus blockage or TXD DTO triggering
STB	Pull-up	Weakly biases STB towards low-power standby mode to prevent excessive system power

## 8.4 Device Functional Modes

### 8.4.1 Operating Modes

The TCAN1044AEV-Q1 has two main operating modes; normal mode and standby mode. Operating mode selection is made by applying a high or low level to the STB pin.

**表 8-3. Operating Modes**

STB	Device Mode	Driver	Receiver	RXD Pin
High	Low current standby mode with bus wake-up	Disabled	Low-power receiver and bus monitor enable	High (recessive) until valid WUP is received See <a href="#">Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode</a>
Low	Normal Mode	Enabled	Enabled	Mirrors bus state

### 8.4.2 Normal Mode

This is the normal operating mode of the TCAN1044AEV-Q1. The CAN driver and receiver are fully operational and CAN communication is bi-directional.

The driver is translating a digital input on the TXD input to a differential output on the CANH and CANL bus pins.

The receiver is translating the differential signal from CANH and CANL to a digital output on the RXD output.

### 8.4.3 Standby Mode

This is the low-power mode of the TCAN1044AEV-Q1. The CAN driver and main receiver are switched off and bi-directional CAN communication is not possible. The low-power receiver and bus monitor circuits are enabled to allow for RXD wake-up requests via the CAN bus. A wake-up request is output to RXD as shown in [Figure 8-5](#). The local CAN protocol controller should monitor RXD for transitions (high-to-low) and reactivate the device to normal mode by pulling the STB pin low. The CAN bus pins are weakly pulled to GND in this mode; see [Figure 8-2](#) and [Figure 8-3](#).

In standby mode, only the  $V_{IO}$  supply is required; therefore, the  $V_{CC}$  may be switched off for additional system level current savings.

#### 8.4.3.1 Remote Wake Request via Wake-Up Pattern (WUP) in Standby Mode

The TCAN1044AEV-Q1 supports a remote wake-up request that is used to indicate to the host controller that the bus is active and the node should return to normal operation.

The device uses the multiple filtered dominant wake-up pattern (WUP) from the ISO 11898-2:2016 standard to qualify bus activity. Once a valid WUP has been received, the wake request is indicated to the controller by a falling edge and low period corresponding to a filtered dominant on the RXD output of the TCAN1044AEV-Q1.

The WUP consists of a filtered dominant pulse, followed by a filtered recessive pulse, and finally by a second filtered dominant pulse. The first filtered dominant initiates the WUP, and the bus monitor then waits on a filtered recessive; other bus traffic does not reset the bus monitor. Once a filtered recessive is received the bus monitor is waiting for a filtered dominant and again, other bus traffic does not reset the bus monitor. Immediately upon reception of the second filtered dominant the bus monitor recognizes the WUP and drives the RXD output low every time an additional filtered dominant signal is received from the bus.

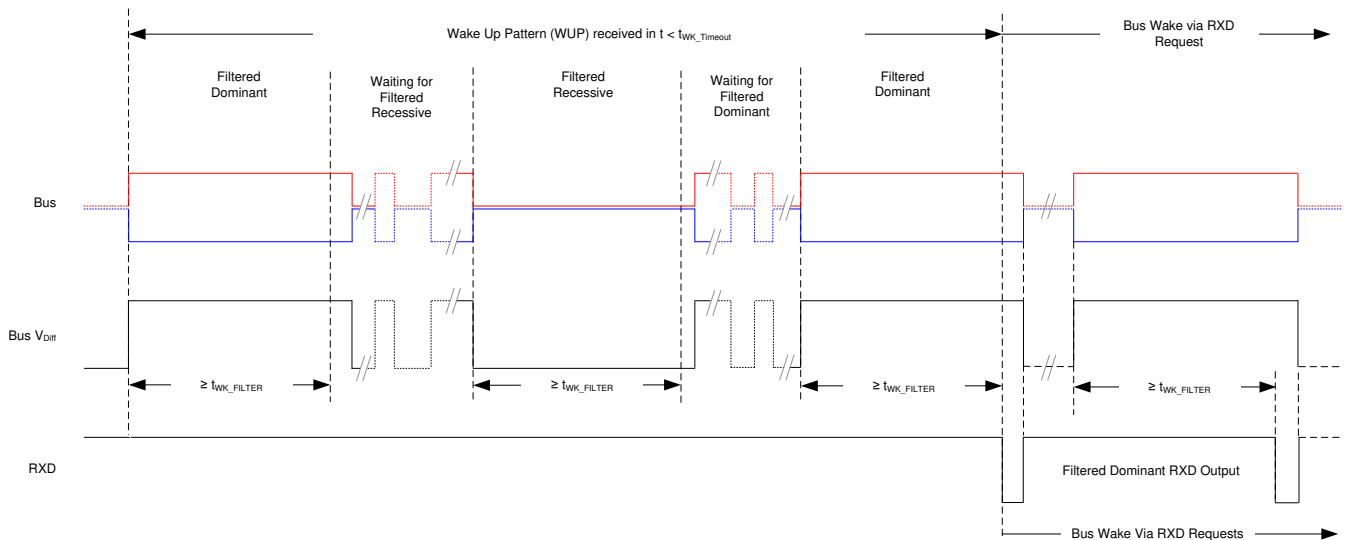
For a dominant or recessive to be considered filtered, the bus must be in that state for more than the  $t_{WK\_FILTER}$  time. Due to variability in  $t_{WK\_FILTER}$  the following scenarios are applicable. Bus state times less than

$t_{WK\_FILTER(MIN)}$  are never detected as part of a WUP and thus no wake request is generated. Bus state times between  $t_{WK\_FILTER(MIN)}$  and  $t_{WK\_FILTER(MAX)}$  may be detected as part of a WUP and a wake-up request may be generated. Bus state times greater than  $t_{WK\_FILTER(MAX)}$  are always detected as part of a WUP, and thus a wake request is always generated. See [Figure 8-5](#) for the timing diagram of the wake-up pattern.

The pattern and  $t_{WK\_FILTER}$  time used for the WUP prevents noise and bus stuck dominant faults from causing false wake-up requests while allowing any valid message to initiate a wake-up request.

The ISO 11898-2:2016 standard has defined times for a short and long wake-up filter time. The  $t_{WK\_FILTER}$  timing for the device has been picked to be within the minimum and maximum values of both filter ranges. This timing has been chosen such that a single bit time at 500 kbps, or two back-to-back bit times at 1 Mbps triggers the filter in either bus state. Any CAN frame at 500 kbps or less would contain a valid WUP.

For an additional layer of robustness and to prevent false wake-ups, the device implements a wake-up timeout feature. For a remote wake-up event to successfully occur, the entire WUP must be received within the timeout value  $t \leq t_{WK\_TIMEOUT}$ . If not, the internal logic is reset and the transceiver remains in its current state without waking up. The full pattern must then be transmitted again, conforming to the constraints mentioned in this section. See [Figure 8-5](#) for the timing diagram of the wake-up pattern with wake timeout feature.



**Figure 8-5. Wake-Up Pattern (WUP) with  $t_{WK\_TIMEOUT}$**

### 8.4.4 Driver and Receiver Function

The TCAN1044AEV-Q1 logic I/Os support CMOS levels with respect to  $V_{IO}$  for compatibility with MCUs that support 1.8-V, 2.5-V, 3.3-V, or 5-V systems.

**Table 8-4. Driver Function Table**

Device Mode	TXD Input <sup>(1)</sup>	Bus Outputs		Driven Bus State <sup>(2)</sup>
		CANH	CANL	
Normal	Low	High	Low	Dominant
	High or open	High impedance	High impedance	Biased recessive
Standby	X	High impedance	High impedance	Biased to ground

(1) X = irrelevant

(2) For bus state and bias see [Figure 8-2](#) and [Figure 8-3](#)

**表 8-5. Receiver Function Table Normal and Standby Mode**

Device Mode	CAN Differential Inputs $V_{ID} = V_{CANH} - V_{CANL}$	Bus State	RXD Pin
Normal	$V_{ID} \geq 0.9 \text{ V}$	Dominant	Low
	$0.5 \text{ V} < V_{ID} < 0.9 \text{ V}$	Undefined	Undefined
	$V_{ID} \leq 0.5 \text{ V}$	Recessive	High
Standby	$V_{ID} \geq 1.15 \text{ V}$	Dominant	High
	$0.4 \text{ V} < V_{ID} < 1.15 \text{ V}$	Undefined	Low if a remote wake event occurred
	$V_{ID} \leq 0.4 \text{ V}$	Recessive	See <a href="#">Figure 8-5</a>
Any	Open ( $V_{ID} \approx 0 \text{ V}$ )	Open	High

## 9 Application Information Disclaimer

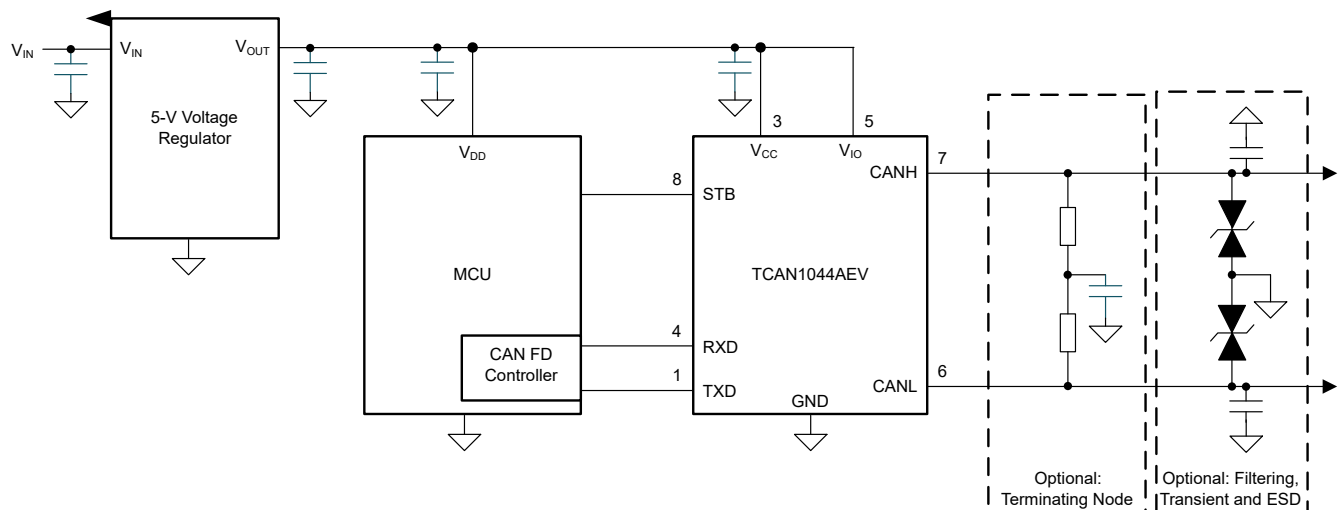
### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.2 Typical Application

The TCAN1044AEV-Q1 transceiver can be used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. [Figure 9-1](#) shows a typical configuration for 5-V controller applications. The bus termination is shown for illustrative purposes.

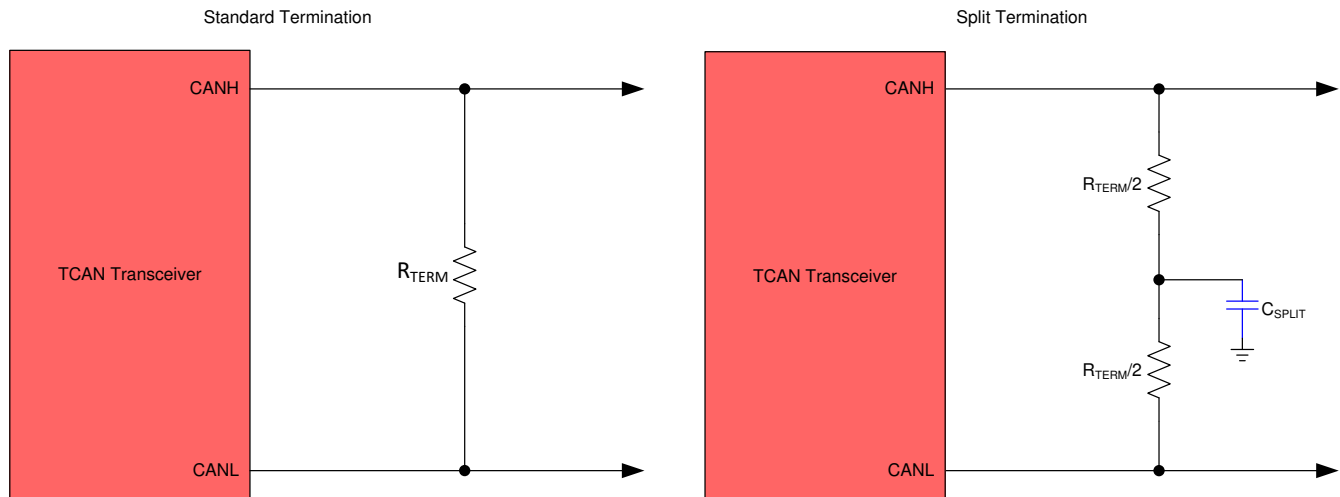


**Figure 9-1. Transceiver Application Using 5-V IO Connections**

#### 9.2.1 Design Requirements

##### 9.2.1.1 CAN Termination

Termination may be a single 120-Ω resistor at each end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common-mode voltage of the bus is desired then split termination may be used, see [Figure 9-2](#). Split termination improves the electromagnetic emissions behavior of the network by filtering higher-frequency common-mode noise that may be present on the differential signal lines.



**图 9-2. CAN Bus Termination Concepts**

## 9.2.2 Detailed Design Procedures

### 9.2.2.1 Bus Loading, Length and Number of Nodes

A typical CAN application may have a maximum bus length of 40 meters and maximum stub length of 0.3 m. However, with careful design, users can have longer cables, longer stub lengths, and many more nodes to a bus. A high number of nodes requires a transceiver with high input impedance such as the TCAN1044AEV-Q1.

Many CAN organizations and standards have scaled the use of CAN for applications outside the original ISO 11898-2 standard. They made system level trade off decisions for data rate, cable length, and parasitic loading of the bus. Examples of these CAN systems level specifications are ARINC 825, CANopen, DeviceNet, SAE J2284, SAE J1939, and NMEA 2000.

A CAN network system design is a series of tradeoffs. In the ISO 11898-2:2016 specification the driver differential output is specified with a bus load that can range from 50  $\Omega$  to 65  $\Omega$  where the differential output must be greater than 1.5 V. The TCAN1044AEV-Q1 is specified to meet the 1.5-V requirement down to 50  $\Omega$  and is specified to meet 1.4-V differential output at 45- $\Omega$  bus load. The differential input resistance of the TCAN1044AEV-Q1 is a minimum of 40 k $\Omega$ . If 100 TCAN1044AEV-Q1 transceivers are in parallel on a bus, this is equivalent to a 400- $\Omega$  differential load in parallel with the nominal 60- $\Omega$  bus termination which gives a total bus load of approximately 52  $\Omega$ . Therefore, the TCAN1044AEV-Q1 theoretically supports over 100 transceivers on a single bus segment. However, for a CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, timing, network imbalances, ground offsets, and signal integrity thus a practical maximum number of nodes is often lower. Bus length may also be extended beyond 40 meters by careful system design and data rate tradeoffs. For example, CANopen network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

This flexibility in CAN network design is one of the key strengths of the various extensions and additional standards that have been built on the original ISO 11898-2 CAN standard. However, when using this flexibility the CAN network system designer must take the responsibility of good network design to ensure robust network operation.

Please refer to the application report [SLLA270: Controller Area Network Physical layer requirements](#). This document discusses in detail all system design physical layer parameters.

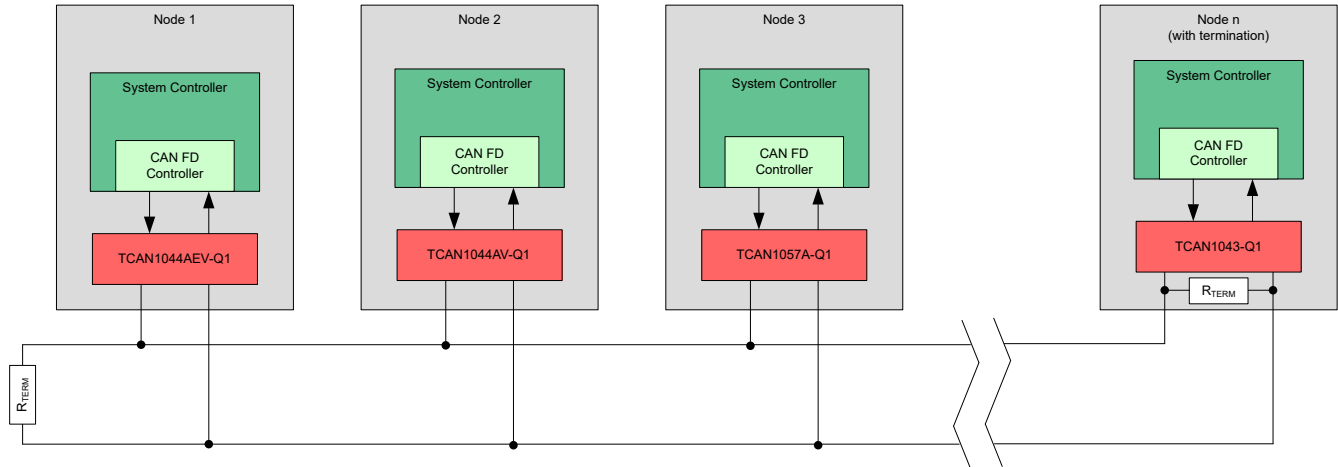


Figure 9-3. Typical CAN Bus

### 9.3 System Examples

The TCAN1044AEV-Q1 CAN transceiver is typically used in applications with a host controller or FPGA that includes the link layer portion of the CAN protocol. A 1.8-V, 2.5-V, or 3.3-V application is shown in Figure 9-4. The bus termination is shown for illustrative purposes.

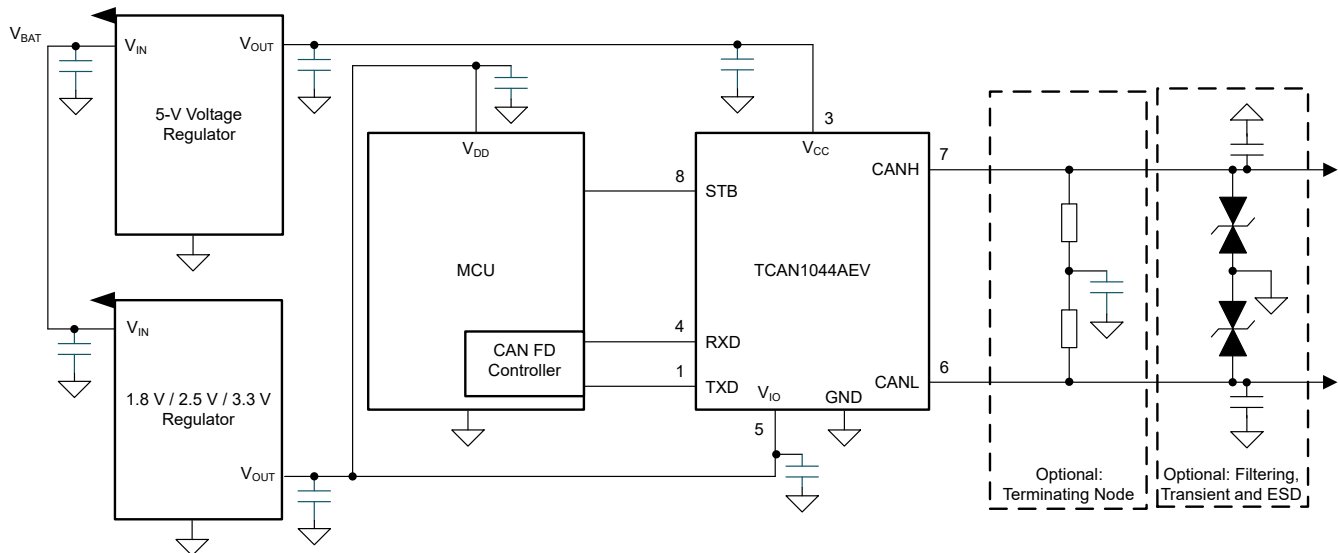


Figure 9-4. Typical Transceiver Application Using 1.8-V, 2.5-V, 3.3-V IO Connections

## 10 Power Supply Recommendations

The TCAN1044AEV-Q1 transceiver is designed to operate with a main  $V_{CC}$  input voltage supply range between 4.5 V and 5.5 V.

The device implements an I/O level shifting supply input,  $V_{IO}$ , designed for a range between 1.8 V and 5.5 V.

Both the  $V_{CC}$  and  $V_{IO}$  inputs must be well regulated. In addition to the power supply filtering a decoupling capacitance, typically 100 nF, should be placed near the CAN transceiver's main  $V_{CC}$  and  $V_{IO}$  supply pins.



## 11 Layout

Robust and reliable CAN node design may require special layout techniques depending on the application and design requirements. Since transient disturbances have high frequency content and a wide bandwidth, high-frequency layout techniques should be applied during PCB design.

### 11.1 Layout Guidelines

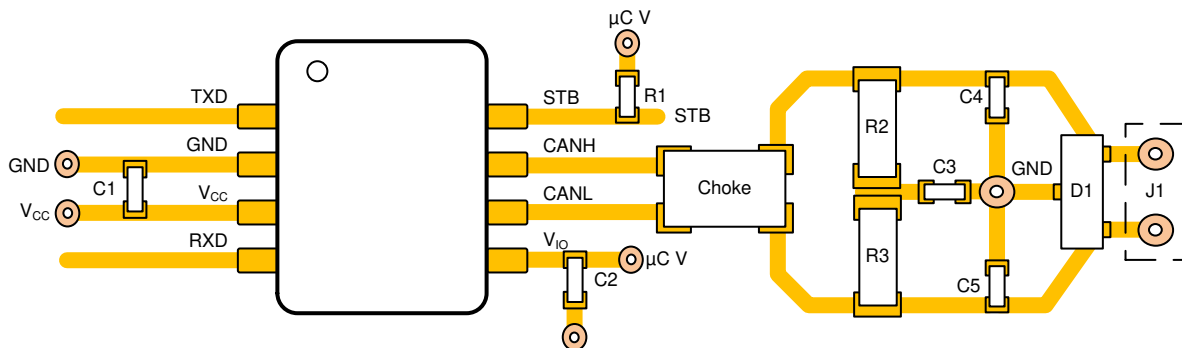
- Place the protection and filtering circuitry close to the bus connector, J1, to prevent transients, ESD, and noise from propagating onto the board. This layout example shows an optional transient voltage suppression (TVS) diode, D1, which may be implemented if the system-level requirements exceed the specified rating of the transceiver. This example also shows optional bus filter capacitors C4 and C5.
- Design the bus protection components in the direction of the signal path. Do not force the transient current to divert from the signal path to reach the protection device.
- Decoupling capacitors should be placed as close as possible to the supply pins  $V_{CC}$  and  $V_{IO}$  of transceiver.
- Use at least two vias for supply and ground connections of bypass capacitors and protection devices to minimize trace and via inductance.

#### Note

High-frequency current follows the path of least impedance and not the path of least resistance.

- This layout example shows how split termination could be implemented on the CAN node. The termination is split into two resistors, R2 and R3, with the center or split tap of the termination connected to ground via capacitor C3. Split termination provides common mode filtering for the bus. See [セクション 9.2.1.1](#), [セクション 8.3.4](#), and [式 2](#) for information on termination concepts and power ratings needed for the termination resistor(s).

### 11.2 Layout Example



11-1. Layout Example

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 サポート・リソース

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCAN1044AEVDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	2HJF	<a href="#">Samples</a>
TCAN1044AEVDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 150	44AEV	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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# DDF0008A



# PACKAGE OUTLINE

## SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

## NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed  $.006$  [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.



# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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