Application Note

Practical Clocking Considerations That Give Your Next High-Speed Converter Design an Edge

Andrea Vallenilla, Rob Reeder

ABSTRACT

There are many deliberations when creating designs with high-speed analog-to-digital converters, or ADC. Understanding the ADC sampling clocking is just one of these deliberations which is paramount to making sure your design requirements are met. There are several metrics that need to be understood about the ADC sampling clock that have a direct effect on the ADC performance (or signal-to-noise ratio, SNR) as discussed in the analog design journal article *Clock jitter analyzed in the time domain Part 1*, *Part 2*, and *Part 3*. However, from a practical stand point, what does that mean? In this application note, numerous experiments and tradeoffs are uncovered and proven on the bench to give better insight for your next high-speed ADC clock design.

Table of Contents

Trademarks

1 Introduction

In this application note, the tradeoffs of different clocking parameters are uncovered and proven on the bench. This demonstrates different common behaviors to avoid common pitfalls when designing your clock tree on your next high-speed converter design. Some relationships seen include the effect of the clock performance when increasing the analog input frequency, the clock slew rate's effect on the performance of the ADC, and so on.

2 Understanding the Difference Between Phase Noise and Jitter

Good phase noise is paramount when maximizing the performance of any ADC. Understanding the sampling clock's phase noise and the relationship to jitter is important when trying to achieve the desired converter's rated performance.

Typically, a phase noise curve or plot is used to analyze the overall noise performance of a clock or clocking signal chain. Phase noise is the accumulation of any additive noise coming from the power supply or other noise contributors that influence the clock's *pure* tone and lead to the signal deviating from the ideal. The signal *wonders* in phase, generating a phase noise curve around the analyzed signal tone. Jitter is then computed by integrating the signal tone's phase noise curve over a specific frequency range, or an integration bandwidth. Figure 2-1 illustrates a phase noise curve with an integration bandwidth of 20Hz to 130MHz. The blue line is the phase noise curve being analyzed and the two red vertical lines represent the integration bandwidth limits.

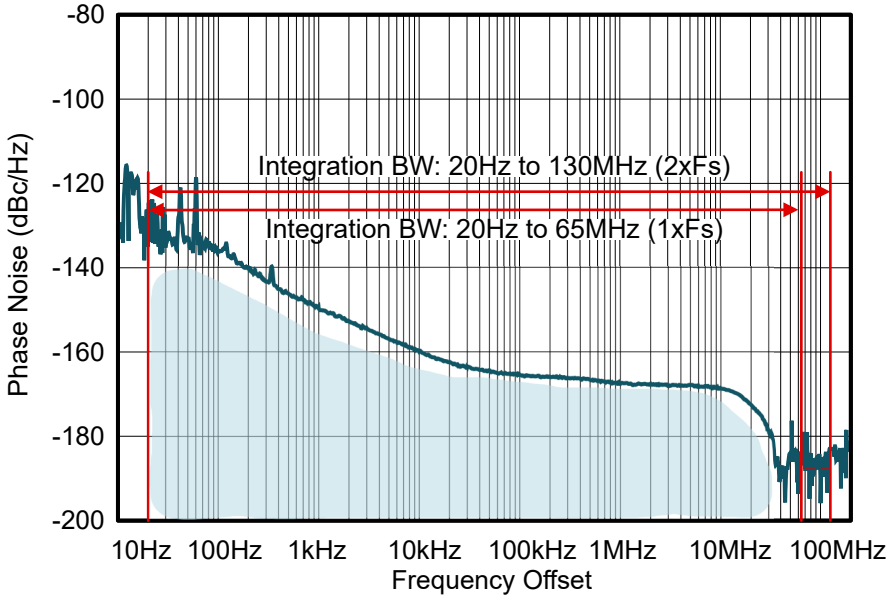

Figure 2-1. Phase Noise Curve Using a Specific Integration Bandwidth to Obtain Jitter

To calculate jitter, set the lower integration bandwidth limit to a value close to DC to consider the entire phase noise profile of the clock. In this application, we selected 20Hz. To obtain the upper integration limit, we recommended to use at least the ADC sampling frequency (Fs) and for an even better analysis, 2×Fs. For example, if the ADC was being sampled at 65MSPS, the integration bandwidth ranges from 20Hz to at least 65MHz (or up to 130MHz for a more detailed noise consideration). Many times, 2×Fs is more appropriate to understand the broadband noise contribution and make sure the sampling clock's noise floor is reached.

After determining the integration bandwidth, jitter can be calculated from the phase noise curve. First, break each section into various quadrants broken up against a log scale, for example, 10kHz to 100kHz, 100kHz to 1MHz, and so on. Each quadrant is then integrated separately to determine the noise power. Each noise power is then added together to understand the total noise power under the curve. Finally, compute the RMS phase jitter in either radians or seconds from the total noise power. Figure 2-2 demonstrates how a phase noise curve is integrated to compute total jitter around a specified integration bandwidth using four quadrants.

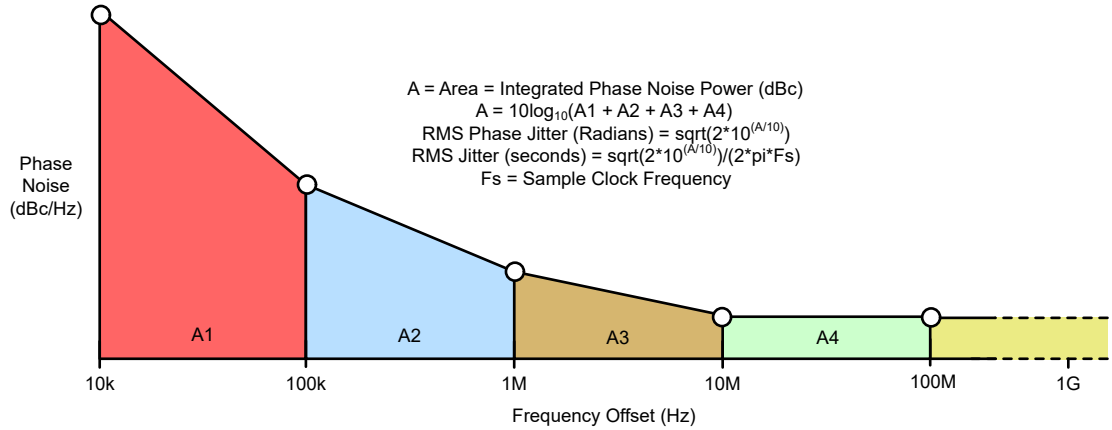

Figure 2-2. Representation of Calculating Phase Noise to Jitter Using a Simpler Approach

3 Understanding How Phase Noise or Jitter can Affect the ADC Performance

Equation 1 depicts the SNR relationship for an ADC. SNR_Q is the ADC inherent quantization, SNR_N is the thermal noise of the ADC, and SNR_J is the contributed overall jitter. SNR_J, shown in Equation 4, is a combination of the entire clock signal chain additive jitter and the ADC inherent aperture jitter in relation to the analog input frequency. The following equations clearly demonstrate that the overall SNR performance is not just dependent on the clock jitter alone but a combination of several terms.

$$SNR_{ADC}\left[\text{dBc}\right] = -20\log\sqrt{\left[10\left(\frac{-\text{SNR}_Q}{20}\right)\right]^2 + \left[10\left(\frac{-\text{SNR}_N}{20}\right)\right]^2 + \left[10\left(\frac{-\text{SNR}_J}{20}\right)\right]^2} \quad (1)$$

$$SNR_Q\left[\text{dBc}\right] = quantization\ of\ ADC \quad (2)$$

$$SNR_N[\text{dBc}] = thermal\ SNR\ of\ ADC \quad (3)$$

$$SNR_J[\text{dBc}] = \ overall\ jitter\ = \ -20\log\left(2\times\pi\times f_{in}\times t_J\right) \quad (4)$$

$$t_J = combined\ rms\ jitter = \sqrt{(clock\ input\ jitter)^2 + (ADC\ aperture\ jitter)^2} \quad (5)$$

Figure 3-1 simulates Equation 1 using one of the higher performing TI ADC, the ADC3683. Each colored curve represents a different clock jitter value demonstrating how increasing clock jitter decreases the SNR of the ADC3683 across analog input frequencies. Notice that for low analog input frequencies, regardless of the overall sampling clock jitter contribution, the ADC SNR performance is maintained because the ADC quantization and thermal SNR terms are significantly higher than the clock input jitter term. However, as the analog input frequency increases, the SNR starts to drop since the clock input term starts dominating the combined rms jitter term and masking the ADC quantization and thermal SNR, as demonstrated in Equation 4 and Equation 5. Clearly, the amount of SNR degradation highly depends on the overall jitter contribution, the ADC aperture jitter (ADC3683 aperture jitter is 180fs), and the difference in magnitude between the clock input jitter and the ADC aperture jitter. The red dashed line in Figure 3-1demonstrates the best performance that can be achieved by the ADC3683. The green and yellow curves are purely theoretical and cannot be achieved in practice and are meant to further show the relationship between a clock's jitter and an ADC SNR.

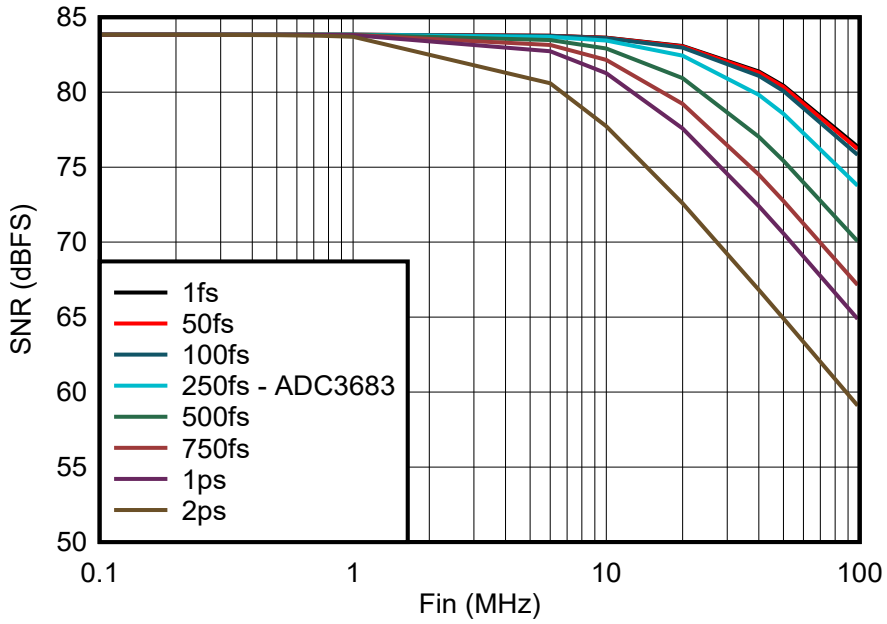

Figure 3-1. SNR vs. Fin External Clock Jitter Relationship

As mentioned before, a better-performing clock is required when higher analog input frequencies are used. This is because increasing the slope or slew rate of the analog input signal leads to a larger conversion error. To compensate for this extra added error, the system requires a less-jittery clock. Figure 3-2 illustrates more clearly how the same clock edge with the same amount of jitter translates to a larger delta error and worse SNR for the same amount of time, as the analog input frequency increases.

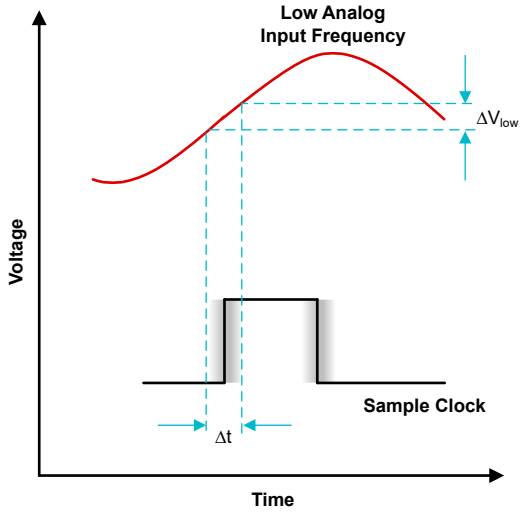

Figure 3-2. Low Analog Input Frequencies vs. the Same Sampling Clock Edge Occurring for the Same Time Period

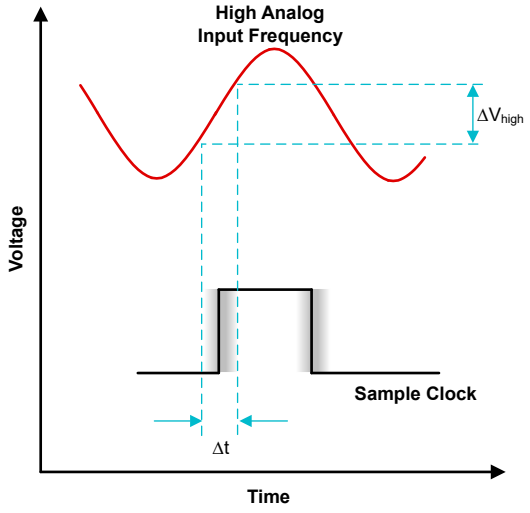

Figure 3-3. High Analog Input Frequencies vs. the Same Sampling Clock Edge Occurring for the Same Time Period

4 Understanding Clocking Tradeoffs and What this Means to an ADC Performance

Now to the fun part of the application note. Here we discuss the many trades offs when trying to achieve good performance out of your high-speed converter design. We start with the source, which is the signal generator used as a sampling clock source in the lab. In this experiment, several signal generators were used. The signal generator's phase noise measurements can be found in Figure 4-1. These phase noise measurements represent a direct connection from the signal generator to a phase noise analyzer. All signal generators were configured with a 25MHz output signal and an +10dBm output power. Keep in mind that a signal generator can have specific upgrades or options that enhance the default configuration off the shelf.

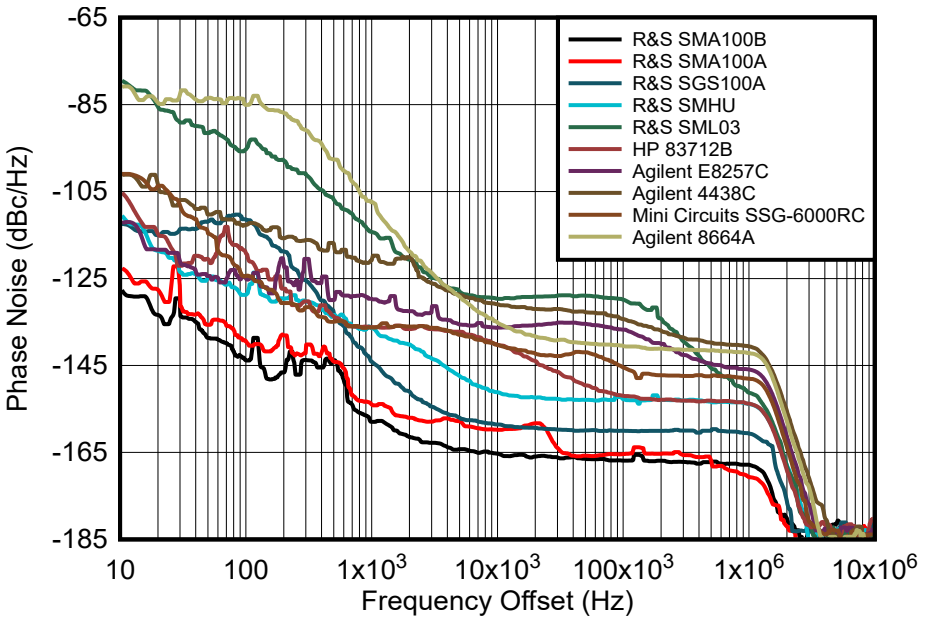

Figure 4-1. Phase Noise Curves of Different Signal Sources at 25MHz and +10dBm Output Power Level

All the experiments used an ADC3683 evaluation board, or EVM, with three different 10MHz reference-locked signal generators, one providing the clock input, another the analog input, and the third one providing the data clock input required by the ADC3683, as shown in Figure 4-2. All of these inputs into the ADC3683 were filtered using bandpass filters to remove any other unwanted noise and spurious coming from the signal generators. The signal generator used for the data clock input was a R&S SGS100A. For the analog input, we used the highest performance signal generator available on the market as of September 2024, the R&S SMA100B. Both of these signal generators were kept constant throughout all experiments unless otherwise stated.

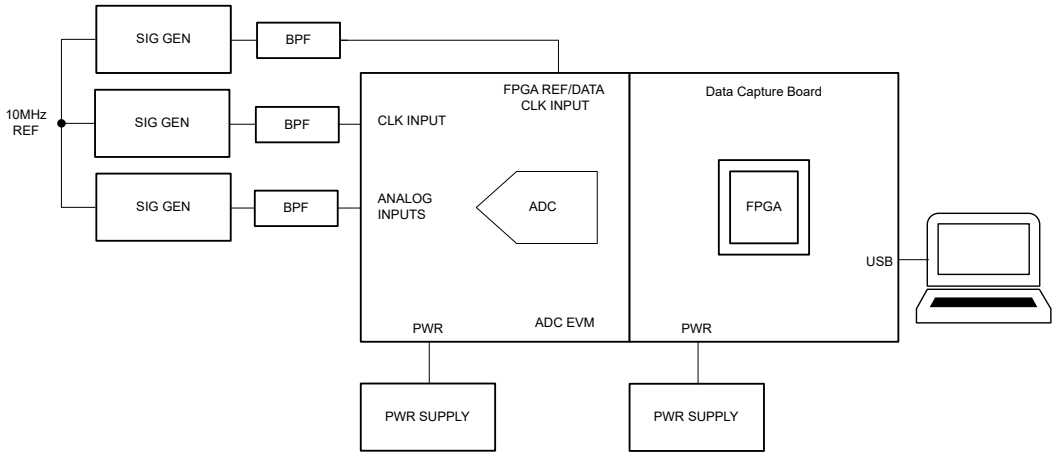

Figure 4-2. ADC Test Measurement Setup in the Lab

Figure 4-3 compares the converter's AC performance, or SNR, across increasing analog input frequencies. Here, the ADC3683 is clocked at 25MSPS with the different signal generators used in Figure 4-1. For each source tested, the clock was held constant at +10dBm, and the analog input frequency was swept from 2MHz to 30MHz. At each frequency point, the analog signal source signal generator output power level was adjusted to -1dBFS before the SNR value (in dBFS) was measured. To keep the experiment consistent, the highest performance signal source was always used for the analog input source and was not changed. As seen in both Figure 3-1 (theoretical) and Figure 4-1 (practical), when the analog frequency increases, the SNR starts to roll off and worsens, or the SNR is *jitter limited*. This means that the jitter or phase noise of the ADC clock source and or clock signal chain begins to dominate the overall performance of the converter, leading to worse SNR from the ADC when operating the converter with of a noisier clock source. Each signal generator has a slightly different phase noise contribution as the analog input frequency gets higher, whereas, at lower frequencies, the phase noise has less of an impact.

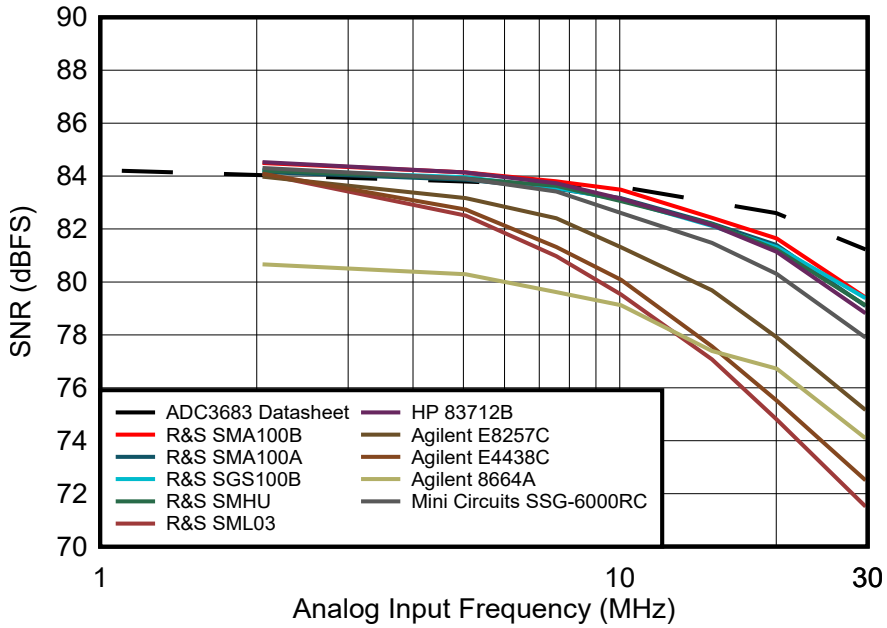

Figure 4-3. ADC3683 SNR vs. Fin With Different Clocking Signal Source at 25MSPS and +10dBm When Operating the ADC With a -1dBFS Analog Input Signal

The clock slew rate is another key characteristic that affects the ADC performance. The sharper the slew rate of the clocking edge, the better the chance to reduce the clock jitter. Also, faster slew rates minimize the timing uncertainty of the sampling clock edge when the clock edge is moving through the ADC sampling threshold. Figure 4-4 demonstrates the effect of the sampling clock slew rate versus the performance of the ADC. As shown in the figure, when decreasing the amplitude level of the 25MSPS clock source from +10dBm to -15dBm, and maintaining a constant output power level for the analog input frequencies (of 5MHz, solid lines and 30MHz, dashed lines), the SNR begins to decrease as the clock signal source becomes -5dBm or smaller. Keep in mind, each ADC has a unique level of sensitivity and -5dBm doesn't cover all ADC. -5dBm is only valid for this ADC test case and was used to demonstrate how sharper slew rates on the clock source lead to obtaining the best SNR from an ADC.

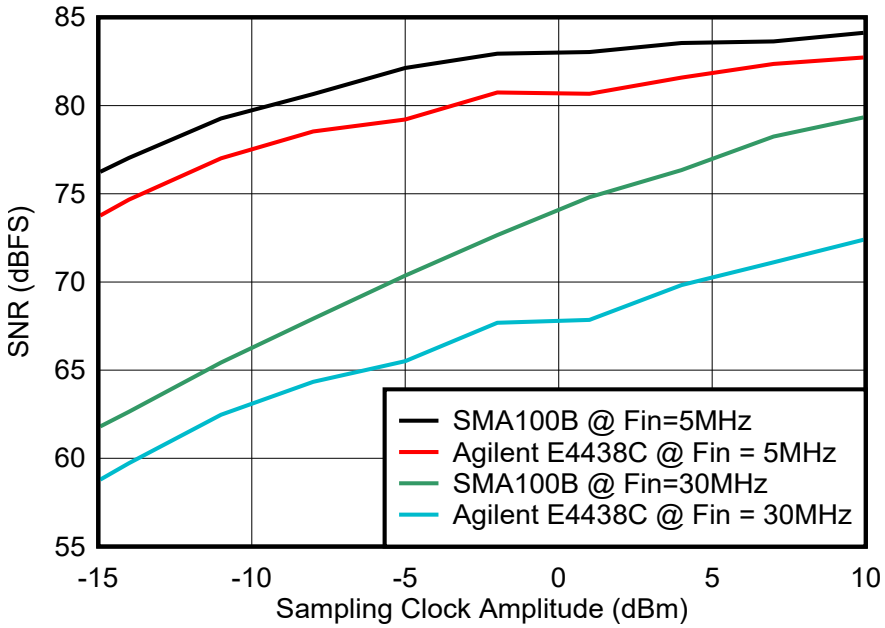

Figure 4-4. SNR vs. Sample Clock Amplitude (Slew Rate)

5 Understanding How to Apply Clocking Tradeoffs to Achieve the Desired ADC Performance

One of the bigger contributors to noise from a phase noise curve is the noise floor, otherwise known as broadband noise. If a source has a higher noise floor than another source, then the source with the higher noise floor increases the area under the phase noise curve, and as a result, increase the jitter value for a specified integration bandwidth.

In general, bandpass filters (BPF) lower the broadband noise of a clock signal or a signal source. BPF also help to inherently filter out an unwanted spurious, even at times generated by high-performance, low-noise signal generators. However, keep in mind that BPF can also lower the slew rate of a signal. Therefore, one needs to increase the clock signal relative to the loss of the filter to keep the slew rate high. Figure 5-1 shows the phase noise curves of three different signal generators phase noise plots with and without bandpass filtering applied. The bandpass filter used for the experiment was centered around 25MHz with a bandpass of 10%. Notice the improved performance drop in the broadband noise beyond 1MHz, which indicates that using a BPF generally results in a cleaner broadband, lower-jitter clock signal (while the clock slew rate degradation is not significant enough to affect the ADC performance).

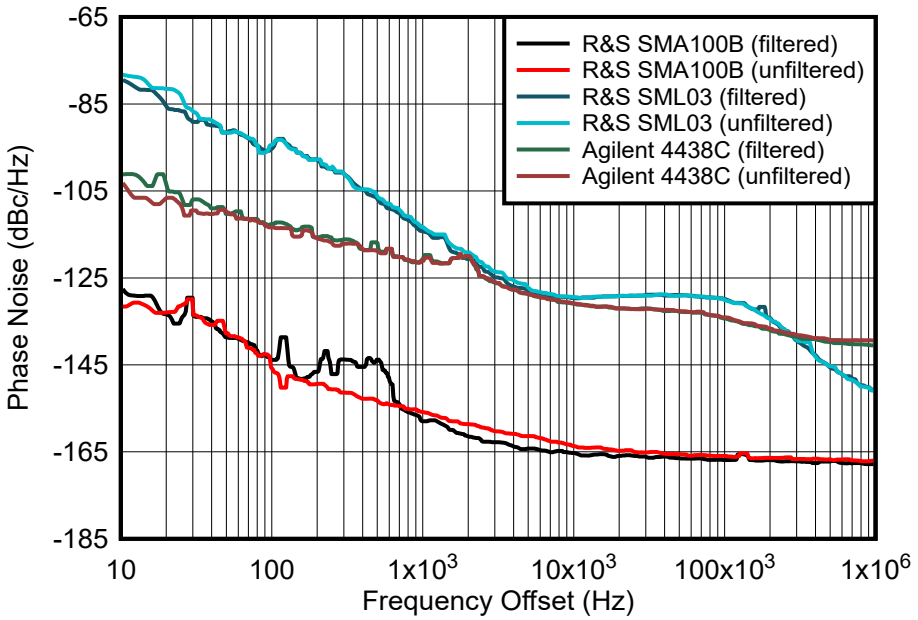

Figure 5-1. Phase Noise Curves of Different Signal Sources With and Without Filtering Applied

Looking at the filter example in a different way, Figure 5-2 demonstrates the ADC3683's SNR performance versus analog input frequency using these same three signal generators for the sampling clock, both when filtered and unfiltered. The SNR improvement is clearly seen when applying a filter on the output of the signal generator used for the clock. This is especially illustrated when applying a filter on a lower-performing signal generator with a higher noise floor, where the inherent phase noise is pretty poor to begin with.

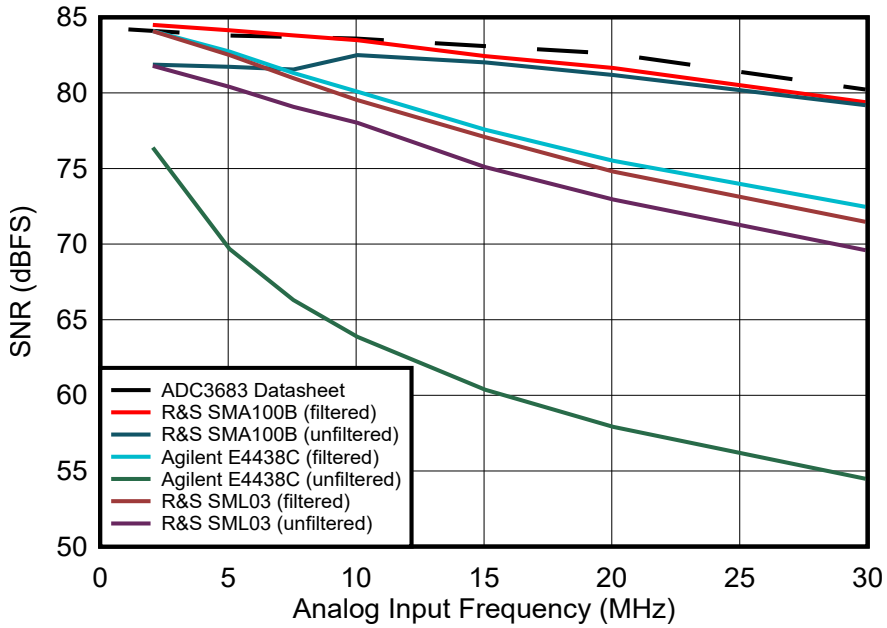

Figure 5-2. SNR of the ADC3683 When Filtering vs. no Filtering Applied With Different Clock Signal Sources

So far, signal generators have been used to demonstrate the various tradeoffs of clocking signals. However, in the real world, most designers choose a specific clocking device for an ADC design. In some cases, the designer wants to use an FPGA for the ADC sampling clock. However, this is not recommended. FPGA clock outputs have significant additive jitter as compared to most of TI clocking portfolio. Figure 5-3 illustrates the 25MHz phase noise curves of the FPGA output clock and the following TI clock products: LMX2572, LMK04832, LMX2571, CDCE6214, and the LMK3H0102. Figure 5-4 demonstrates the test setup used for the clocking devices. The phase noise curve of the FPGA clock (green curve) is worse as compared to any of the TI clocking devices shown, especially at the noise floor. Using an FPGA as an ADC sampling clock is not a good design choice and is not recommended if the converter's data sheet performance, or similar, is required. Keep in mind that TI clock devices' performance can range based on configuration, which directly affect the device's phase noise curve.

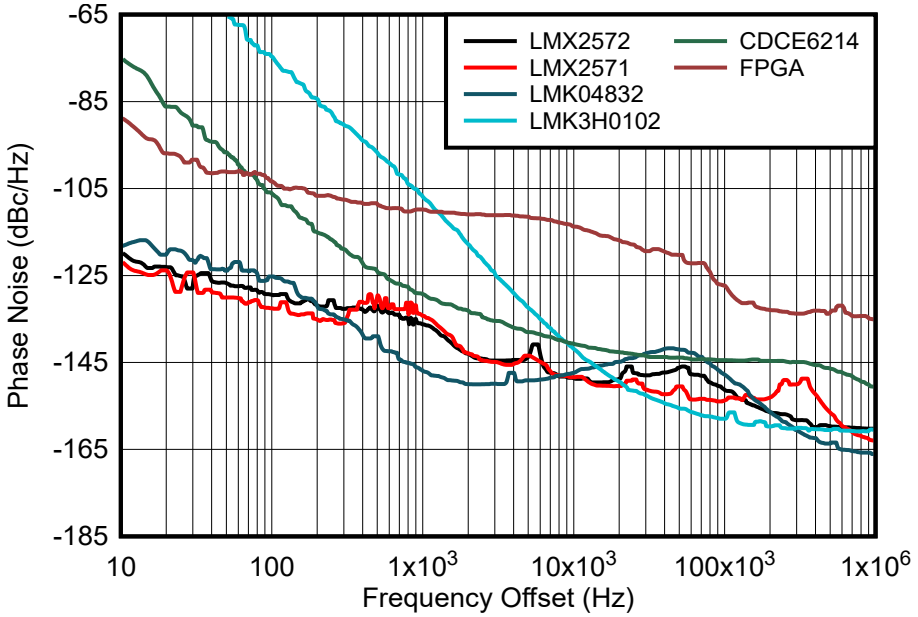

Figure 5-3. Phase Noise Curves of Several TI Clock Devices vs. a FPGA Output Clock

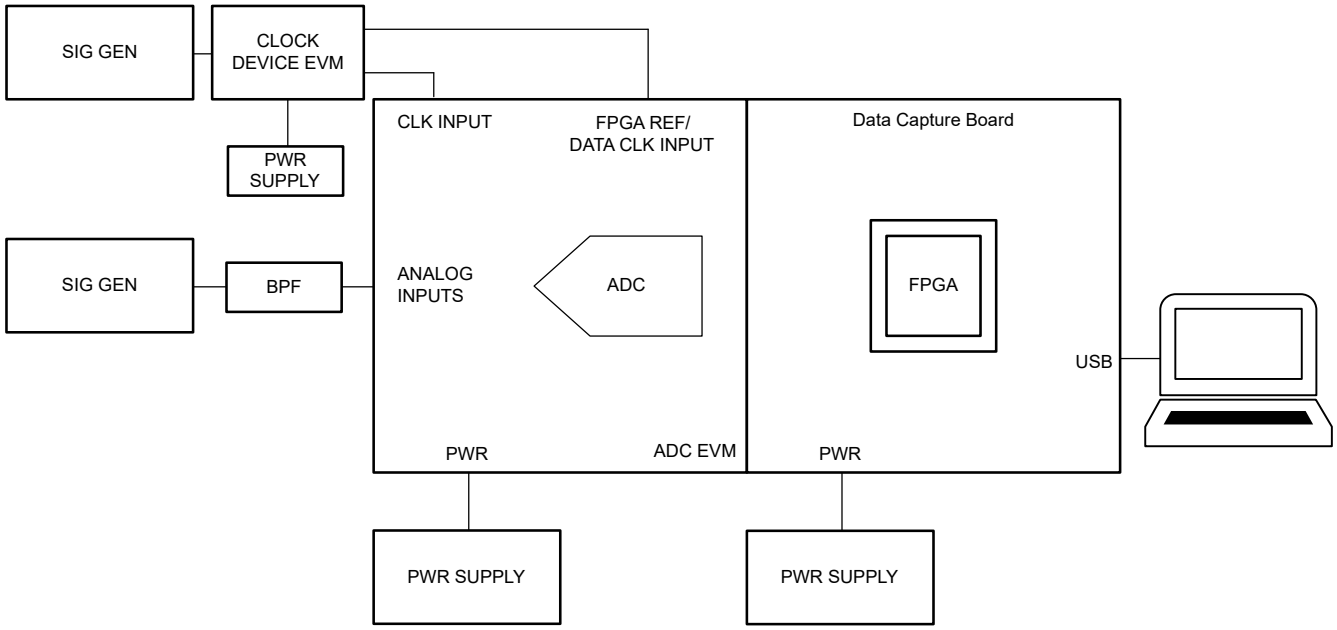

Figure 5-4. ADC With Clock Device Test Measurement Setup in the Lab

Figure 5-5 demonstrates the effect on the ADC SNR performance when clocking the ADC3683 with the FPGA output clock against the previously mentioned TI clocking devices. Figure 5-5 confirms that a clock source with a higher phase noise and noise floor can significantly affect the performance of a converter. To achieve the ADC3683's high SNR data sheet performance, the ADC was clocked with a passive device, for example, transformer or balun, instead of an active device, such as TI clocking parts or other. Using an active device further introduces noise and degrades the ADC performance. However, even though using passive devices results in best performance, passive devices are bigger, more expensive and don't have good *drive* capacity. This typically moves engineers away from using passive clock devices on their system design and instead leads them to choose an active clocking device that is good enough to meet the required performance. As previously mentioned, filtering can also be employed to the active clock design and can result in bettering the ADC performance. In this experiment however, this was not done because of the complexity of adding a BPF to P and N outputs due to extensive modifications that need to be completed either on board or off board.

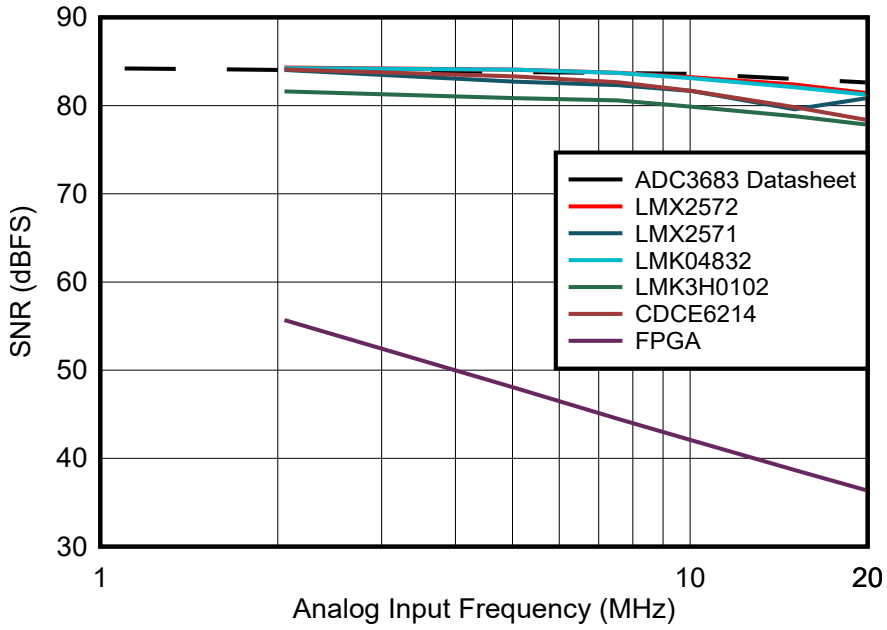

Figure 5-5. TI Clock Devices and FPGA Output Clock vs. ADC3683's Data Sheet SNR Across Analog input frequencies

Fast-rising signals with high slew rates,like LVPECL or CML interfaces also result in better ADC performance than an LVDS signal. Figure 5-6 illustrates the impact on SNR performance versus frequency for the ADC3683 when using a 25MHz sampling clock source with different output configurations, signaling standards, and a filtered analog input source. The clock device was configured and tested using a differential (DIFF) LVDS and LVPECL style interface and a single-ended (SE) LVCMOS style interface. Differential style interfaces are also primarily better since any common mode noise is inherently canceled. For more on differential vs. single-ended signals, see reference *SLLD009*. When the clock device was configured to output an LVCMOS signal, the ADC SNR decreased.

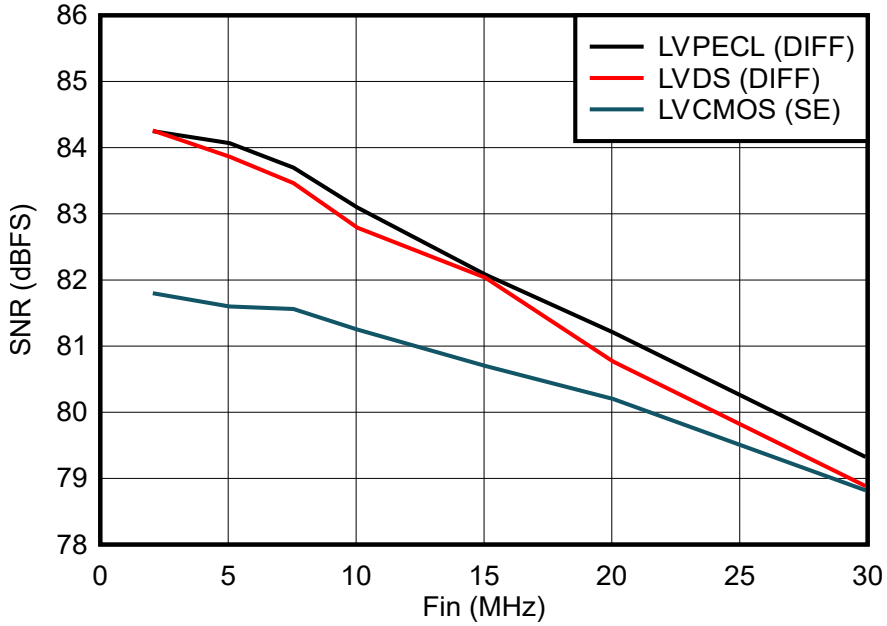

Figure 5-6. Clock Device Configured for Various Output Signaling Standards vs. ADC3683's SNR Performance Across Frequency

6 Summary

Providing a clean, high-slew rate clock source is paramount to maximizing the performance of any ADC, even though all the experimental cases shown in this paper were in the MSPS range. These fundamental points translate well when designing with GSPS ADC, or any high-speed ADC for that matter.

Understanding the difference between phase noise and jitter is also of utmost importance. Keep in mind, set the integration bandwidth upper limit to at least Fs, where 2×Fs is recommended, to capture the noise floor of the jitter contributed by the sampling clocking source. Another consideration is that the broadband noise floor is the largest noise contributor of the phase noise and/or jitter calculations. This quadrant of the phase noise curve has the largest impact on the ADC SNR performance.

Choosing a good, clean clock is paramount in achieving the ADC desired performance, especially since not all clock devices, oscillators, and signal sources are created equal. Filter the clock when appropriate to help knock down spurious and/or lower the broadband noise. However, there can be tradeoffs when using filters, since filters can decrease the clocking edge's slew rate, and this too can affect an ADC performance.

Stay away from FPGA clocks, These clocks are simple to design and implement as FPGA clocks make a good, low cost alternative. However, if maximizing the ADC SNR performance is a top requirement in your design, these clocks do not have the performance required to achieve said ADC data sheet performance.

Lastly, choosing the correct clocking interface is also important. Differential signaling is key in choking out common mode noise and interference on your clocking signals. So, go with a LVPECL or CML style interfaces for best slew signal quality rather than LVDS or single ended LVCMOS clocking signal interfaces.

Overall, if achieving maximum SNR performance of your next ADC design is of utmost importance, then use all these considerations before for your next ADC clocking design shows pitfalls and gives you the jitters.

7 References

- Texas Instruments, *Clock jitter analyzed in the time domain, Part 1*, analog engineers journal
- Texas Instruments, *Clock jitter analyzed in the time domain, Part 2*, analog engineers journal
- Texas Instruments, *Clock jitter analyzed in the time domain, Part 3*, analog engineers journal
- Texas Instruments, *LVDS Application and Data Handbook*.
- EE|Times, *Cut ADC Skewing Errors*.
- EE|Times, *Analogue to Digital Converter (ADC) Basics*.
- Planet Analog, *ADC Noise: How can the Clock Input Can Help*.
- EDN, *Understanding the effect of clock jitter on high-speed ADCs*.

Appendix A: Choosing a TI Clock Device Based on the TI High-Speed Converter Used

TI clocking portfolio ranges from a variety of parts that offer low power, low phase noise/jitter, and low cost. However, there are design tradeoffs to achieve the best performance, power, and cost on a single clocking device. High performing devices tend to draw more current and be more expensive, while lower power devices tend to be cheaper but not as high performing. Because of these trade-offs and ample clocking and high-speed converter portfolios, TI created Table 8-1 to guide you in selecting a clock for the high-speed converter your using. Keep in mind that these are general recommendations and the best clock device can vary depending on your specific application requirements. For personalized support, please post your application requirements on E2E.

Table 8-1. TI High-Speed Converter and TI Clock Pairings

High Speed Converter	Overall Best Clock Pairing		Clock Pairing Tradeoff by Priority (only for clock generation)			
	Clock generation	Clock distribution	Lowest Cost	Highest Performance	Lowest Power	Tradeoffs/Comments
ADC12xJ3200	When clocking or synchronizing multiple ADCs: **LMK04832** When clocking or synchronizing single ADC: **LMX2594**		**LMK04832**	**LMX2820**	**LMX2594**	**LMK04832:** higher power, bigger part, and has 14 total outputs **LMX2594:** more expensive but lower power, smaller part
ADC12xJ2700						
ADC12xJ1600						
ADC09xJ1300						
ADC09xJ800						
ADC12DJ5200RF	**LMX2820** or **LMX2594**	**LMX1204**	**LMX2594**	**LMX2820**	**LMX2594**	**LMX2594/LMX2820 + LMX1204** can be paired to create multiple copies of CLK and SYSREF at higher sampling frequencies
ADC35xx/ ADC36xx	For frequencies < 328MHz: **CDCE6214** For frequencies between 328MHz and 400MHz: **LMK3H0102** For frequencies between 400MHz and 500MHz: **CDCM6208**		**CDCE6214**	**LMK04832**	**CDCE6214**	**CDCE6214:** cheapest, small (4mm x 4mm) and lowest power (about 50mA) but can only output up to 328MHz **LMK3H0102:** smallest (3mm x 3mm), newer part, but second highest power (about 90mA) **CDCM6208:** third highest power (about 115mA), but versatile part and can output up to 800MHz **LMK04832:** highest power (about 350mA) and biggest size (9mm x 9mm) but results in best performance (about 10x better than other 3 parts)
AFE79xx	LMX2820 or **LMX2594**	**LMX1204**	**LMX2594**	**LMX2820**	**LMX2594**	**LMX2594** can be good enough for some applications and overall better clock pairing, but if performance is of utmost importance then the **LMX2820** needs to be used (with an external VCO to achieve the absolute best performance)
ADC3xRF5x/7x	**LMX2820** in external VCO mode			**LMX2820** in external VCO mode		
AFE8000	LMX2820 or **LMX2594**			**LMX2820**		
DAC39RF10	LMX2820 or **LMX2594**					
ADC39xx (8-bit)	**LMK6P**		**CDC6C**	**LMK6P**	**CDC6C**	**LMK6P:** best performance but slightly bigger (2.5mm x 2mm) and higher power (about 90mA) **CDC6C:** smaller (1.2mm x 1.6mm) and lower power (about 6mA) but worse performance
ADC39xx (10-bit)	**CDCE6214**		**LMK3H0102**	**CDCE6214**	**CDCE6214**	** Same tradeoffs as the ADC35xx/ ADC36xx family
ADC3669	**LMX2571**		**CDCE6214**	**LMX2571**	**CDCE6214**	**LMX2571:** better performance, comparable in power (about 55mA) and bigger (6mm x 6mm) **CDCE6214:** cheaper, smaller (4mm x 4mm), and slightly lower power (about 50mA) but worse performance

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265