

LAN and WAN Clock Generation and Muxing Using the CDCE62005

Firoj Kabir / Johnny Lau
Clock Distribution Circuits

ABSTRACT

This application note is a guide for using Texas Instruments CDCE62005 in a LAN/WAN application as a clock distributor and clock synthesizer along with measured jitter performance results. In addition, several examples are given to show the flexibility of the CDCE62005 generating the most common frequencies used in various networking applications today.

Contents

1	Background.....	2
2	Functional Description	2
3	Application	3
4	Test Equipment, Setup, and Measured Results	4
5	Test Equipment and Setup	6
	5.1 Configuration #1 Phase Noise Plot Results	7
	5.2 Configuration #2 Phase Noise Plot Results	13
	5.3 Configuration #3 Phase Noise Plot Results	20
	5.4 Configuration #4 Phase Noise Plot Results	25
6	Performance Summary	30
	6.1 Configuration #1.....	30
	6.2 Configuration #2.....	30
	6.3 Configuration #3.....	30
	6.4 Configuration #4.....	31
7	Conclusion	31

List of Figures

1	CDCE62005 Functional Block Diagram	3
2	Setup Configuration # 1.....	4
3	Setup Configuration # 2.....	4
4	Setup Configuration # 3.....	5
5	Setup Configuration # 4.....	5
6	Setup Configuration # 1.....	6
7	TI GUI Setup Configuration # 1	6
8	Setup Configuration # 2	12
9	TI GUI Setup Configuration # 2	12
10	Setup Configuration # 3	18
11	TI GUI Setup Configuration # 3 – CDCE62005 #1	18
12	TI GUI Setup Configuration # 3 – CDCE62005 #2	19
13	Setup Configuration # 4	24
14	TI GUI Setup Configuration # 4	24

1 Background

Networking equipment frequently has a need for clock muxing different frequencies to meet a given system application. Traditional methods involved 2 different clock oscillators and a clock mux device. For LAN applications, a typical 156.25 MHz clock is needed, and for WAN applications a 155.52 MHz clock is used. Due to the low jitter and accuracy needed for these clock oscillators, the cost of these oscillators may be high. To obtain lower cost but maintain the low jitter, high accuracy, and clock muxing in a single solution, the CDCE62005 can be used.

2 Functional Description

The CDCE62005 is a high performance low phase noise clock synthesizer with five universal output buffers that can be configured individually to be LVPECL, LVDS or LVCMOS. Each of the 5 universal differential outputs can be converted to two LVCMOS outputs for a total of 10 LVCMOS outputs. It has two fully integrated low noise LC based Voltage Controlled Oscillators (VCOs) which operates in the 1.750 GHz -2.356 GHz range. The VCO Core output frequency is proportional to the frequency of the VCO core input, the pre-scaler divider, feedback divider, output divider and VCO selection. Each output has an independent Output Divider and each output can be sourced from the Primary Input, Secondary Input, Smart Mux Output, or the Output of the Integrated VCO Core. Another unique feature is the output phase adjust. All device settings are programmable through a SPI serial interface and the CDCE62005 contains an integrated EEPROM to store all user settings for use on power on default settings.

For more details refer to the application note, *Using the CDCE62005 as a Frequency Synthesizer ..*

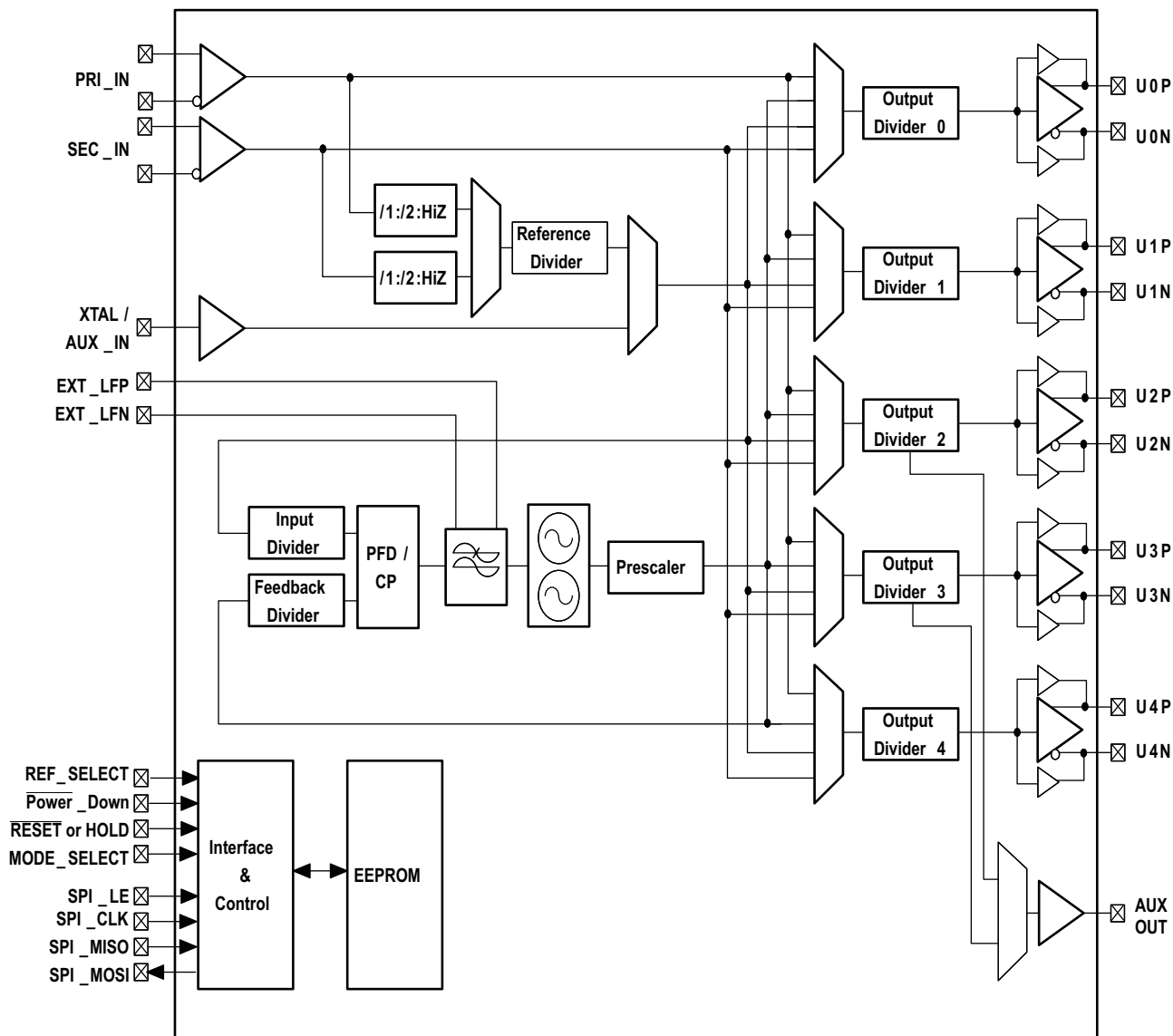


Figure 1. CDCE62005 Functional Block Diagram

3 Application

Networking LAN and WAN clocking needs require low jitter (typ < 1ps rms or lower). Typical clock speeds for LAN applications are 625 MHz, 312.5 MHz, 156.25 MHz, 125 MHz, and 25 MHz. For WAN applications 622.08 MHz, 311.04 MHz, 155.52 MHz, 77.76 MHz, and 19.44 MHz are commonly used. For both LAN and WAN systems, the output signal type needed can be differential (LVPECL or LVDS) or single ended 3.3V LVCMOS. This application report demonstrates 4 solutions that can meet these needs while also offering a lower cost solution to oscillators and clock muxes.

4 Test Equipment, Setup, and Measured Results

1. A solution on how to generate networking LAN clocks from a single CDCE62005 device and a low cost crystal is provided in [Figure 2](#).

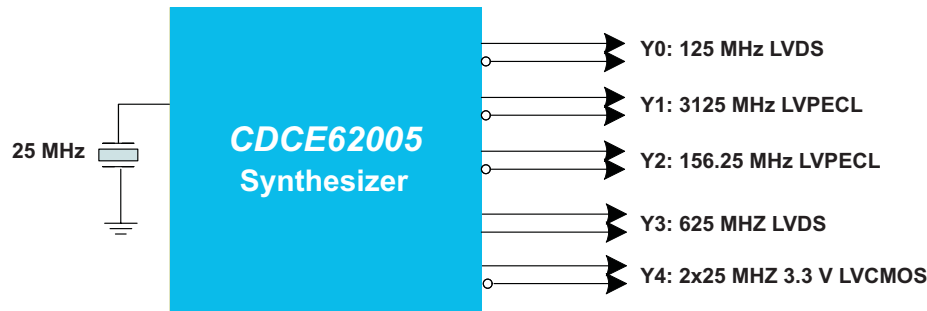


Figure 2. Setup Configuration # 1

[Figure 2](#) uses a standard 25 MHz crystal connected to the CDCE62005 auxiliary input. The 25 MHz is then fed into the CDCE62005 VCO core to generate a 625 MHz frequency available to all five output muxes. From there post dividers can be used to output 625 MHz, 312.5 MHz, 156.25 MHz, 125 MHz, and 25 MHz. The output signal type can be native LVPECL, LVDS, or LVCMOS; and can be mixed to avoid use of external components to accomplish signal type translation. This example selects all three types to show the flexibility of the CDCE62005 output buffers. For every differential output, 2 LVCMOS signals can take its place as shown. In the above example, the CDCE62005 outputs 4 differential signals and 2 LVCMOS signals.

2. Second is a solution on how to generate networking WAN clocks from a single CDCE62005 device and a low cost crystal.

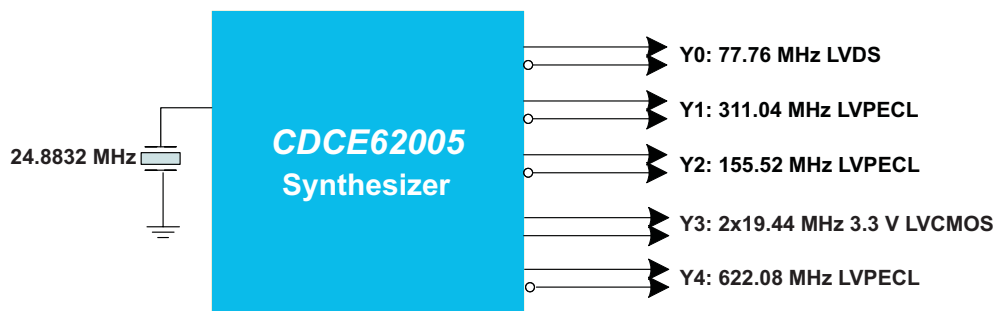


Figure 3. Setup Configuration # 2

[Figure 3](#) uses a standard 24.8832 MHz crystal connected to the CDCE62005 auxiliary input. The 24.8832 MHz is then feed into the CDCE62005 VCO core to generate a 622.08 MHz frequency available to all five output muxes. From there post dividers can be used to output 622.08 MHz, 311.04 MHz, 155.52 MHz, 77.76 MHz, and 19.44 MHz. The output signal type can be native LVPECL, LVDS, or LVCMOS; and can be mixed to avoid use of external components to accomplish signal type translation. Again, this example selects all three types to show the flexibility of the CDCE62005 output buffers. It should also be noted that a standard 19.44 MHz crystal can used instead of 24.8832 MHz crystal to generate above mentioned frequencies.

3. Third is a solution that requires both LAN and WAN clock and that all outputs be frequency selectable using software to control the output clock muxing. For simplicity, lets limit the frequencies to 156.25 MHz and 155.56 MHz that are commonly used in 10G networking designs. It should be noted that any of the frequencies in example 1 or 2 are also possible if needed.

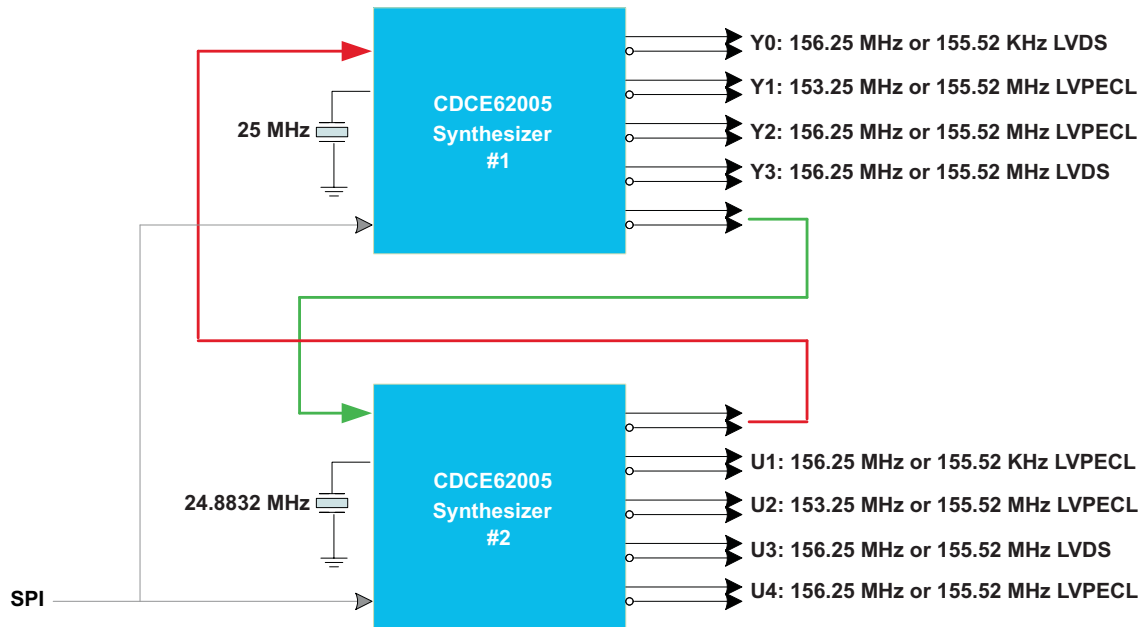


Figure 4. Setup Configuration # 3

Figure 4 uses two CDCE62005. One is to generate the 156.25 MHz and the other to generate 155.52 MHz. One output of each device is then connected back into the Primary Input of the other device. This allows a total of 8 usable output buffers that can be software selectable over SPI to be either 156.25 MHz or 155.52 MHz.

4. This last example demonstrates the flexibility of all 3 inputs of the CDCE62005 and it is not limited to only networking application.

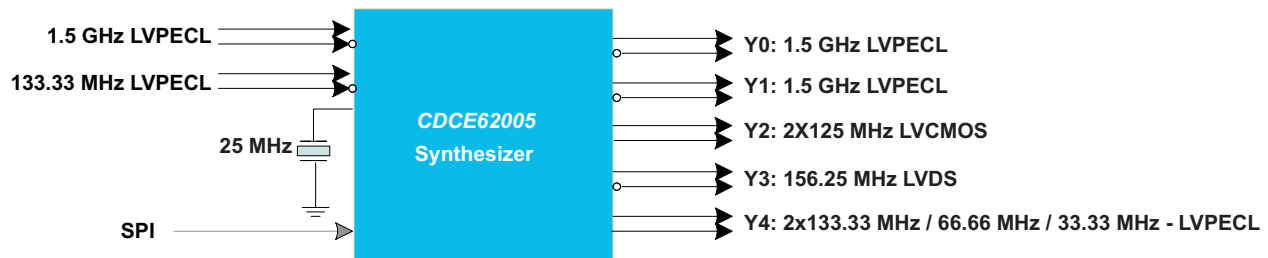


Figure 5. Setup Configuration # 4

Figure 5 uses a 1.5 GHz differential clock that is feed in the CDCE62005 Primary Input, a 133.33 MHz differential clock feed into the Secondary Input, and finally a 25 MHz crystal that is feed into the Auxiliary Input. Both the Primary and Secondary inputs can be either differential or single ended while the Auxiliary input can be a crystal or single ended input only. The setup for the example above uses a 25 MHz crystal input to feed the CDCE62005 VCO core and generates a 625 MHz frequency available to all five output muxes. From there post dividers can be used to output 156.25 MHz on Y3 and 125 MHz on Y2. The 1.5 GHz LVPECL input at the Primary is then feed to same output muxes and is available on all output but Y0 and Y1 have been selected for this example. The 133.33 MHz on the Secondary input is also feed to all the output muxes and is used on output Y4 for this example. Note that the user can use the post dividers on Y4 to get 133.33 MHz (/1), 66.66 MHz (/2), or 33.33 MHz (/4). The outputs can be software selected or the internal EEPROM can be programmed to contain the configuration so that at power-up it will default to the example above without the need for software interaction.

5 Test Equipment and Setup

All measurements discussed in this application report were taken under nominal operating conditions using a 3.3-V power supply and at room temperature.

Equipment used:

- Agilent E5052A Signal Source Analyzer
- Power supply
- Signal Generators
- CDCE62005 Evaluation modules and GUI

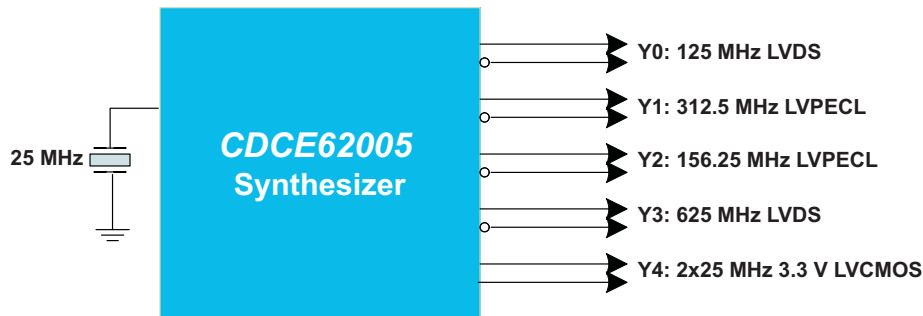


Figure 6. Setup Configuration # 1

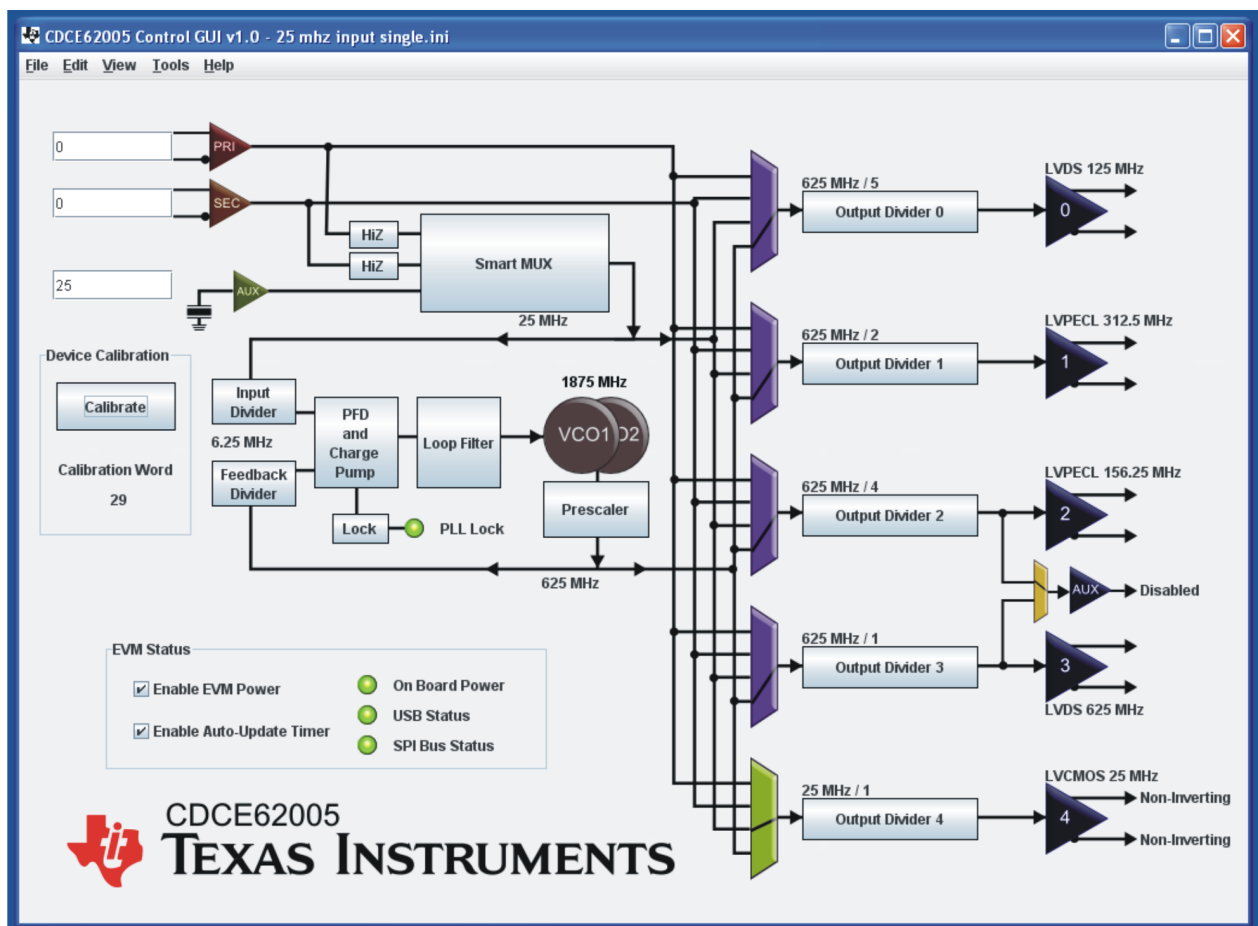
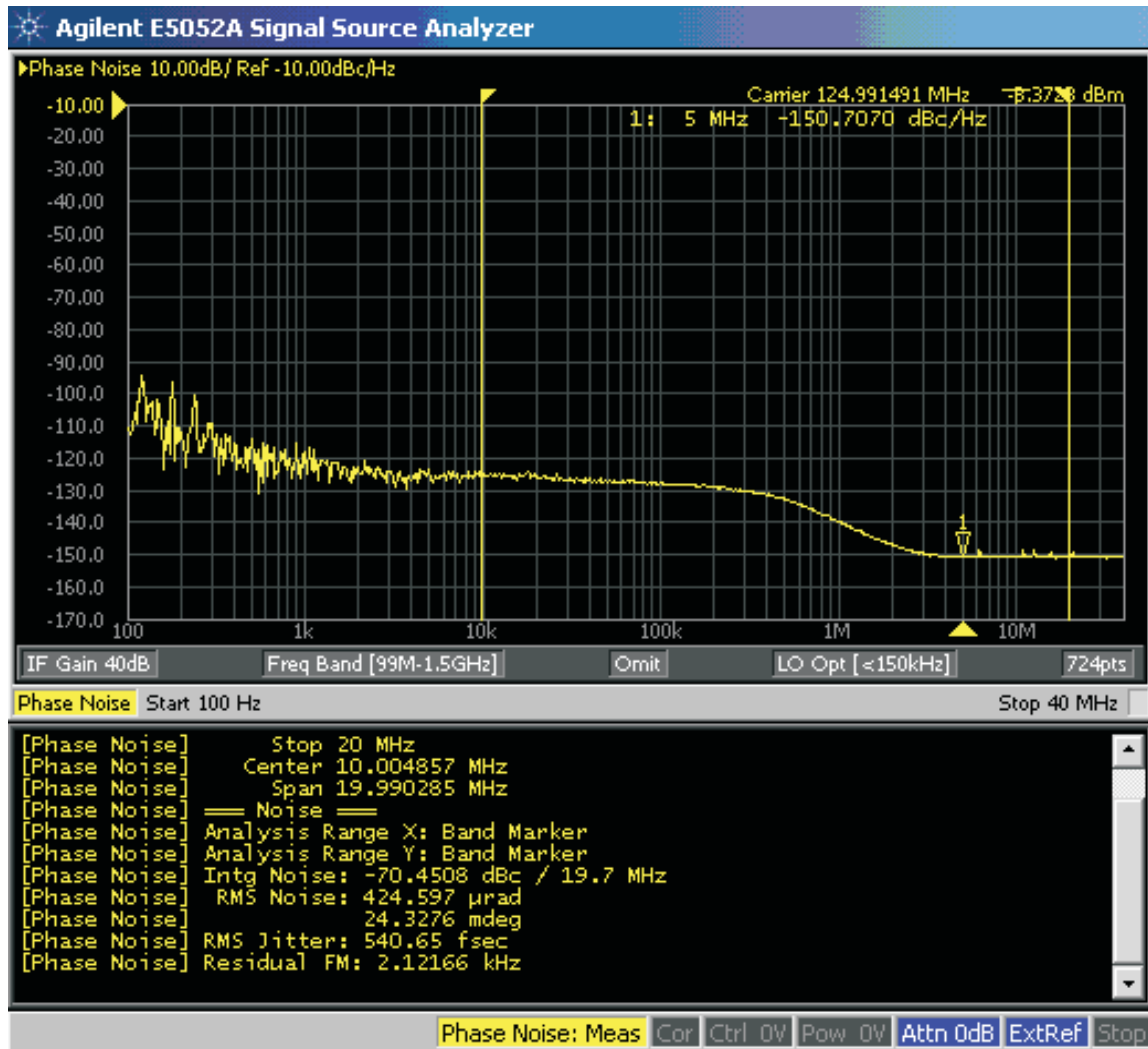


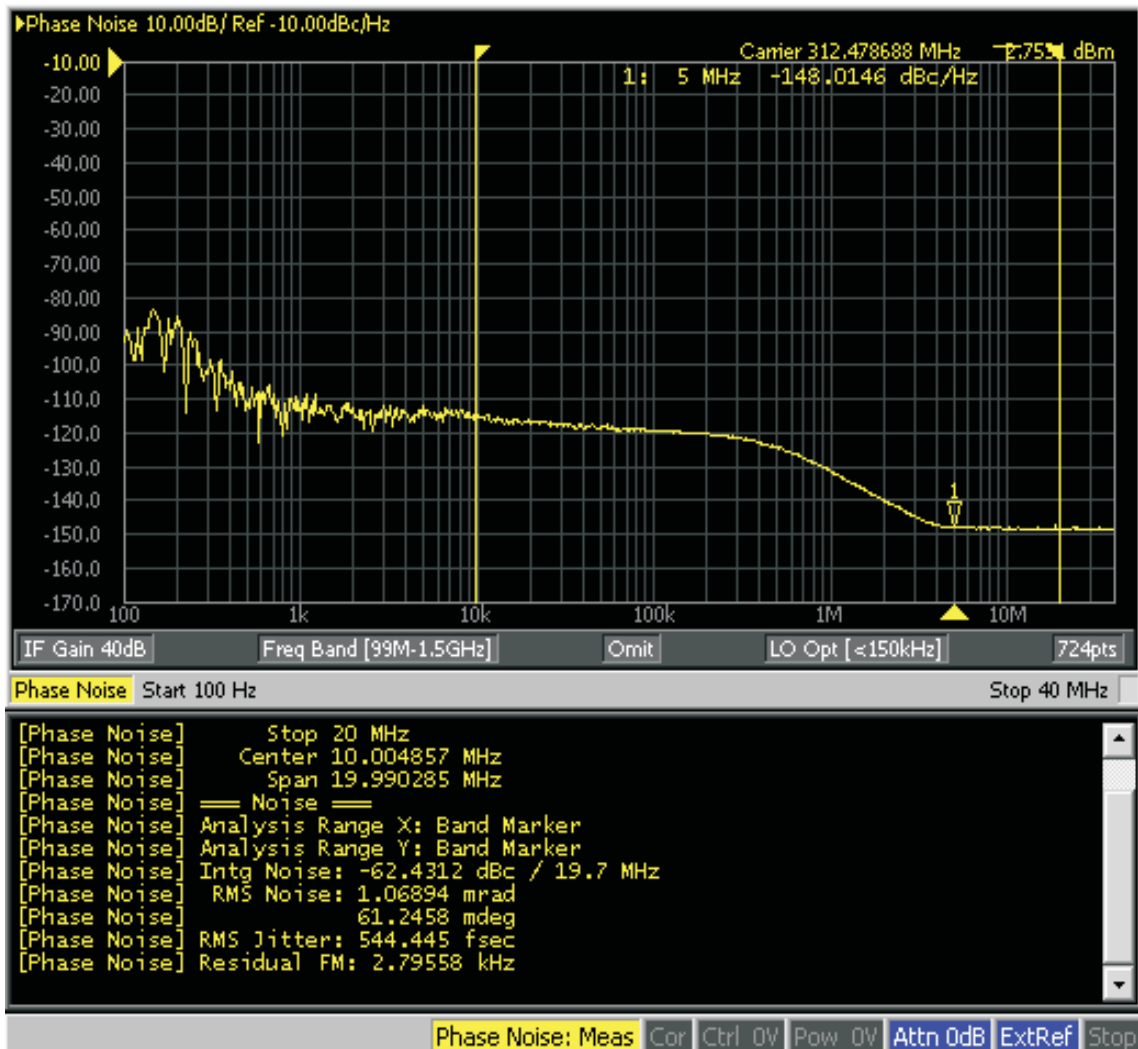
Figure 7. TI GUI Setup Configuration # 1

5.1 Configuration #1 Phase Noise Plot Results

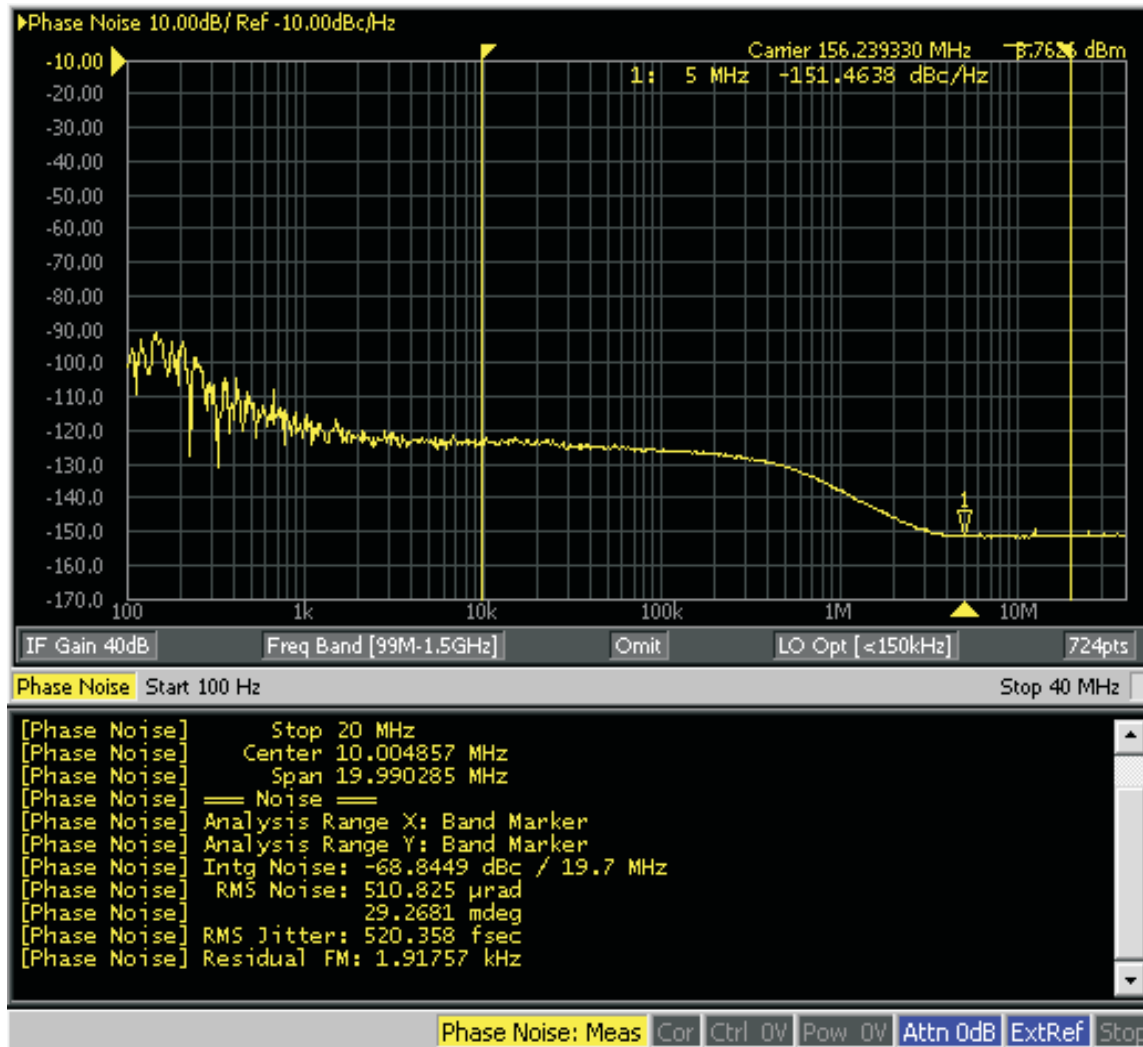
5.1.1 Y0 = 125 MHz LVDS – RMS Jitter is 540 fsec (10 kHz – 20 MHz)



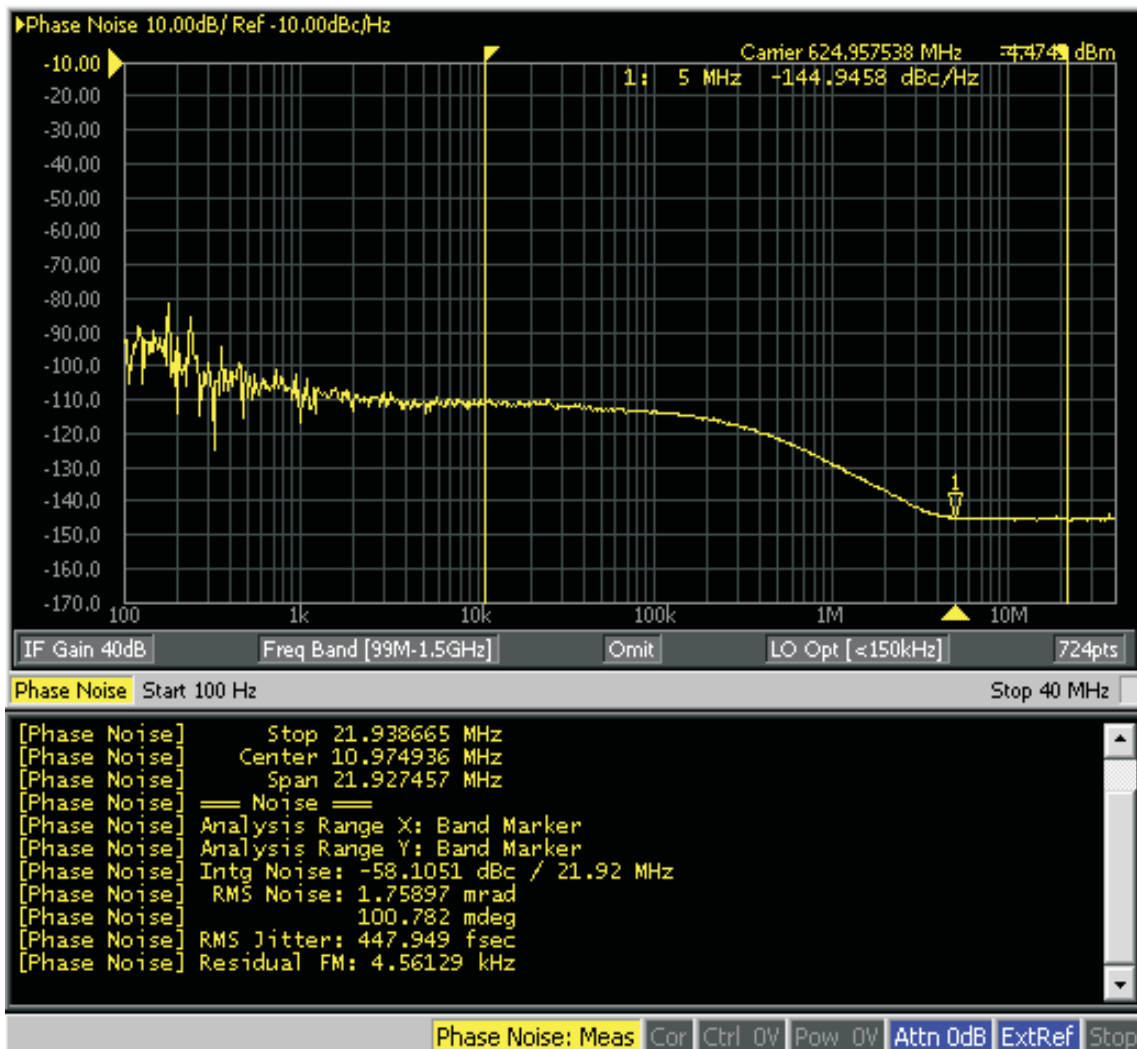
5.1.2 Y1 = 312.5 MHz LVPECL – RMS Jitter is 544 fsec (10 kHz – 20 MHz)



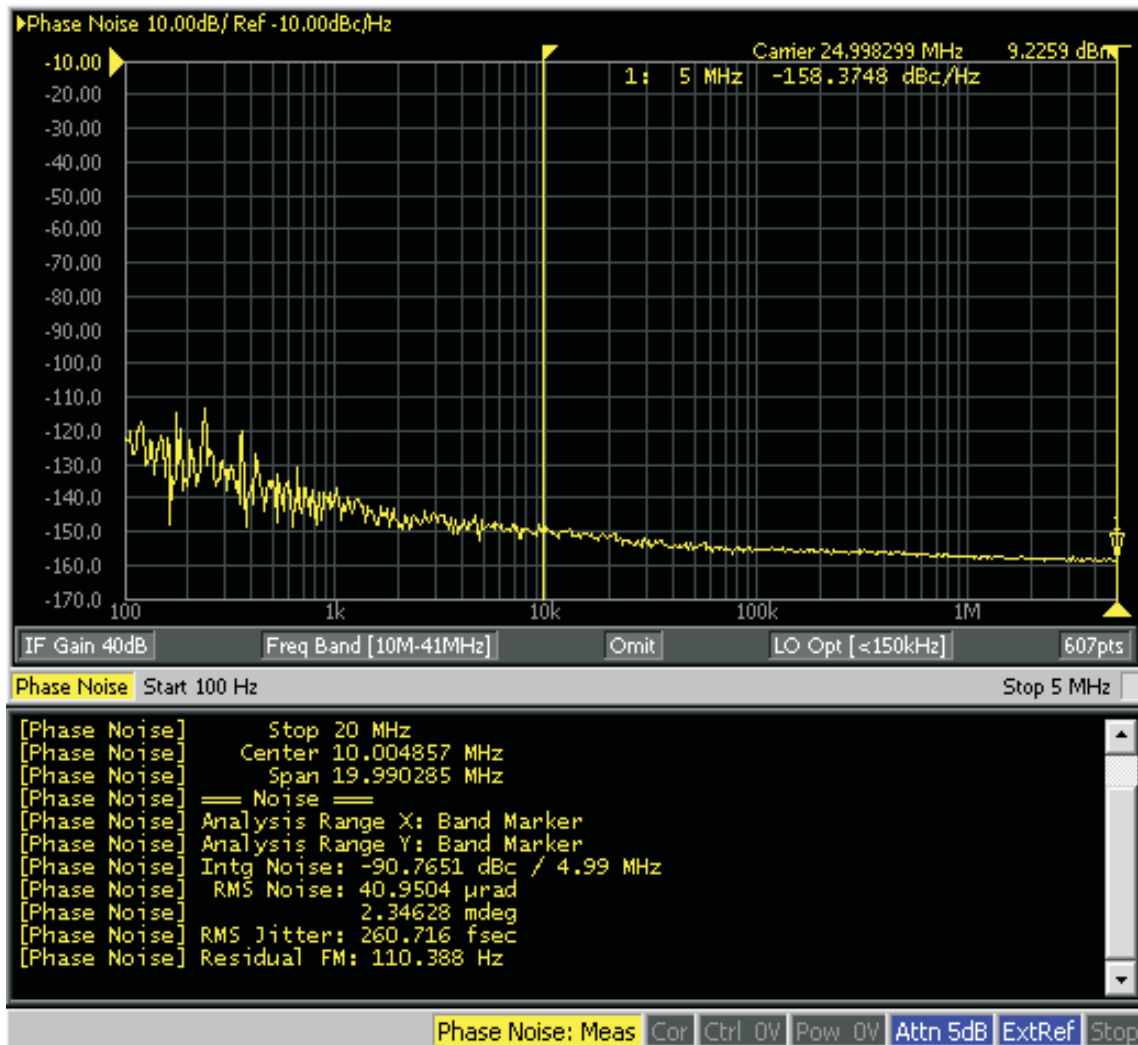
5.1.3 Y2 = 156.25 MHz LVPECL – RMS Jitter is 520 fsec (10 kHz – 20 MHz)



5.1.4 Y3 = 625 MHz LVPECL – RMS Jitter is 448 fsec (10 kHz – 20 MHz)



5.1.5 Y4 = 25 MHz LVCMOS – RMS Jitter is 261 fsec (10 kHz – 5 MHz)



This 25 MHz clock output is directly from the 25 MHz crystal.

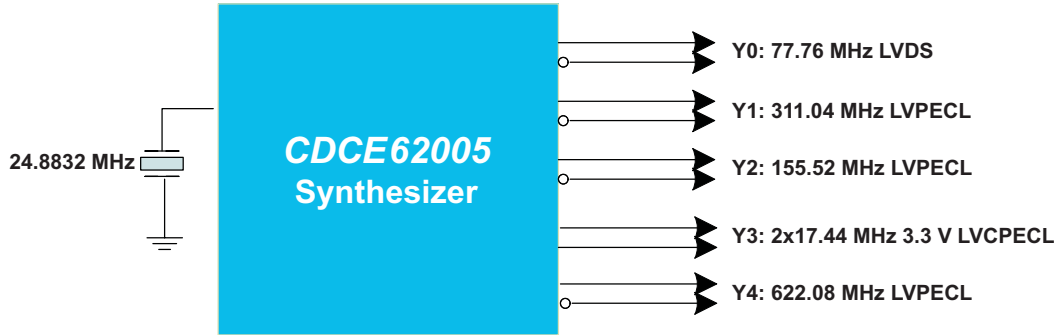


Figure 8. Setup Configuration # 2

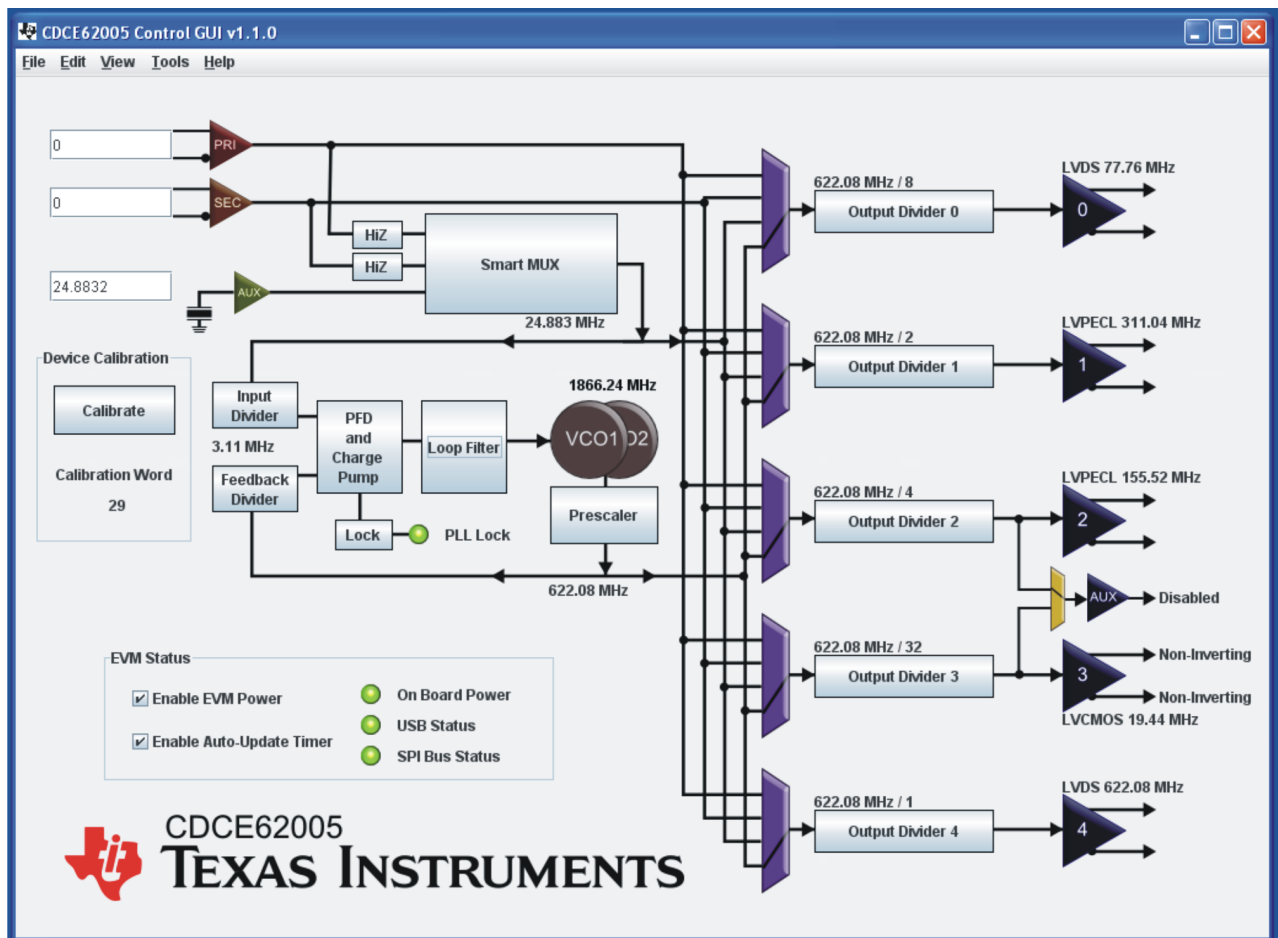
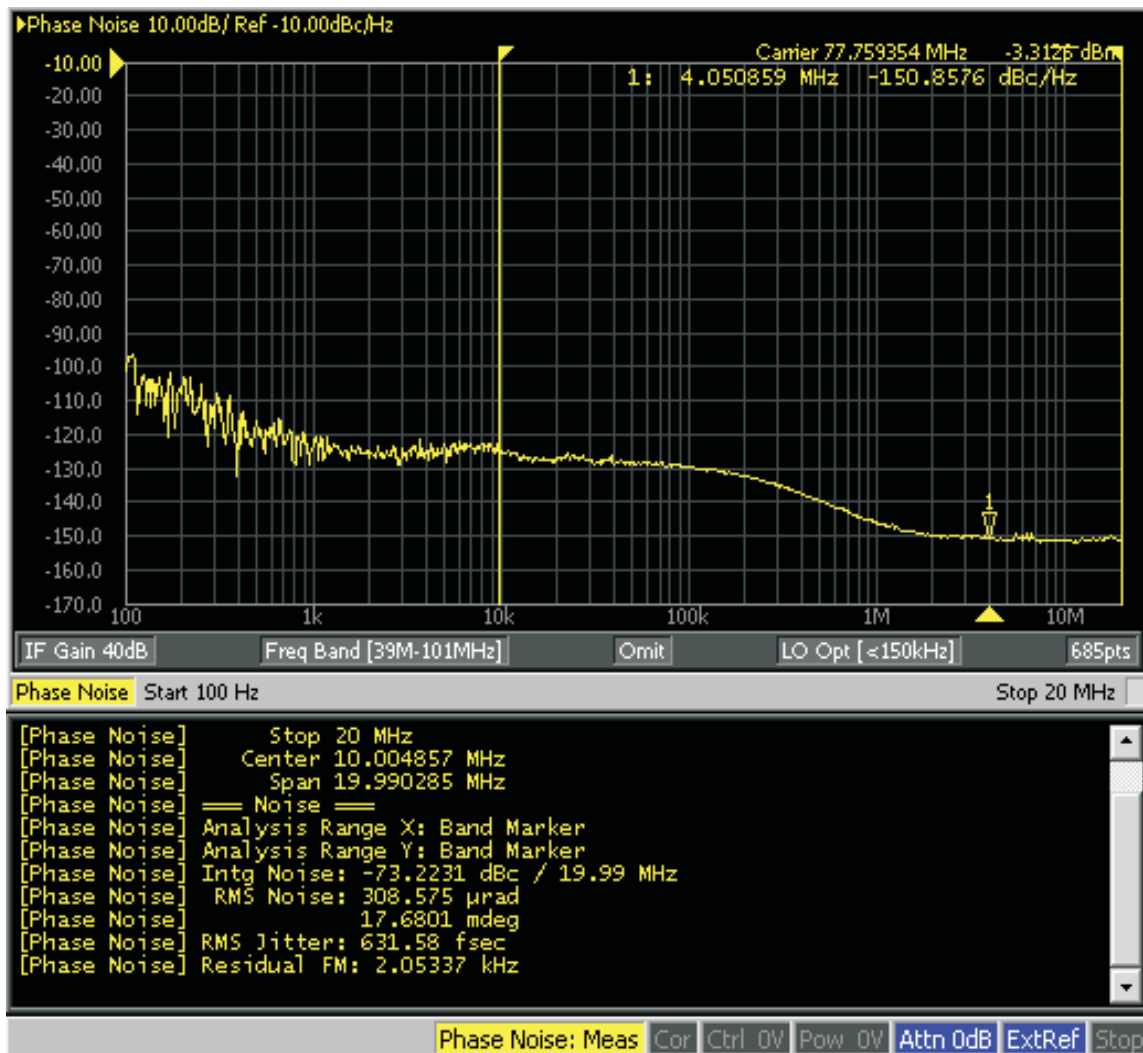


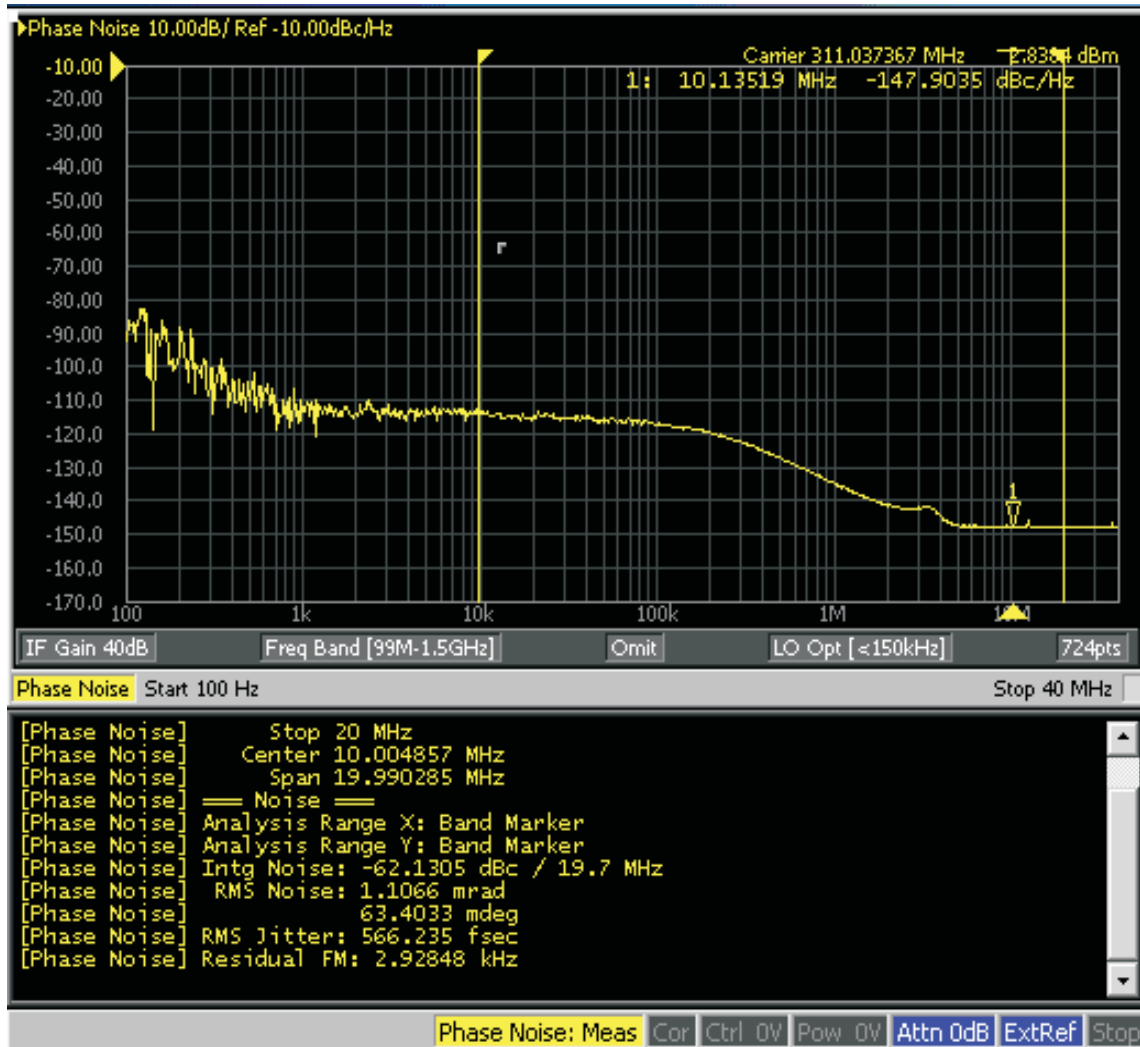
Figure 9. TI GUI Setup Configuration # 2

5.2 Configuration #2 Phase Noise Plot Results

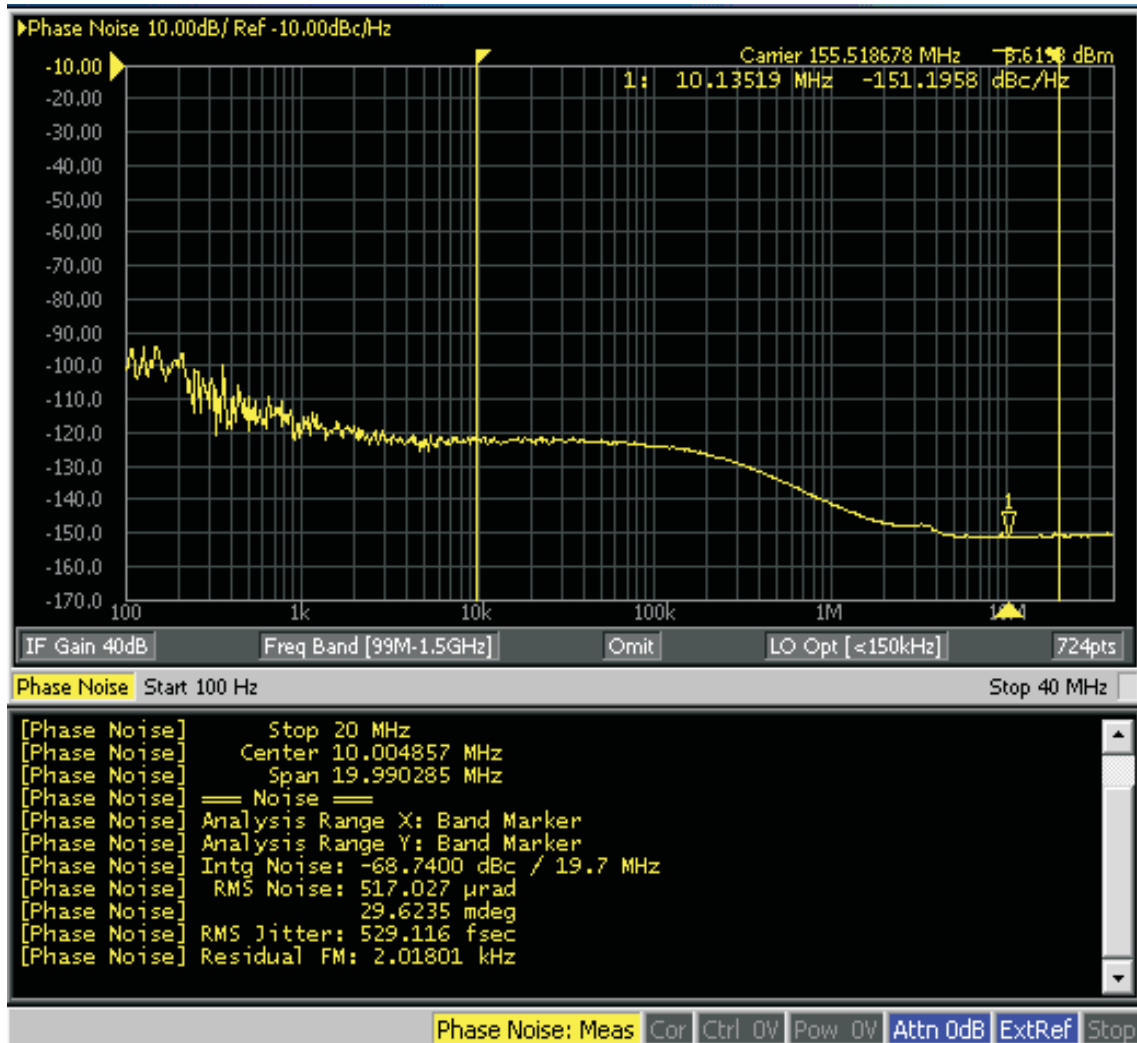
5.2.1 Y0 = 77.76 MHz LVDS – RMS Jitter is 631 fsec (10 kHz – 20 MHz)



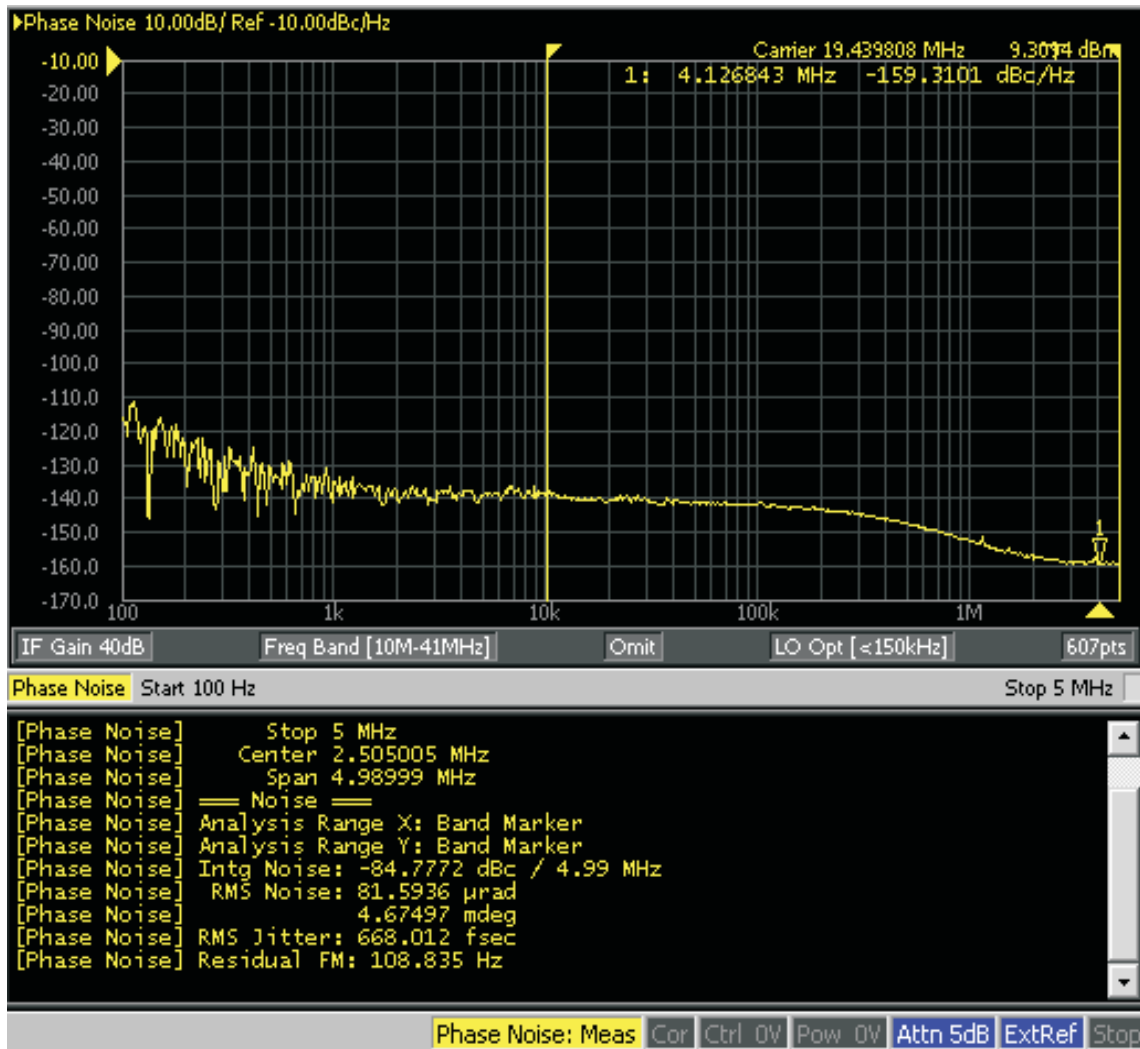
5.2.2 Y1 = 311.04 MHz LVPECL – RMS Jitter is 566 fsec (1 kHz – 20 MHz)



5.2.3 Y2 = 155.52 MHz LVPECL – RMS Jitter is 529 fsec (10 kHz – 20 MHz)



5.2.4 Y3 = 19.44 MHz LVCMOS – RMS Jitter is 668 fsec (10 kHz – 5 MHz)



5.2.5 Y4 = 622.08 MHz LVPECL – RMS Jitter is 550 fsec (10 kHz – 20 MHz)



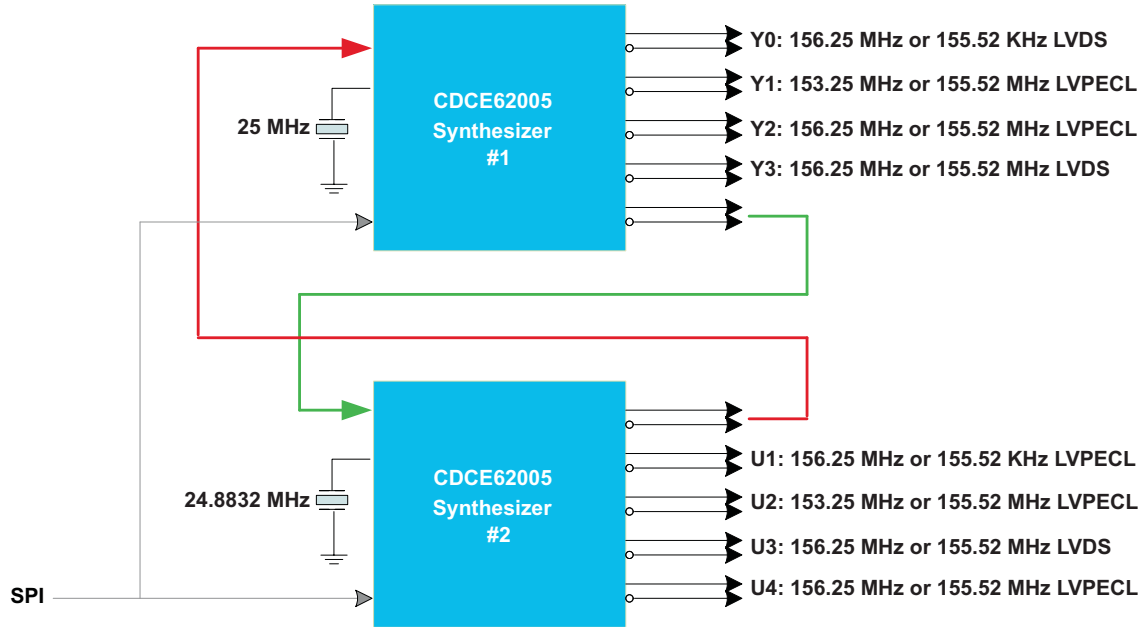


Figure 10. Setup Configuration # 3

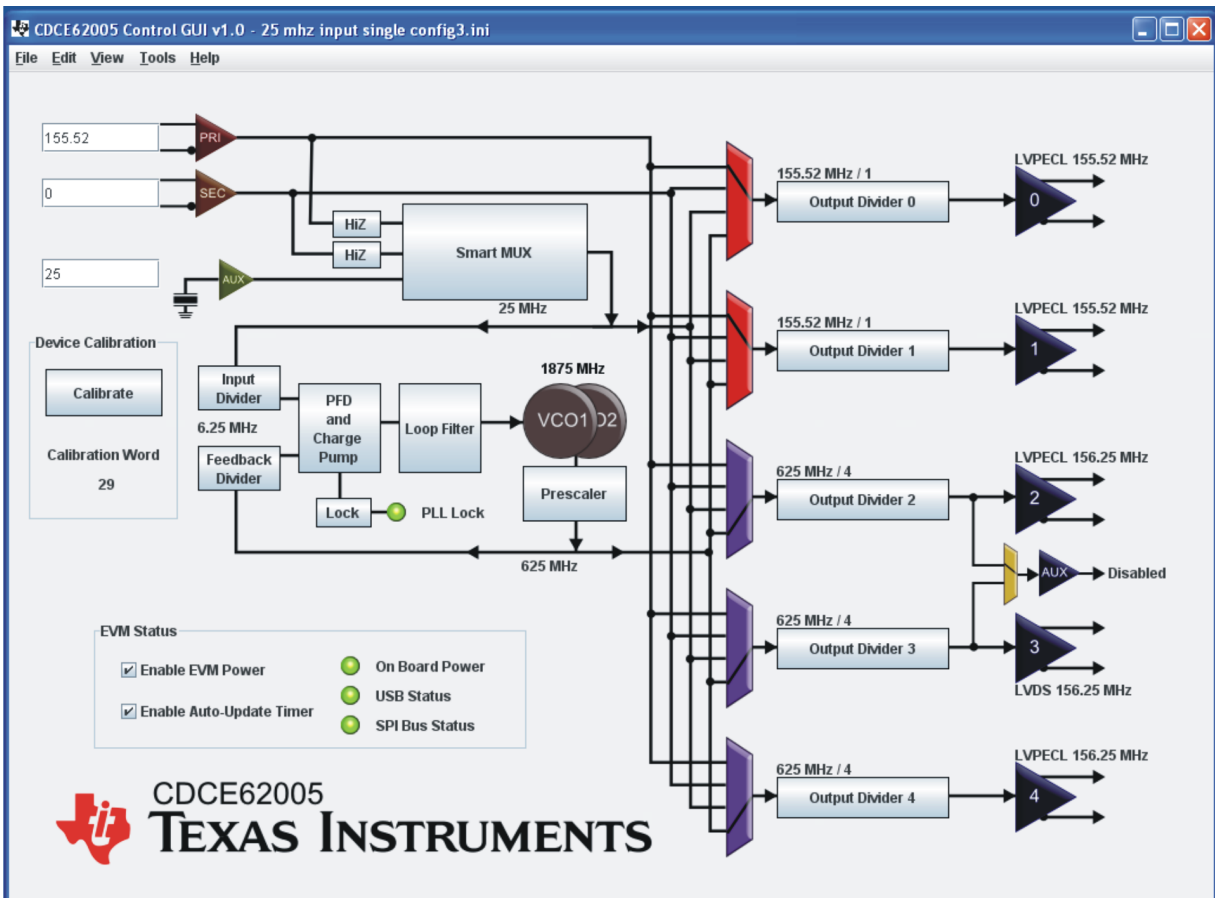


Figure 11. TI GUI Setup Configuration # 3 – CDCE62005 #1

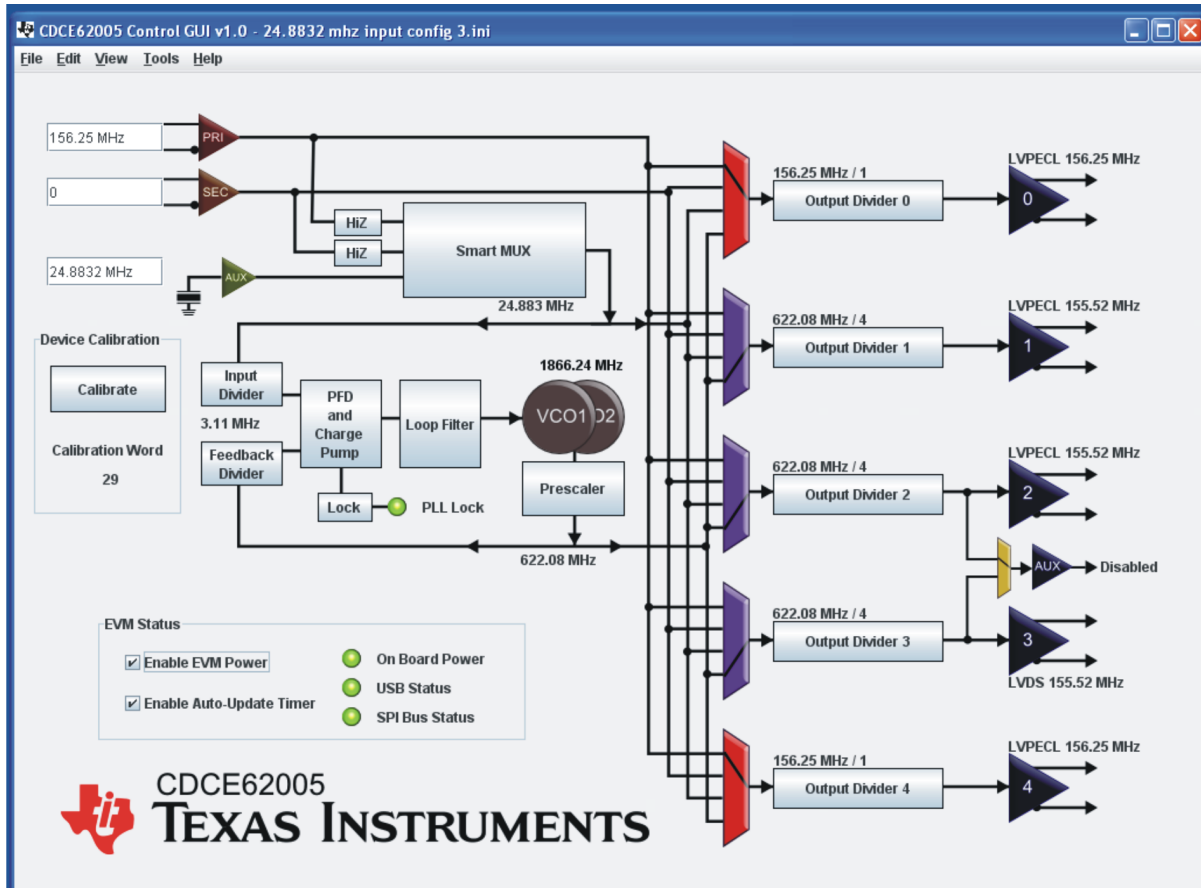
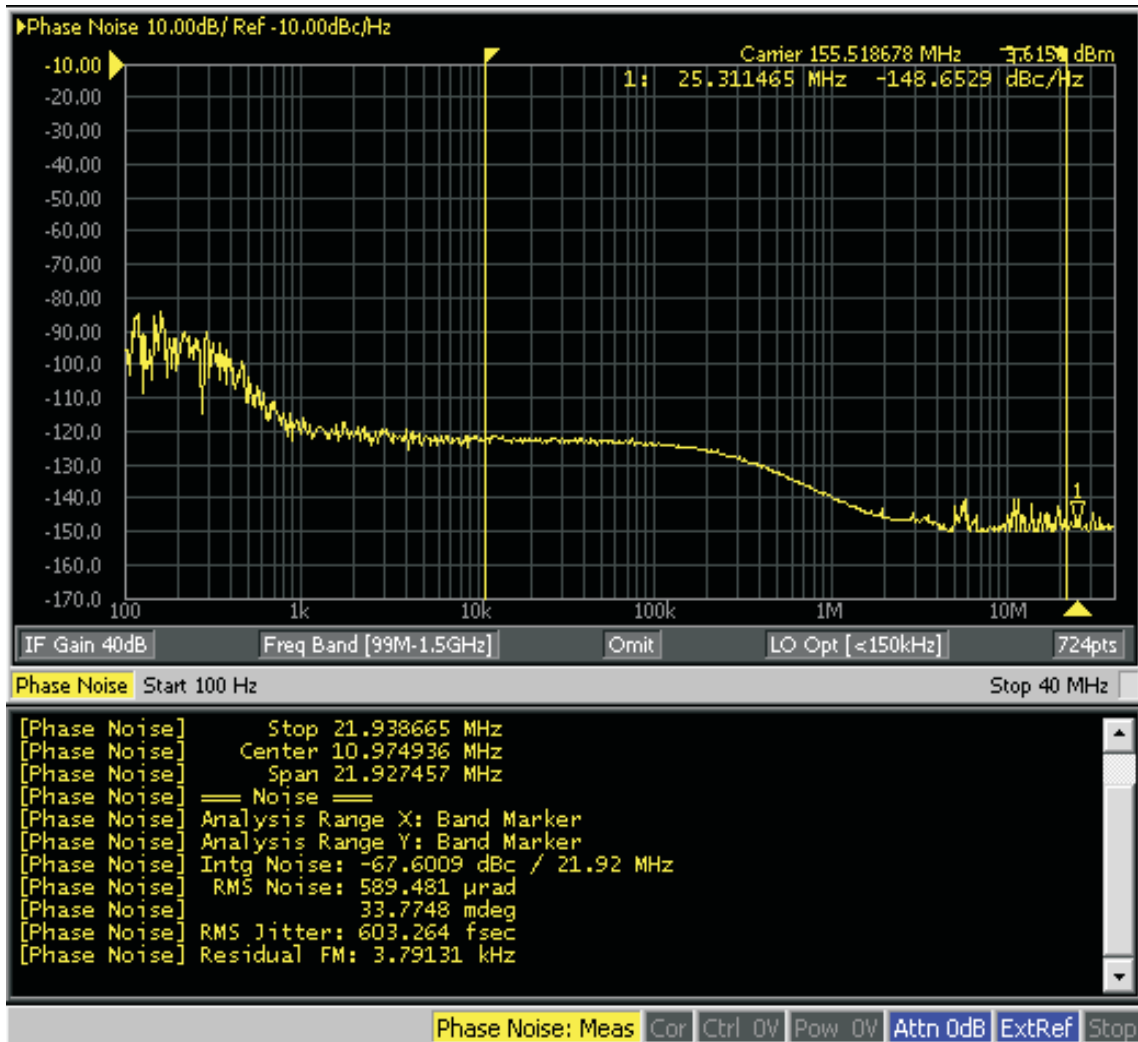


Figure 12. TI GUI Setup Configuration # 3 – CDCE62005 #2

5.3 Configuration #3 Phase Noise Plot Results

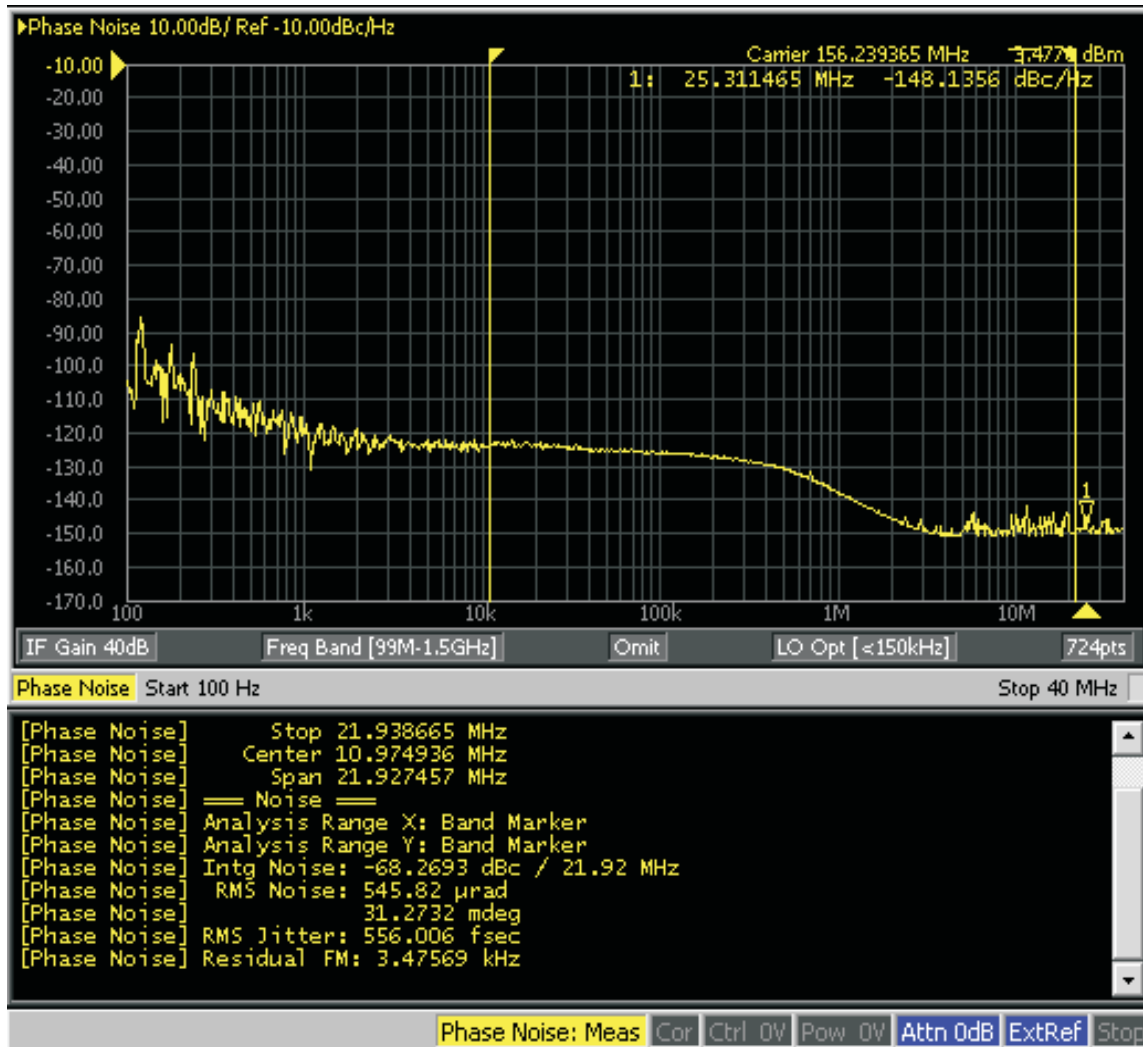
5.3.1 Device #1 - Y0 = 155.52 MHz LVPECL – RMS Jitter is 603 fsec (10 kHz – 20 MHz)



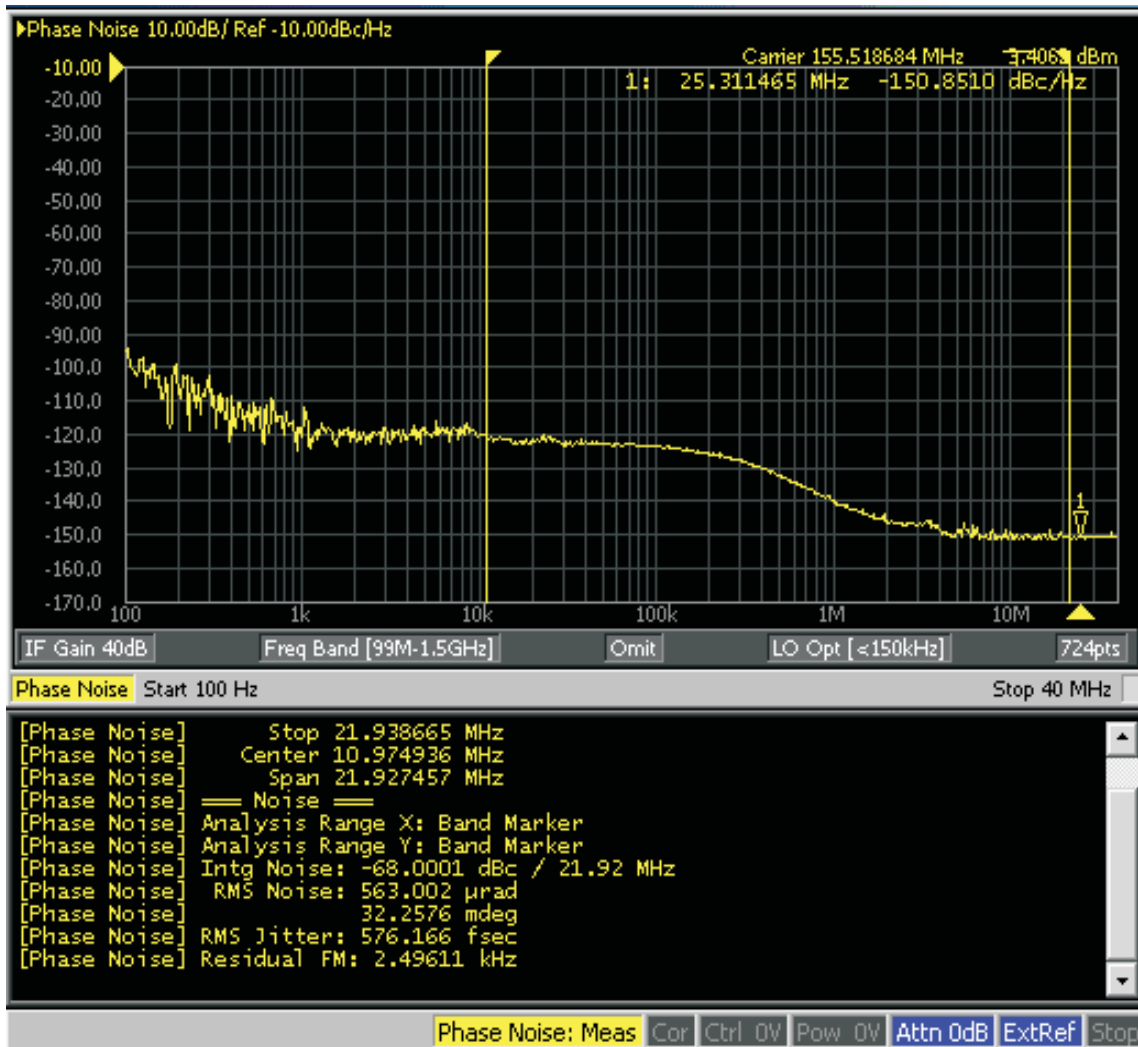
5.3.2 Device #1 - Y0 = 156.25 MHz LVPECL – RMS Jitter is 522 fsec (10 kHz – 20 MHz)



5.3.3 Device #2 - U1 = 156.25 MHz LVPECL – RMS Jitter is 556 fsec (10 kHz – 20 MHz)



5.3.4 Device #2 - U1 = 155.52 MHz LVPECL – RMS Jitter is 576 fsec (10 kHz – 20 MHz)



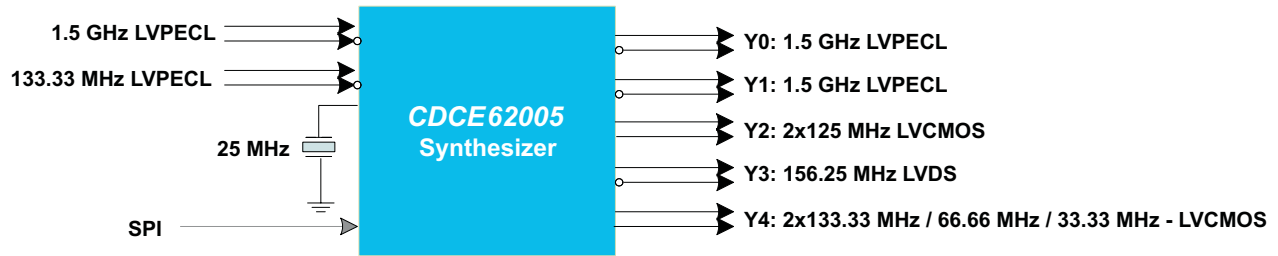


Figure 13. Setup Configuration # 4

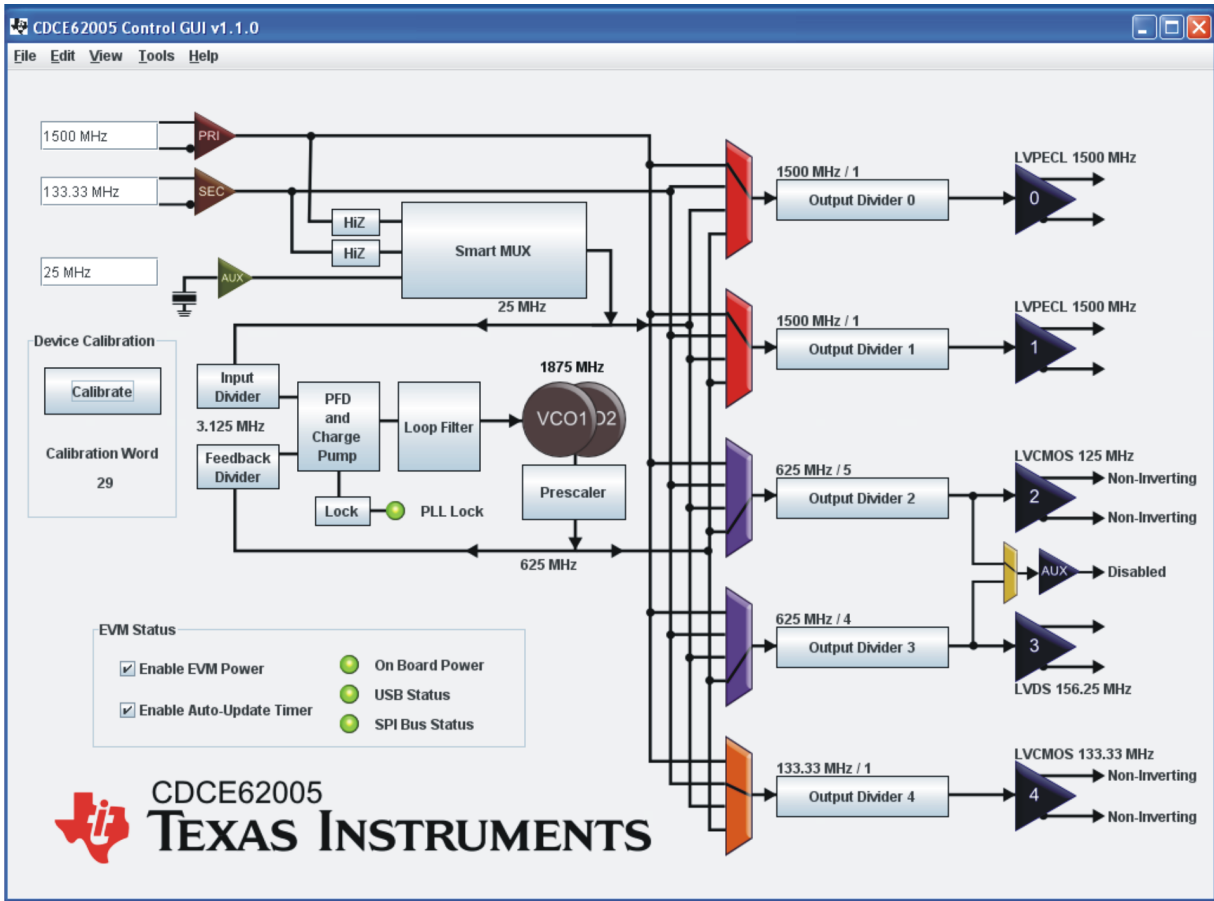
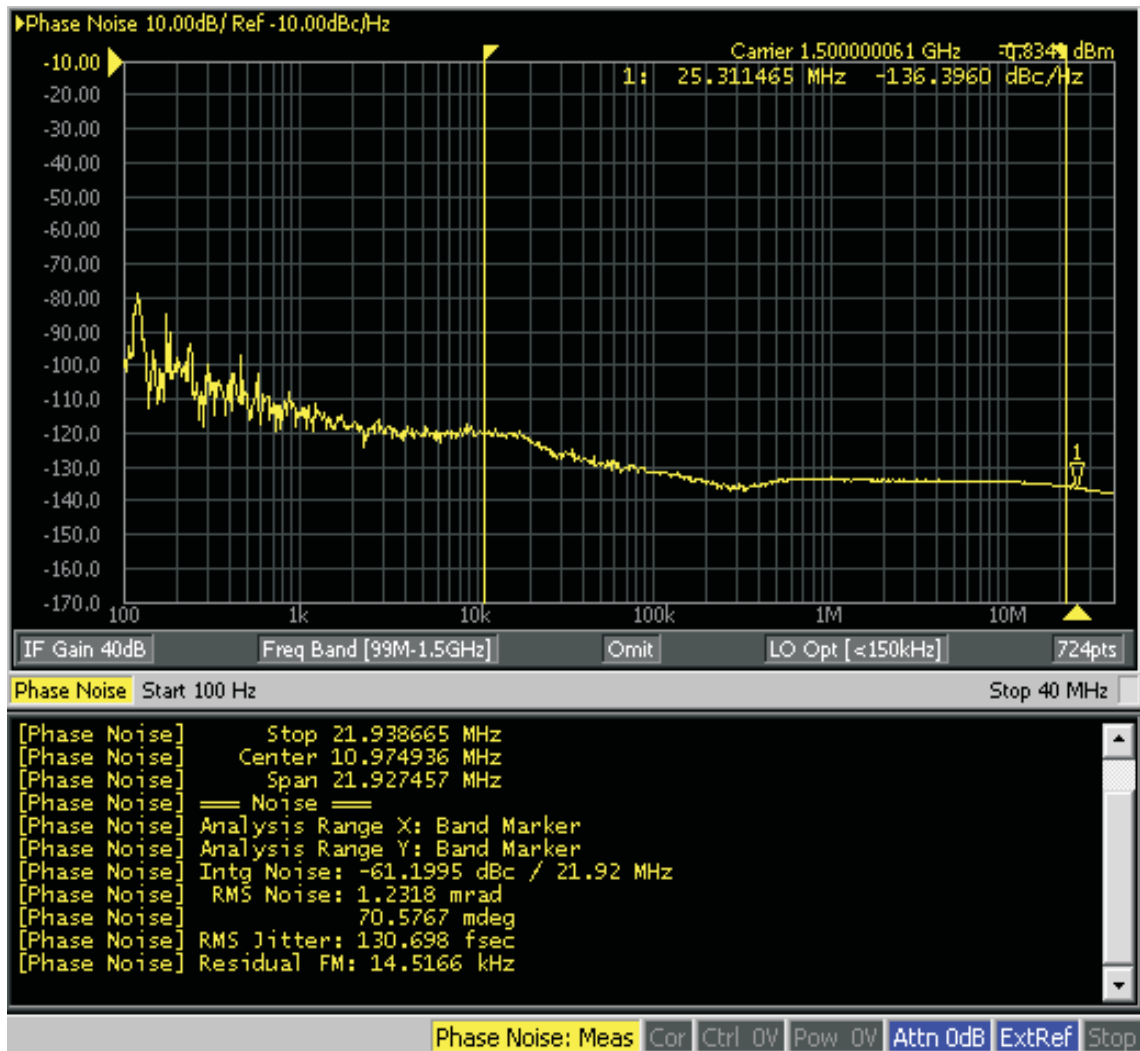


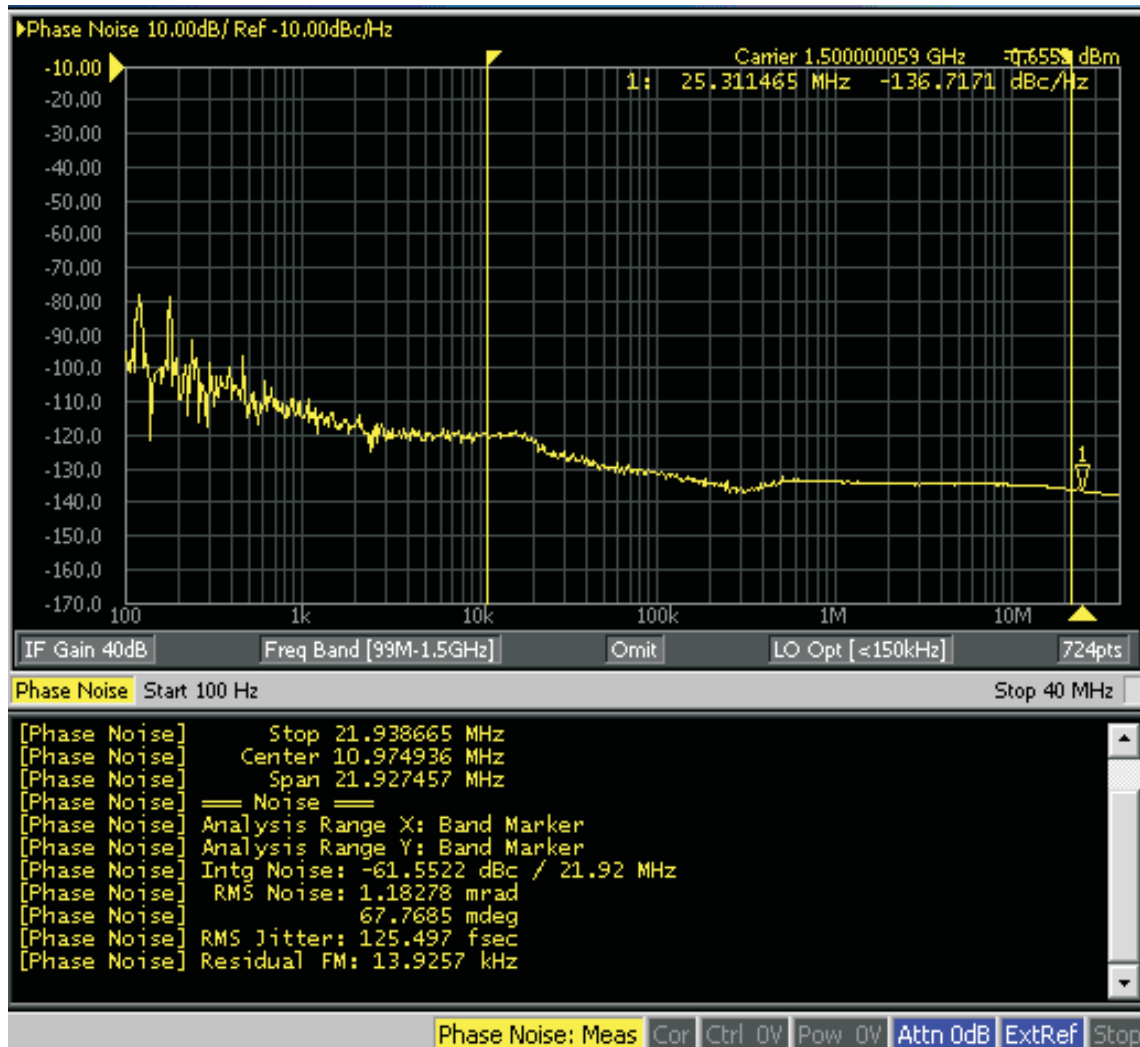
Figure 14. TI GUI Setup Configuration # 4

5.4 Configuration #4 Phase Noise Plot Results

5.4.1 Y0 = 1500 MHz LVPECL – RMS Jitter is 131 fsec (10 kHz – 20 MHz)



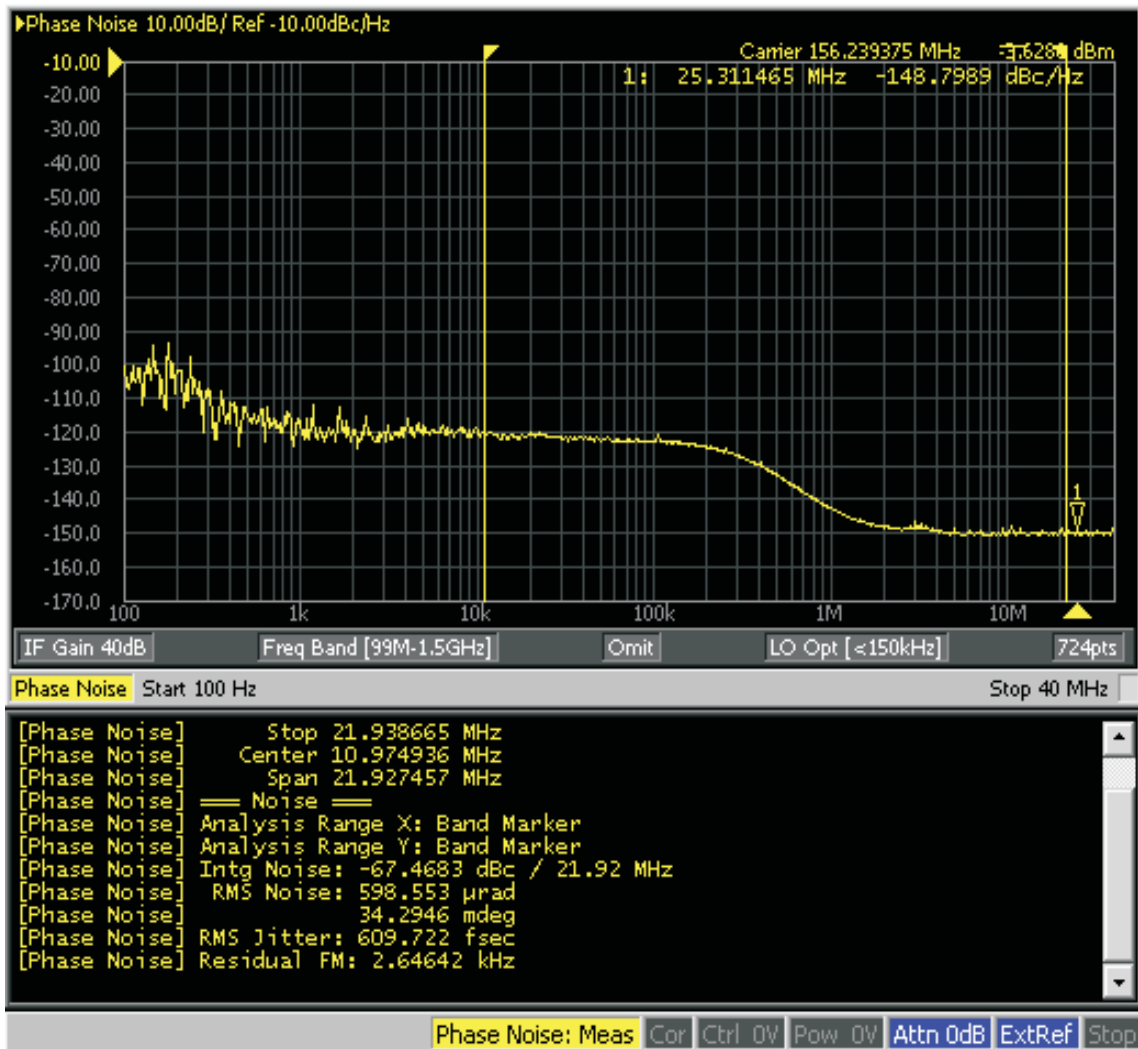
5.4.2 Y1 = 1500 MHz LVPECL – RMS Jitter is 126 fsec (10 kHz – 20 MHz)



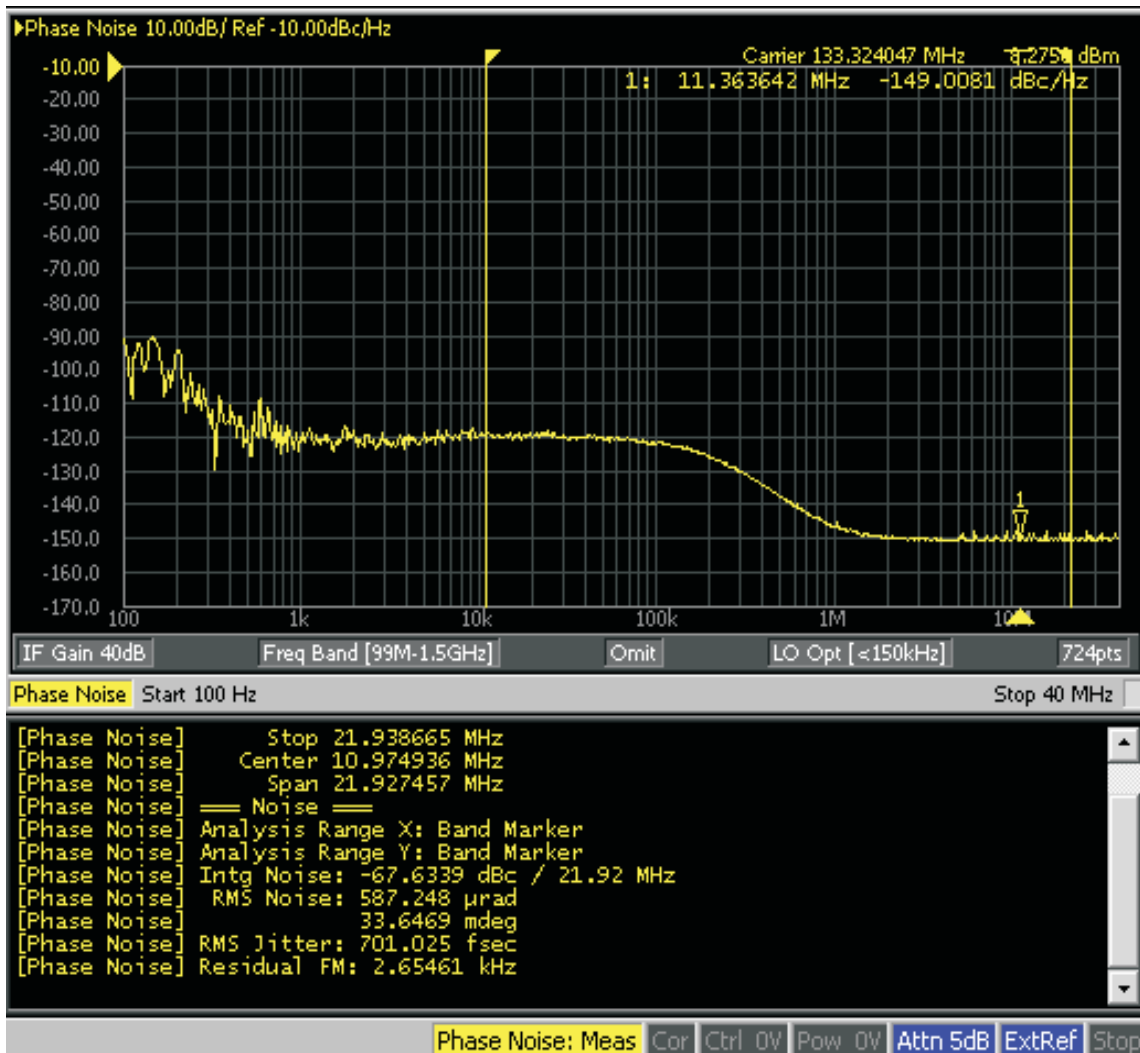
5.4.3 Y2 = 125 MHz LVC MOS – RMS Jitter is 598 fsec (10 kHz – 20 MHz)



5.4.4 Y3 = 156.25 MHz LVDS – RMS Jitter is 610 fsec (10 kHz – 20 MHz)



5.4.5 Y4 = 133.33 MHz LVCMOS – RMS Jitter is 701 fsec (10 kHz – 20 MHz)



6 Performance Summary

6.1 Configuration #1

Performance results of this LAN configuration are:

- Y0 = 125 MHz LVDS – RMS Jitter is 540.65 fsec (10 kHz–20 MHz)
- Y1 = 312.5 MHz LVPECL – RMS Jitter is 544.445 fsec (10 kHz–20 MHz)
- Y2 = 156.25 MHz LVPECL – RMS Jitter is 520.358 fsec (10 kHz–20 MHz)
- Y3 = 625 MHz LVPECL – RMS Jitter is 447.949 fsec (10 kHz–20 MHz)
- Y4 = 25 MHz LVCMOS – RMS Jitter is 260.716 fsec (10 kHz–5 MHz)

All the above frequencies are generated by a standard 25MHz input crystal. Y4 is a bypass of the input crystal and is not generated from the internal VCO core.

6.2 Configuration #2

Performance results of this WAN configuration are:

- Y0 = 77.76 MHz LVDS – RMS Jitter is 631.58 fsec (10 kHz–20 MHz)
- Y1 = 311.04 MHz LVPECL – RMS Jitter is 566.235 fsec (10 kHz–20 MHz)
- Y2 = 155.52 MHz LVPECL – RMS Jitter is 529.116 fsec (10 kHz–20 MHz)
- Y3 = 19.44 MHz LVCMOS – RMS Jitter is 668.012 fsec (10 kHz–5 MHz)
- Y4 = 622.08 MHz LVPECL – RMS Jitter is 550.111 fsec (10 kHz–20 MHz)

6.3 Configuration #3

Performance results of this LAN/WAN configuration are:

- Device #1 : Y0 = 155.52 MHz LVPECL – RMS Jitter is 603.264 fsec (10 kHz–20 MHz)
- Device #1 : Y0 = 156.25 MHz LVPECL – RMS Jitter is 522.996 fsec (10 kHz–20 MHz)
- Device #2 : U1 = 156.25 MHz LVPECL – RMS Jitter is 556.006 fsec (10 kHz–20 MHz)
- Device #2 : U1 = 155.52 MHz LVPECL – RMS Jitter is 576.166 fsec (10 kHz –20 MHz)

In this example, only the measurement data is shown for device #1 output Y0 and device #2 output U1 at 155.52 MHz and then switched to 156.25MHz. All other outputs (Y1-Y4; U0,U2-U4) will show approximately the same jitter as they are just copies of the same frequency. Remember that device #1 bypasses the 155.52MHz from the output of device #2 output U0, so the additive jitter of the CDCE62005 device # 1 output Y0 can be calculated as follows:

$$\begin{aligned}
 \text{Additive jitter at device \#1 output Y0} &= \sqrt{(Y0^2 - U0^2)} \\
 &= \sqrt{(603.264^2 - 576.166^2)} \\
 &= 178.7741 \text{ fsec RMS}
 \end{aligned}$$

Assume that $U0 = \approx U1$.

The same applies for calculating the additive jitter of device # 2 when the 156.25MHz is bypassed from device #1 Y4

$$\begin{aligned}
 \text{Additive jitter at device \#2 output U1} &= \sqrt{(U1^2 - Y4^2)} \\
 &= \sqrt{(556.006^2 - 522.996^2)} \\
 &= 188.7269 \text{ fsec RMS}
 \end{aligned}$$

Assume that $Y4 = \approx Y0$.

6.4 Configuration #4

Performance results of this general purpose configuration are:

- Y0 = 1500 MHz LVPECL – RMS Jitter is 130.698 fsec (10 kHz–20 MHz)
- Y1 = 1500 MHz LVPECL – RMS Jitter is 125.497 fsec (10 kHz–20 MHz)
- Y2 = 125 MHz LVCMOS – RMS Jitter is 597.782 fsec (10 kHz–20 MHz)
- Y3 = 156.25 MHz LVDS – RMS Jitter is 609.722 fsec (10 kHz–20 MHz)
- Y4 = 133.33 MHz LVCMOS – RMS Jitter is 701.025 fsec (10 kHz – 20 MHz)

In this example there are 3 clocks that are bypassed for the input and 2 clocks that are generated by the internal VCO core.

Input jitter of the 1500 MHz clock at PRI_IN is 120 fsec RMS.

Input jitter of the 133.33 MHz clock at SEC_IN is 512 fsec RMS.

Additive jitter can then be calculated as:

$$\begin{aligned} \text{Y0 additive jitter} &= \sqrt{(\text{Y0 total output jitter}^2 - \text{Input jitter}^2)} \\ &= \sqrt{(130.689^2 - 120^2)} \\ &= 51.765 \text{ fsec RMS} \end{aligned}$$

$$\begin{aligned} \text{Y1 additive jitter} &= \sqrt{(\text{Y1 total output jitter}^2 - \text{Input jitter}^2)} \\ &= \sqrt{(125.497^2 - 120^2)} \\ &= 36.7355 \text{ fsec RMS} \end{aligned}$$

$$\begin{aligned} \text{Y4 additive jitter} &= \sqrt{(\text{Y4 total output jitter}^2 - \text{Input jitter}^2)} \\ &= \sqrt{(701.025^2 - 512^2)} \\ &= 478.8445 \text{ fsec RMS} \end{aligned}$$

7 Conclusion

The CDCE62005 performance meets networking frequencies and low jitter requirements <1ps RMS. It is a flexible device that can be configured in a number of ways to meet specific system needs.

The CDCE62005 is offered in a 48-pin 6mm × 6mm QFN package. This single, 3.3 V device can replace the functionality of multiple expensive oscillators, clock muxes, and buffers. In addition to lowering cost, the CDCE62005 offers additional advances features like output phase adjust and mixed output signal levels. Either through the SPI bus or EEPROM, the required frequencies can be generated.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
RF/IF and ZigBee® Solutions	www.ti.com/lprf

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Medical	www.ti.com/medical
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2008, Texas Instruments Incorporated