Application Note

LVxT Family of Single Supply Translating Logic Gates

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ABSTRACT

Compared to other logic families, the LVxT family is the most well-rounded and universal in terms of specifications. The LVxT family of devices combines a reduced input threshold voltage with a wide supply range, allowing for up or down voltage translation with only one power rail. The family has overvoltage-tolerant inputs that allow down translation from up to 5.5 V down to the supply voltage, which can be as low as 1.6 V. The reduced input thresholds allow for up-translation from inputs as low as 2.03 V up to 5-V outputs. See the list below for a summary of common voltage nodes and translation combinations supported.

1.8-V Supply	2.5-V Supply	3.3-V Supply	5.0-V Supply
1.2 V → 1.8 V			
1.8 V → 1.8 V	1.8 V → 2.5 V	1.8 V → 3.3 V	
2.5 V → 1.8 V	2.5 V → 2.5 V	2.5 V → 3.3 V	2.5 V → 5.0 V
3.3 V → 1.8 V	3.3 V → 2.5 V	3.3 V → 3.3 V	3.3 V → 5.0 V
5.0 V → 1.8 V	5.0 V → 2.5 V	5.0 V → 3.3 V	5.0 V → 5.0 V

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1 Advantages of Using the LVxT Gates and Buffers to Translate

Many Common Functions Supported

The LVxT family includes many common logic gates such as AND, NAND, OR, NOR, XOR, and XNOR functions. We also offer configurable gates that provide the greatest flexibility. See our full portfolio of translating gates here.

Simplified System Design

Because only one supply is required for operation, the LVxT family of logic can be used to reduce the number of supply rails required in some systems.

Reduced Design Size

The LVxT family are available in the surface mount DBV (SOT-23) and DCK (SC70) packages and replace both a logic function and voltage translator reducing BOM count and overall solution size.

No Pull-ups or Pull-downs Required

Unlike open-drain translators, no external resistors are required for voltage translation.

Over-voltage Tolerant Inputs

All LVxT devices support up to 5.5-V input signals independent of supply voltage allowing for simple down-translation.

Mixed Mode Operation

Inputs can be at different voltages, allowing for logic using signals from different voltage domains.

2 Translating Down

Using these parts to translate down is very simple because the inputs are tolerant to 5.5 V, completely independent of supply voltage (V_{CC}). The input high-state voltage can be any value from the defined minimum input high-state voltage (V_{IH}) in the datasheet to 5.5 V, **including above V_{CC}**.

The output high-level voltage (V_{OH}) always equals the supply (V_{CC}) level, which can be as low as 1.6 V. One advantage to down translating using this part is that the I_{CC} current remains less than or equal to the maximum specified value in the datasheet as long as the input voltage is equal to or larger than the supply voltage. The typical switching thresholds for 3.3-V operation can be seen in Figure 2-1.

Common down translation possibilities with the LVxT family:

- 1.8-V V_{CC}: from 2.5 V, 3.3 V, or 5 V down to 1.8 V
- 2.5-V V_{CC}: from 3.3 V, to 5 V down to 2.5 V
- 3.3-V V_{CC}: from 5 V down to 3.3 V

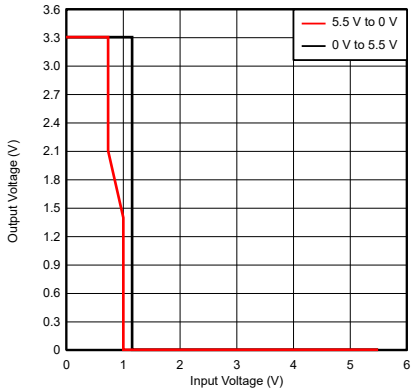

Figure 2-1. Switching Threshold with 3.3-V Supply (V_{CC})

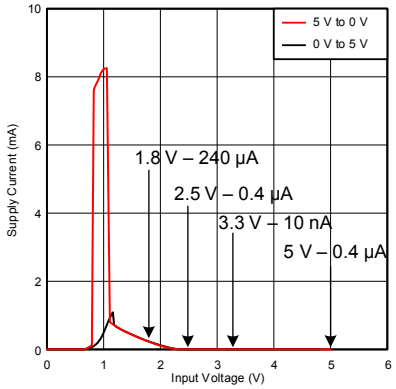

Figure 2-2. Power Consumption when Translating

3 Translating Up

Using the LVxT family to translate up is very simple. The input switching threshold is lowered, thus the high state voltage level (V_{IH}) of the input can be much lower than that used for a typical CMOS device. For example, if the V_{CC} is 3.3 V, the typical CMOS switching threshold would be $V_{CC}/2$, or 1.65 V. Thus the input high voltage level (V_{IH}) must be at least V_{CC} × 0.7, or 2.31 V. However, for LVxT devices the input threshold for 3.3-V V_{CC} is approximately 1 V. This allows a signal with a 1.8-V V_{IH} to be translated up to the V_{CC} level of 3.3 V. See an example of this in the voltage characteristic plot, Figure 1.

Common up translation possibilities with LVxT family:

- 2.5-V V_{CC}: from 1.8 V to 2.5 V
- 3.3-V V_{CC}: from 1.8 V or 2.5 V to 3.3 V
- 5-V V_{CC}: from 2.5 V or 3.3 V to 5 V

Because these parts are CMOS, there is additional supply current (I_{CC}) consumption only when the input is much less than V_{CC}, which is common when up-translating. The current draw for up-translation at different input values is shown in Figure 2-2.

4 Example Application 1: PWM with Filter

One application where the LVxT family can be useful is in PWM translation. In this example, the amplifier accepts a 3.3-V PWM into its input filter, but the MCU can only supply 1.8 V from its GPIOs. The SN74LV1T34 is used in this example to translate the PWM signal to a 3.3-V level. It also serves to isolate the MCU from excess line capacitance, making the signal cleaner at higher speeds.

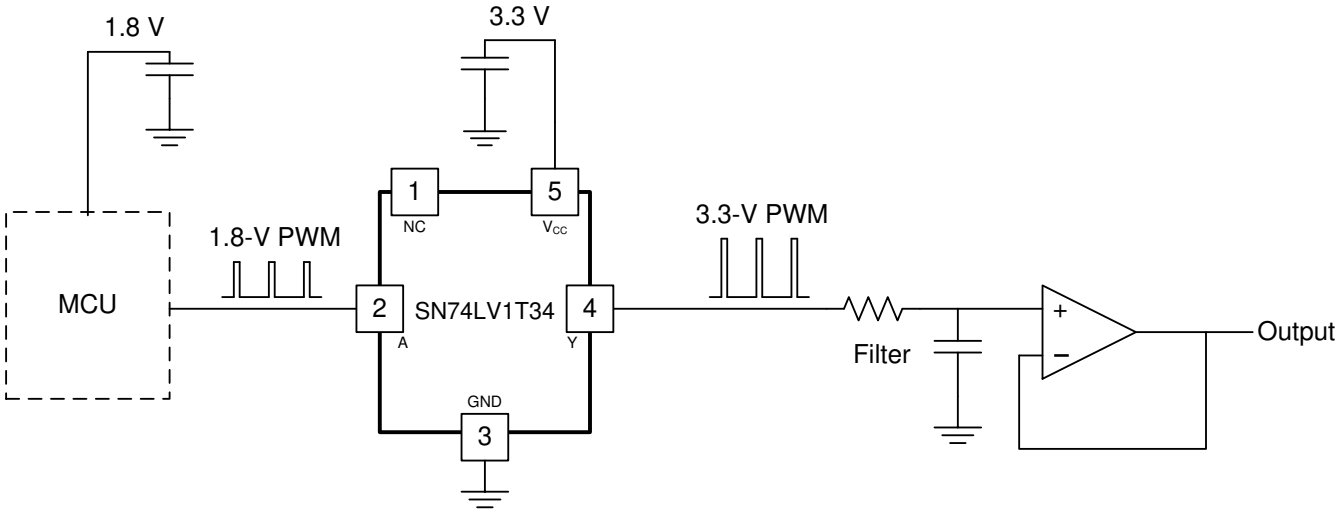

Figure 4-1. Example schematic for SN74LV1T34 PWM buffer circuit

5 Example Application 2: PGOOD Circuit

In this example, the engineer wants to send a signal to the MCU when both power ICs have been ramped to their appropriate output levels. Normally, this application would require an AND gate, combined with appropriate translators for each level. The SN74LV1T08 2-input AND gate can accept input voltages different than its supply (V_{CC}), even when the A and B inputs are at different voltage levels. The LVxT device allows the engineer to use a single device in the place of the AND gate and translators, which could have previously required up to three separate devices.

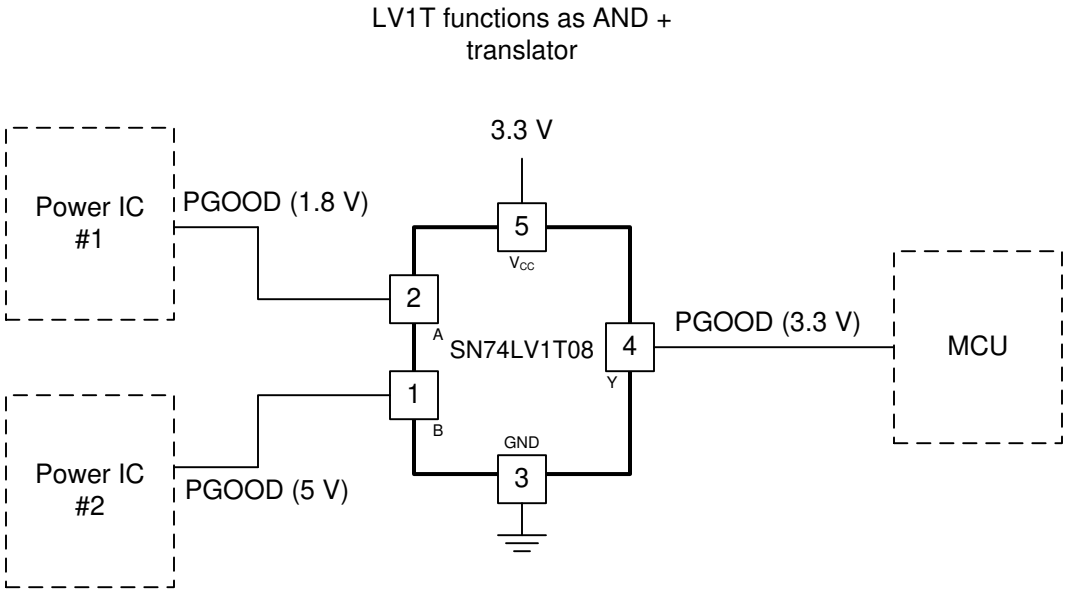

Figure 5-1. Power good schematic with SN74LV1T08 operating with mixed input voltages

6 Conclusion

When a logic function and voltage translation are required together, the LVxT family of devices provides a simple and small solution, whether translating up, down, or even both in some cases.

There will be a small amount of extra power consumption when translating up: consult the datasheet specs if the power consumption is critical, as in a battery-powered device. For the most power efficient solution, see our line of active dual supply translators here.

7 Revision History

Changes from Revision * (November 2013) to Revision A (December 2014)	Page
• Modified Abstract	1
• Added Family Comparison graph	1
• Updated Advantages section	2

Changes from Revision A (December 2014) to Revision B (November 2022)	Page
• Updated formatting, improved verbiage, and removed Family Comparison graph	1

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