Functional Safety Information

LM74703-Q1 and LM74704-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for LM74703-Q1 and LM74704-Q1 to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device

Figure 1-1 shows the device functional block diagram for reference.

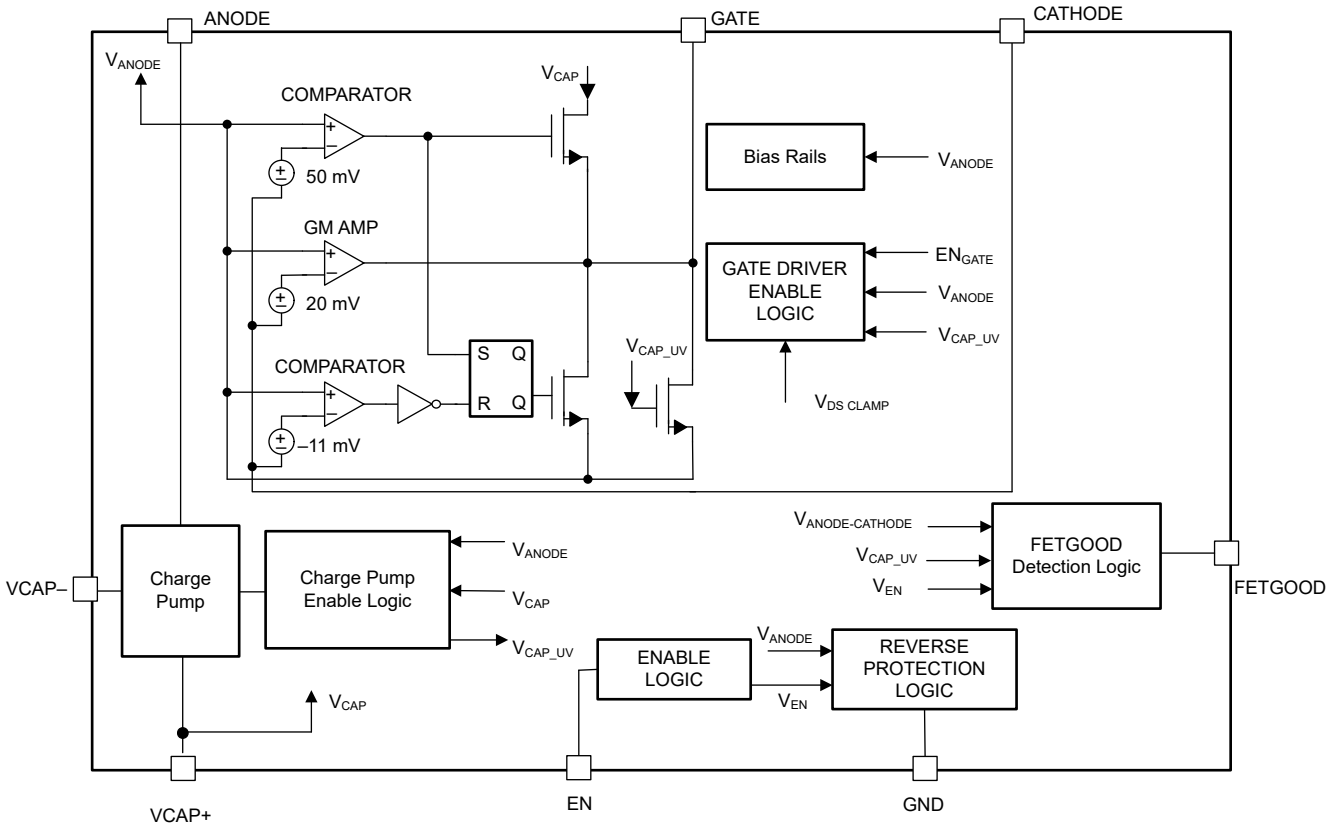

Figure 1-1. Functional Block Diagram

LM74703-Q1 and LM74704-Q1 are developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for LM74703-Q1 and LM74704-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	5
Die FIT Rate	3
Package FIT Rate	2

The failure rate and mission profile information in Table 2-2 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 2mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS logic	12	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for LM74703-Q1 and LM74704-Q1 in Table 3-1comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
GATE output voltage or timing not in specification	25%
GATE Stuck at High	20%
GATE stuck at Low	30%
FETGOOD fails to trip or false trip	20%
Pin to Pin short	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the LM74703-Q1 and LM74704-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the LM74703-Q1 and LM74704-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration* and *Functions* section in the LM74703-Q1 and LM74704-Q1 data sheet.

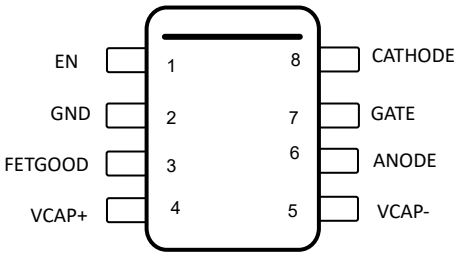

Figure 4-1. Pin Diagram

The pin FMA is provided under the assumption that the device is operating under the specified ranges within the Recommended Operating Conditions section of the data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	Device does not power up External FET can get hot due to Body Diode conduction and be damaged	B
FETGOOD	3	1. PGOOD cannot assert high in open drain variant (LM74704-Q1) 2. PGOOD cannot assert high in push-pull variant (LM74703-Q1) and device Iq increases	B
VCAP+	4	Device can be damaged due to internal paths from ANODE to VCAP External FET can get hot due to Body Diode conduction and be damaged	A
VCAP-	5	Device can be damaged. External FET can get hot due to Body Diode conduction and be damaged	A
ANODE	6	Equivalent to supply short to GND. Device does not power up	B
GATE	7	External FET does not turn ON External FET can get hot due to Body Diode conduction and be damaged Device can be damaged due to diode path between Anode and GATE	A
CATHODE	8	Equivalent to output short to GND Linear regulation and reverse current blocking functionality is lost	B

Table 4-3. Pin FMA for Device Pins Open Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	Device is in OFF state due to internal pull down External FET can get hot due to Body Diode conduction and be damaged	B
GND	2	Device does not power up External FET can get hot due to Body Diode conduction and be damaged	B
FETGOOD	3	FETGOOD information is not provided to monitoring system	B
VCAP+	4	External FET does not turn ON External FET can get hot due to Body Diode conduction and be damaged	B
VCAP-	5	External FET does not turn ON External FET can get hot due to Body Diode conduction and be damaged	B
ANODE	6	Device does not power up External FET can get hot due to Body Diode conduction and be damaged	B
GATE	7	External FET does not turn ON External FET can get hot due to Body Diode conduction and be damaged	B
CATHODE	8	The external FET is fully ON, functions as an ON/OFF switch Reverse Current Blocking feature is lost	B

Table 4-4. Pin FMA for Device Pins Short Circuited to Adjacent Pin

Pin Name	Shorted to	Description of Potential Failure Effects	Failure Effect Class
EN	GND	Device does not power up External FET can get hot due to Body Diode conduction and get damaged	B
GND	FETGOOD	1. PGOOD cannot assert high in open drain variant (LM74704-Q1) 2. PGOOD cannot assert high in push-pull variant (LM74703-Q1) and device Iq increases	B
FETGOOD	VCAP+	1. High current flows in the push-pull variant (LM74703-Q1) and device can heat up 2. High current flows when FETGOOD pin tries to go low, device can heat up in open drain variant (LM74704-Q1) 3. In both the variants, VCAP+ collapses when high current flows into PGOOD pin hence GATE can be turned OFF	A
VCAP-	ANODE	No impact	C
ANODE	GATE	External FET does not turn ON External FET can get hot due to Body Diode conduction and be damaged	B
GATE	CATHODE	External FET does not turn ON External FET can get hot due to Body Diode conduction and be damaged	B

Table 4-5. Pin FMA for Device Pins Short Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
EN	1	Device is always on as EN is pulled to supply	B
GND	2	Equivalent to supply short to GND. Device does not power up	B
FETGOOD	3	1. High current flows in the push-pull variant (LM74703-Q1) and device can heat up 2. High current flows when PGOOD pin tries to go low, device can heat up in open drain variant (LM74704-Q1)	A
VCAP+	4	Device cannot turn ON external FET Gate External FET can get hot due to body diode conduction and be damaged	B
VCAP-	5	No impact	C
ANODE	6	No impact	D
GATE	7	External FET does not turn ON External FET can get hot due to body diode conduction and be damaged	B
CATHODE	8	Ideal diode functionality is not available	B

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