TLC6C5816-Q1 Power Logic 16-Bit Shift Register LED Driver With Diagnostics

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125ºC Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H3A
  - Device CDM ESD Classification Level C6
  - Functional safety capable
    - Documentation available to aid functional safety system design
- 16 Channels With Power DMOS Transistor Outputs
  - Open-Drain Outputs up to 50 mA per Channel
  - Output Voltage Maximum Rating: 45 V
  - Optimized Slew Rate for Reducing EMI
- Serial Interface and PWM Inputs
  - Shift Register Compatible With TPIC6C596, TLC6C598-Q1, TLC6C5912-Q1
  - LED Status Read-back
  - 2 PWM Inputs for Group Dimming
- Diagnostics and Protection
  - Configurable LED Open and Short Diagnostics
  - Overtemperature Protection
  - Serial-Interface Communication-Error Detection
  - Open-Drain Error Feedback

2 Applications

- Automotive Instrument Clusters
- Automotive HVAC Control Panels
- Automotive Interior Faceplate
- Automotive E-Shifter Indicators
- Automotive Center Stacks

3 Description

There are various LED indicators in automotive applications. Some applications such as hybrid instrument clusters and E-shifters have safety requirements which must have LED fault diagnostics; other applications such as HVAC panels only have an LED on-off control, which does not require LED diagnostics. To cover both applications, the TLC6C5816-Q1 device implements a flexible LED diagnostics function. By writing to the registers, the output channels can be configured with LED diagnostics features or without LED diagnostics features.

The TLC6C5816-Q1 device is a 16-bit shift register LED driver designed to support automotive LED applications. A built-in LED open and LED short diagnostic mechanism provides enhanced safety protection. The device contains 16 channels with power DMOS transistor outputs. Eight of the channels support LED fault diagnostics by configuring corresponding registers, the device can drive 16 channels without diagnostics or 8 channels with diagnostics. The diagnostics channels DIAGn must connect to DRAINn to realize LED diagnostics. A command error fault implies that a channel is configured for LED diagnostics but a register write command has turned on the channel at the same time. The device provides a cyclic redundancy check to verify register values in the shift registers. In read-back mode, the device provides 6 bits of the CRC remainder. The MCU can read back the CRC remainder and check if the remainder is correct to determine whether the communication loop between MCU and device is good.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLC6C5816-Q1	HTSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic

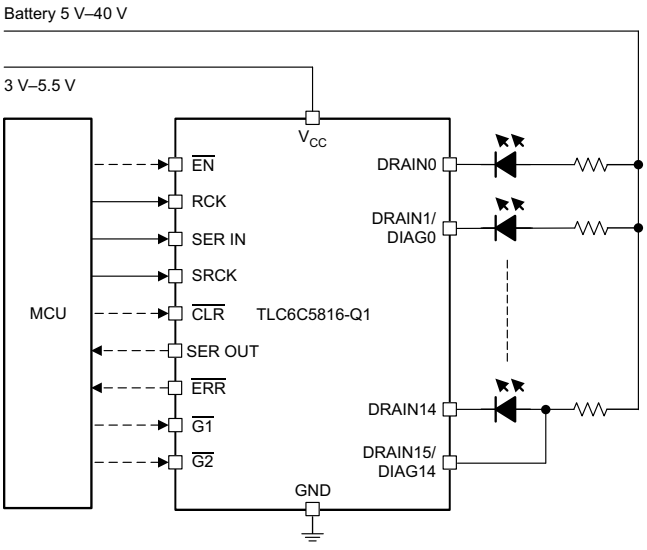


Table of Contents

4 Revision History

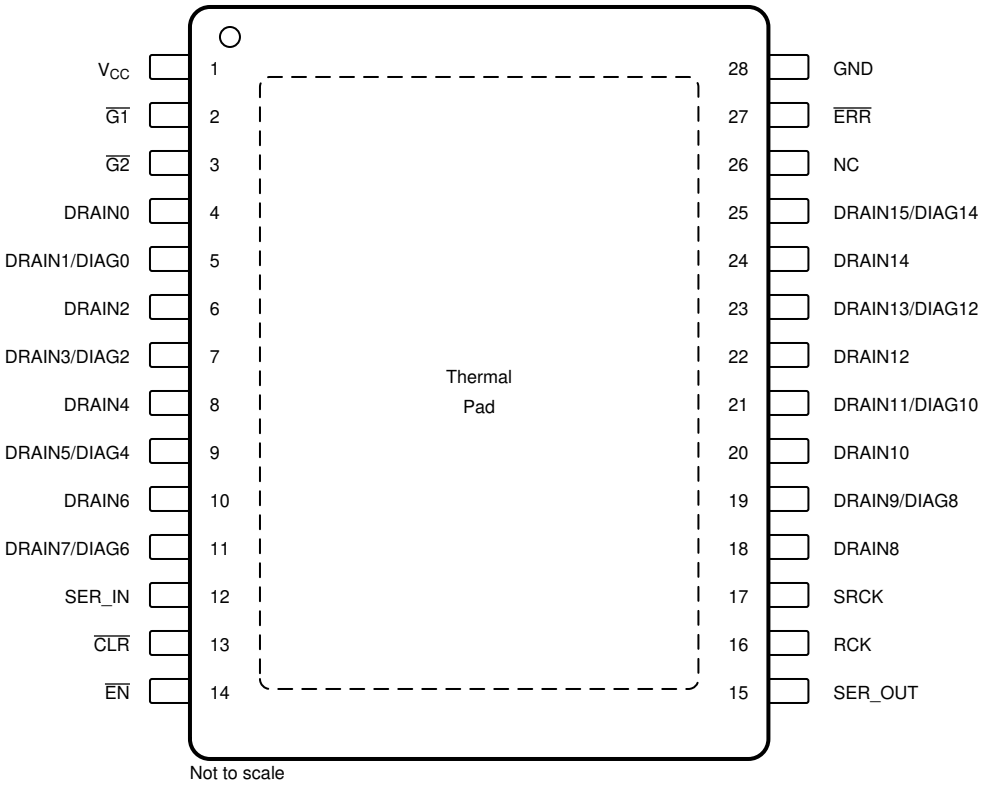
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2017) to Revision B	Page
• Added the functional safety link to the *Features* section	1

Changes from Original (October 2017) to Revision A	Page
• Changed data sheet from Advance Information to Production Data	1

5 Pin Configuration and Functions

PWP PowerPAD™ Package
28-Pin HTSSOP With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{CLR}$	13	I	Shift register clear, active-low. $\overline{CLR}$ low level clears all the storage registers in the device, shift registers work normally. $\overline{CLR}$ high level makes both storage registers and shift registers work normally.
DRAIN0	4	O	Channel 0 open drain-output
DRAIN1/DIAG0	5	I/O	Channel 1 open-drain output or diagnostics input 0
DRAIN2	6	O	Channel 2 open drain output
DRAIN3/DIAG2	7	I/O	Channel 3 open-drain output or diagnostics input 2
DRAIN4	8	O	Channel 4 open drain output
DRAIN5/DIAG4	9	I/O	Channel 5 open-drain output or diagnostics input 4
DRAIN6	10	O	Channel 6 open-drain output
DRAIN7/DIAG6	11	I/O	Channel 7 open-drain output or diagnostics input 6
DRAIN8	18	O	Channel 8 open-drain output
DRAIN9/DIAG8	19	I/O	Channel 9 open-drain output or diagnostics input 8
DRAIN10	20	O	Channel 10 open-drain output
DRAIN11/DIAG10	21	I/O	Channel 11 open-drain output or diagnostics input 10
DRAIN12	22	O	Channel 12 open-drain output
DRAIN13/DIAG12	23	I/O	Channel 13 open-drain output or diagnostics input 12
DRAIN14	24	O	Channel 14 open-drain output
DRAIN15/DIAG14	25	I/O	Channel 15 open-drain output or diagnostics input 14

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{EN}$	14	I	Device enable, active-low. $\overline{EN}$ high level shuts down the device, all the registers reset, and the device enters standby mode. $\overline{EN}$ low level enables the device, all functions work normally.
$\overline{ERR}$	27	O	Open-drain error feedback
$\overline{G1}$	2	I	Channel enable, controls DRAIN0–DRAIN7 outputs, active-low
$\overline{G2}$	3	I	Channel enable, controls DRAIN8–DRAIN15 outputs, active-low
NC	26	NC	No intenal connection
RCK	16	I	Serial data latch. The data in each shift register transfers to a storage register at the rising edge of RCK. Meanwhile, the status bit is loaded to the shift register.
SER IN	12	I	Serial data input. Data on SER IN loads into the shift register on each rising edge of SRCK.
SER OUT	15	O	Serial data output. The purpose of this pin is to cascade several devices on the serial bus.
SRCK	17	I	Serial clock input. On each rising SRCK edge, data transfers from SER IN to the internal serial shift registers.
V_{CC}	1	P	Power supply pin for the device. Add a 0.1-μF ceramic capacitor near the pin.
GND	28	G	Power ground, the ground reference pin for the device. This pin must connect to the ground plane on the PCB.
Thermal pad	—	—	Connect to polygon pour to optimize thermal performance

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
V_I	Logic input voltage, $\overline{CLR}$, $\overline{EN}$, $\overline{G1}$, $\overline{G2}$, RCK, SER IN, SRCK	–0.3	6	V
V_O	Logic output voltage, SER OUT	–0.3	V_{CC} + 0.3	V
V_{DS}	Power DMOS drain-source voltage, DRAIN0–DRAIN15	–0.3	45	V
V_{ERR}	Error output voltage, $\overline{ERR}$	–0.3	6	V
I_O	Channel output current		50	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±4000	V
	Charged-device model (CDM), per AEC Q100-011	All pins	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	5.5	V
V_{IH}	High-level input voltage, $\overline{CLR}$, $\overline{EN}$, $\overline{G1}$, $\overline{G2}$, RCK, SER IN, SRCK	2.4		V
V_{IL}	Low-level input voltage, $\overline{CLR}$, $\overline{EN}$, $\overline{G1}$, $\overline{G2}$, RCK, SER IN, SRCK		0.7	V
T_A	Operating ambient temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TLC6C5816-Q1 PWP (HTSSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	44.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

V_{CC} = 5 V, T_J = –40°C to 150°C unless otherwise specified

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{(POR\text{-}rising)}$	Power-on-reset rising threshold			1.5		2.5	V
$V_{(POR\text{-}falling)}$	Power-on-reset falling threshold			1			V
$t_{(device\text{-}ready)}$	Device ready time	V_{CC} > 0.5 V, $\overline{EN}$ = 0			50		µs
I_{CC}	Logic supply current	All outputs off, no clock signal , $\overline{EN}$ = 0			60	120	µA
		All outputs on, no clock signal, $\overline{EN}$ = 0			210	300	
$I_{CC(FRQ)}$	Logic supply current at frequency	f_{SRCK} = 5 MHz, C_L = 30 pF, all outputs on			320	600	µA
$I_{(Q)}$	Quiescent current	$\overline{EN}$ = 1				1	µA
V_{OH}	High-level output voltage SER OUT	I_{OH} = –20 µA		4.9	4.99		V
		I_{OH} = –4 mA		4.5	4.69		
V_{OL}	Low-level output voltage SER OUT	I_{OH} = –20 µA			0.001	0.01	V
		I_{OH} = –4 mA			0.25	0.4	
I_{IH}	High-level input current	V_I = 5 V			0.2		µA
I_{IL}	Low-level input current	V_I = 0 V			–0.2		µA
$I_{D(SX)}$	Off-state drain current	V_{DS} = 30 V			0.01	0.1	µA
		V_{DS} = 30 V, T_A = 125°C			0.1	0.3	
$r_{DS(on)}$	Static drain-source on-state resistance	V_{CC} = 5 V, I_D = 20 mA	T_A = 25°C, single channel ON	5	6.2	8	Ω
		V_{CC} = 3.3 V, I_D = 20 mA	T_A = 25°C, all channels ON	6	7.3	9	
			T_A = 125°C, all channels ON	9	11.6	13.5	
$T_{(SHUTDOWN)}$	Thermal shutdown threshold				175		°C
$T_{(HYS)}$	Thermal shutdown hysteresis				15		°C
$V_{(OC\_th)}$	LED-open detection threshold			4	4.3	4.5	V
$V_{hys(OC)}$	LED-open detection-threshold hysteresis				60		mV
$V_{(SC\_th)}$	LED-short detection threshold			1	1.22	1.5	V
$V_{hys(SC)}$	LED-short detection-threshold hysteresis				60		mV
$V_{(ERR\_PD)}$	ERR pin open-drain voltage drop	I_{ERR} = 4 mA				0.3	V
$I_{lkg(ERR)}$	ERR pin leakage current	V_{ERR} = 5 V		–1		1	µA

6.6 Timing Requirements

V_{cc} = 5 V, T_J = 25°C, C_L = 30 pF, I_D = 20 mA unless otherwise specified

		MIN	NOM	MAX	UNIT
f_{SRCK}	Serial clock frequency			10	MHz
t_{SRCK}	Serial clock duration	100			ns
t_{SRCKH}	SRCK pulse duration, high	30			ns
t_{SRCKL}	SRCK pulse duration, low	30			ns
t_{su}	Setup time, SER IN high before SRCK rise	15			ns
t_h	Hold time, SER IN high after SRCK rise	15			ns
$t_{SER\ IN}$	SER IN pulse duration	40			ns
t_d	Last SRCK rise to RCK rise	200			ns

6.7 Switching Characteristics

V_{cc} = 5 V, T_J = 25ºC, C_L = 30 pF, I_D = 20 mA unless otherwise specified

PARAMETER		MIN	TYP	MAX	UNIT
$t_{pd(deg\_open)}$	LED open to $\overline{ERR}$ pin pulled down time		35		µs
$t_{pd(deg\_short)}$	LED short to $\overline{ERR}$ pin pulled down time		35		µs
$t_{pd(GOFF)}$	Propagation delay time, output off (V_{OUT} equals 10% LED supply voltage) from $\overline{Gx}$ rising		250		ns
$t_{pd(GON)}$	Propagation delay time, output on (V_{OUT} equals 90% LED supply voltage) from $\overline{Gx}$ falling		250		ns
$t_{pd(ROFF)}$	Propagation delay time, output off (V_{OUT} equals 10% LED supply voltage) from RCK rising		250		ns
$t_{pd(RON)}$	Propagation delay time, output on (V_{OUT} equals 90% LED supply voltage) from RCK rising		250		ns
t_r	Rise time, drain output		100		ns
t_f	Fall time, drain output		100		ns
$t_{pd(SIO)}$	Propagation delay time, SRCK falling edge to SEROUT change		35		ns
$t_{r(o)}$	SEROUT rise time (10% to 90%)		20		ns
$t_{f(o)}$	SEROUT fall time (90% to 10%)		20		ns

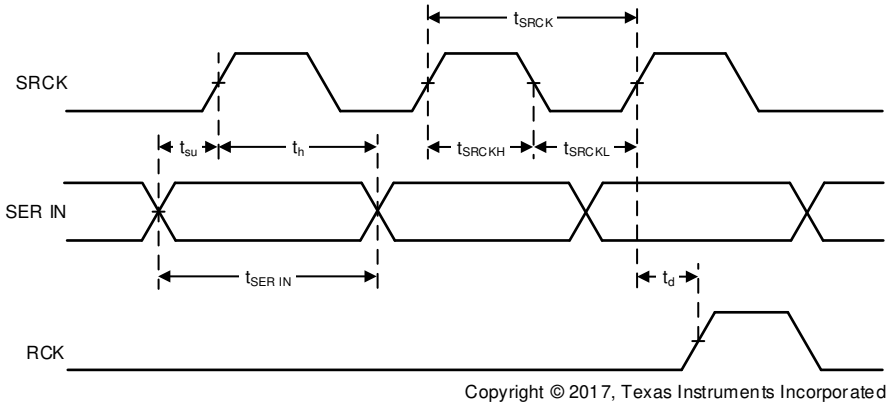


Figure 1. Timing Diagram of Input Signals

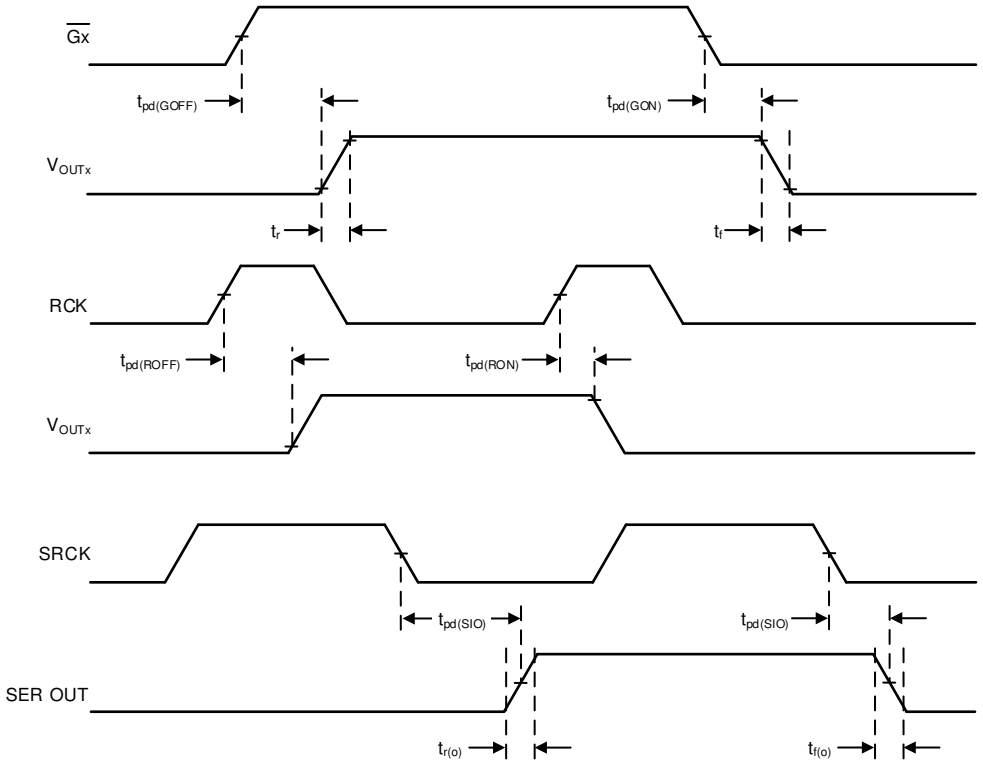


Figure 2. Timing Diagram of Output Signals

6.8 Typical Characteristics

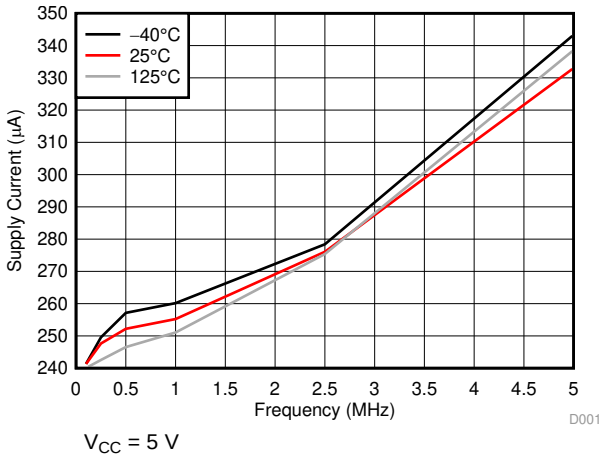


Figure 3. Supply Current vs CLK Frequency

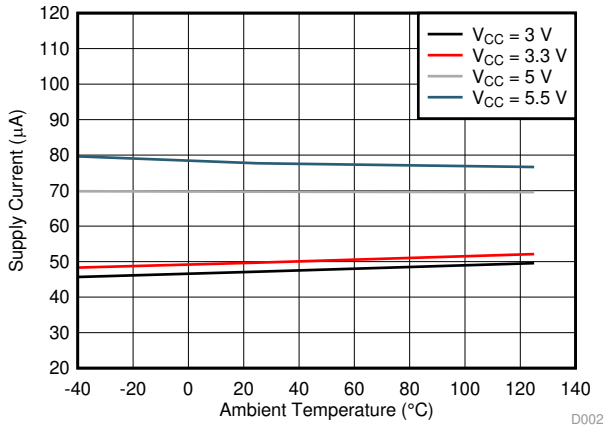


Figure 4. Supply Current vs Ambient Temperature

Typical Characteristics (continued)

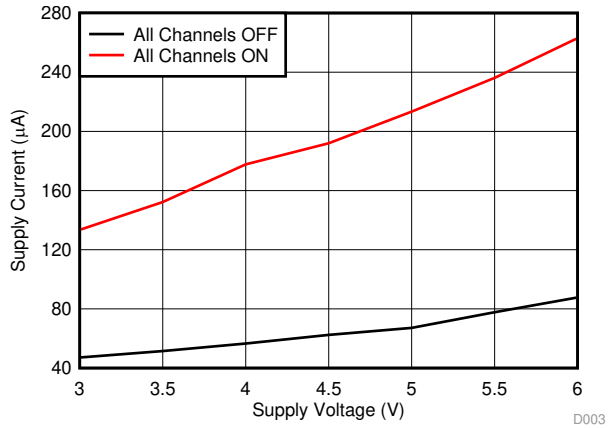


Figure 5. Supply Current vs Supply Voltage

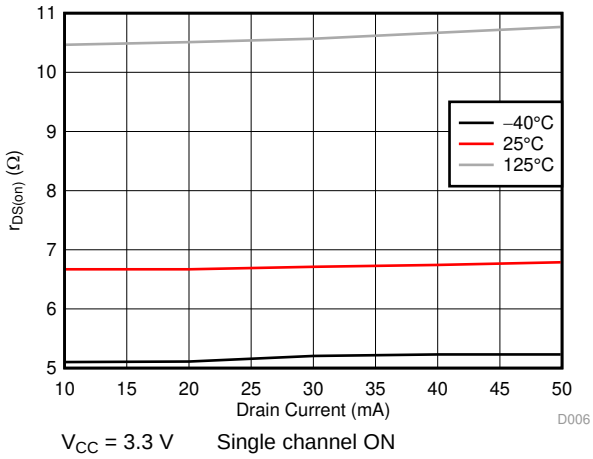


Figure 6. $r_{DS(on)}$ vs Ambient Temperature

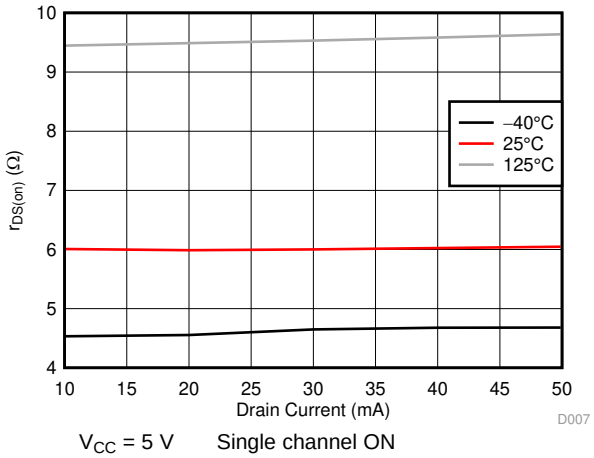


Figure 7. $r_{DS(on)}$vs Ambient Temperature

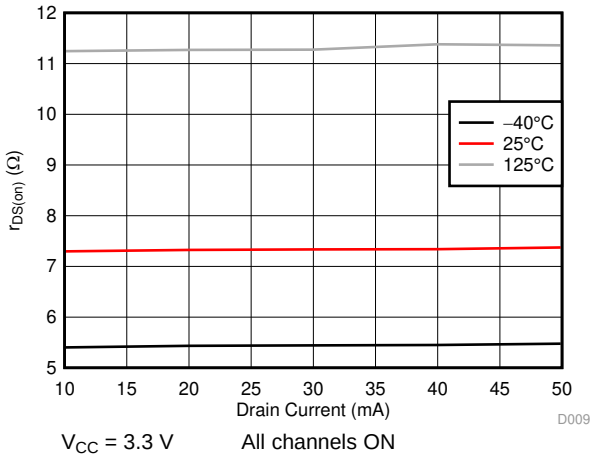


Figure 8. $r_{DS(on)}$vs Drain Current

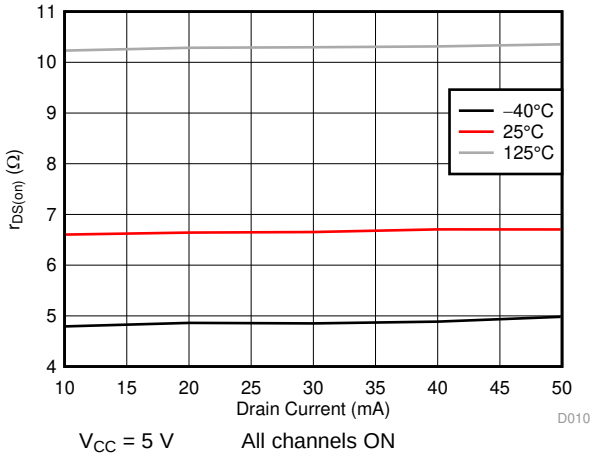


Figure 9. $r_{DS(on)}$ vs Drain Current

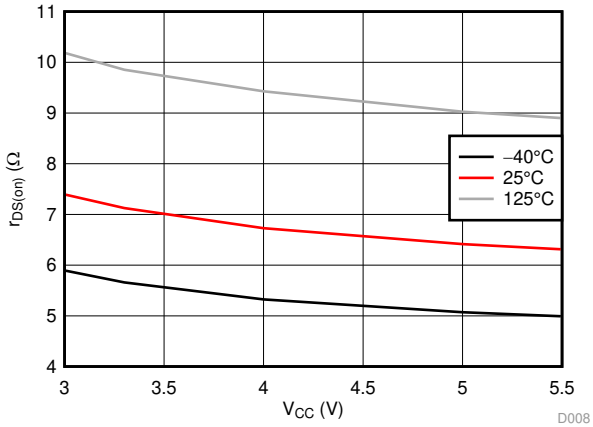


Figure 10. $r_{DS(on)}$ vs Supply Voltage

Typical Characteristics (continued)

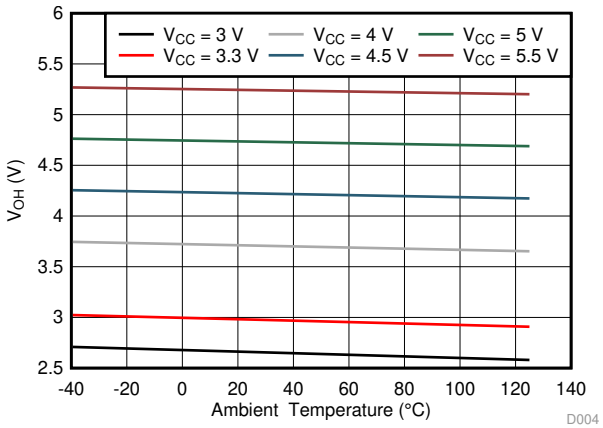


Figure 11. SER OUT High Voltage vs Temperature (°C)

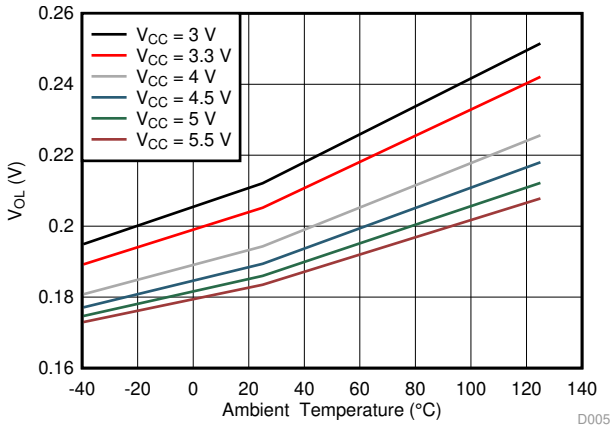


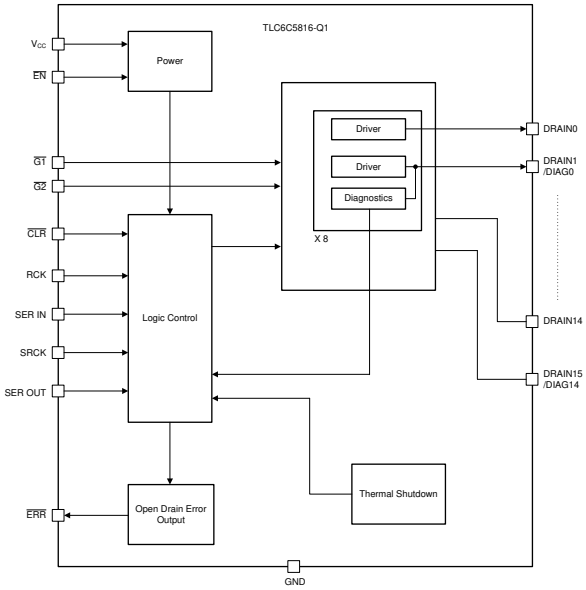
Figure 12. SER OUT Low Voltage vs Temperature (°C)

7 Detailed Description

7.1 Overview

The TLC6C5816-Q1 device is a 16-bit shift-register LED driver designed to support automotive LED applications. A built-in LED-open and LED-short diagnostic mechanism provides enhanced safety protection. The device contains 16 channels with power DMOS transistor outputs, but 8 of the channels can instead be configured by the corresponding DIAGn bits in the Configuration register to support LED fault diagnostics. The diagnostics channels DIAGn must connect to DRAINn to realize LED diagnostics. A command error fault implies that a channel is configured for LED diagnostics, but a register write command has turned on the channel at the same time. The device provides a cyclic redundancy check to verify register values in the shift registers. In readback mode, the device provides 6 bits of the CRC remainder. The MCU can read back the CRC remainder and check if the remainder is correct. This checks whether the communication loop between MCU and device is good.

7.2 Functional Block Diagram



7.3 Feature Description

The features of the TLC6C5816-Q1 device are described in the following sections. Table 1 describes device behavior under different conditions.

Table 1. TLC6C5816-Q1 Behavior Under Different Conditions

		CONFIGURATION REGISTERS	STATUS REGISTERS	OUTPUTS 0-7	OUTPUTS 8-15	DEVICE CURRENT
$\overline{EN}$ = HIGH	$\overline{CLR}$ = X	Clear	Clear	Hi-Z	Hi-Z	Low $I_{(Q)}$
$\overline{EN}$ = LOW	$\overline{CLR}$ = LOW	Clear	Clear	Hi-Z	Hi-Z	Active current
	$\overline{CLR}$ = HIGH	Set by interface	Set by fault detection	Controlled by configuration and $\overline{G1}$ level	Controlled by configuration and $\overline{G2}$ level	Operation current

7.3.1 Device Enable ($\overline{EN}$)

The TLC6C5816-Q1 device provides a low $I_{(Q)}$ mode. A high $\overline{EN}$ level shuts down the device, all the registers reset, and the device enters standby mode. A low $\overline{EN}$ level enables the device, and all functions work normally.

7.3.2 Gated Output ($\overline{Gx}$)

The device provides two active-low inputs to control gated outputs. $\overline{G1}$ turns channels DRAIN0–DRAIN7 on and off, and $\overline{G2}$ turns channels DRAIN8–DRAIN15 on and off.

7.3.3 Register Clear ($\overline{CLR}$)

The device provides a convenient function for clearing registers. A low $\overline{CLR}$ input level clears all internal registers and all fault states. A high $\overline{CLR}$ level makes the device work normally.

7.3.4 Open-Drain Outputs and Flexible Diagnostics Channel

The device provides 16 output channels. All 16 channels have integrated low-side switches to drive external loads such as LEDs independently. Eight channels have integrated voltage comparators dedicated for LED-open and -short diagnostics as depicted in the following sections.

7.3.4.1 Configurable Outputs

The 16 channels are divided into eight pairs of outputs like DRAIN0, DRAIN1/DIAG0 as shown in Figure 13. By default, both outputs of this pair are open-drain outputs. Each of the pair is independent from the other.

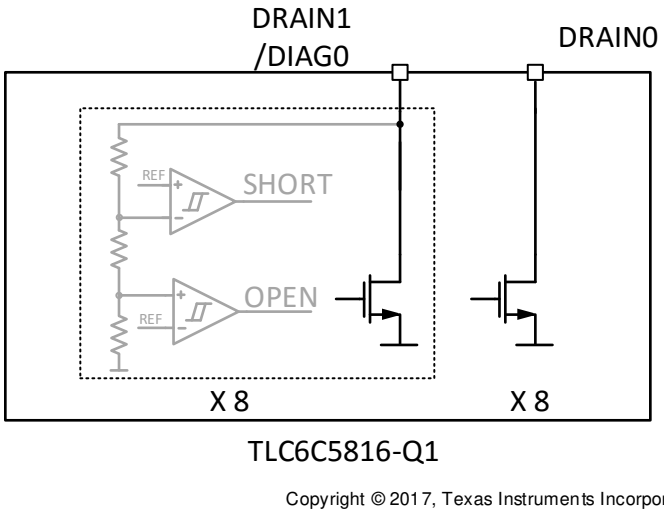


Figure 13. Open-Drain Output and Flexible Diagnostics

By setting its bit in the configuration register to HIGH, the DRAIN1/DIAG0 output can be configured as diagnostics channel DIAG0 for DRAIN0.

By setting the configuration register to LOW, DRAIN1/DIAG0 can be configured as the independent open-drain output DRAIN1.

If DRAIN1/DIGA0 is configured as a diagnostics channel, when DRAIN0 is on, the DRAIN1/DIAG0 diagnostics path monitors the voltage. When DRAIN0 is off, DRAIN1/DIAG0 is in the high-impedance state to avoid any leakage current.

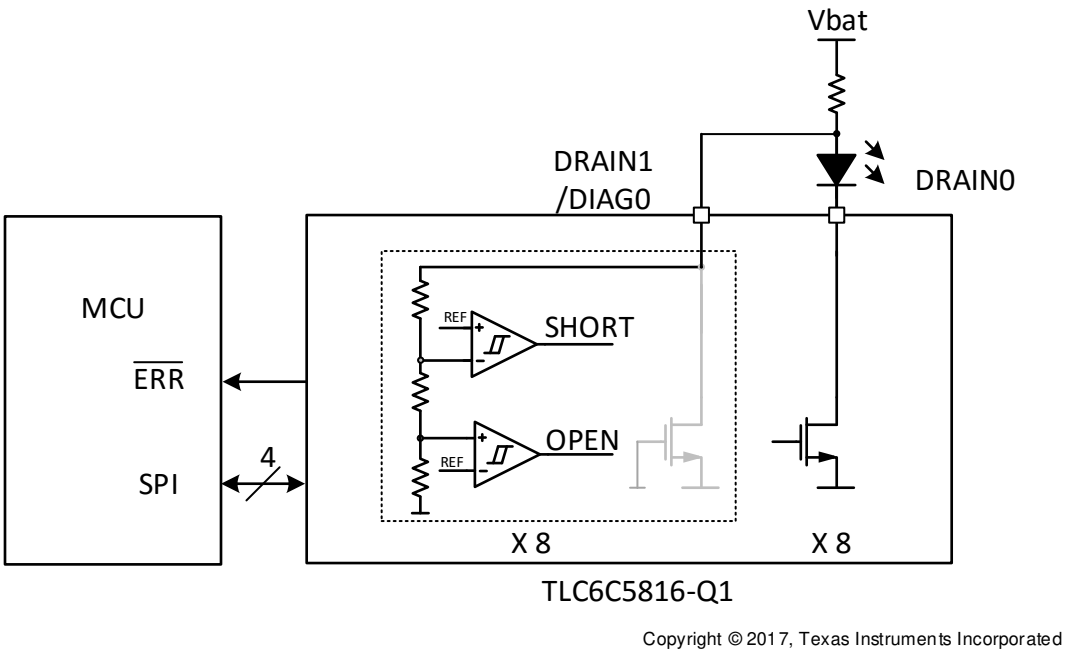


Figure 14. Diagnostics Configuration of Output Driver Pair

7.3.4.2 LED-Open Diagnostics

As depicted in *Configurable Outputs*, the DIAG0 channel monitors the anode voltage of the LED load of DRAIN0. When the DRAIN0 channel turns on, DIAG0 compares the DRAIN0 voltage with internal threshold for LED-open detection, $V_{(OC\_th)}$. When DRAIN0 is on, and $V_{(DIAG0)}$ is continuously higher than $V_{(OC\_th)}$ for $t_{pd(deg\_open)}$, the device asserts an LED-open fault, sets the corresponding bit in the fault table, and pulls $\overline{ERR}$ low.

An LED-open fault does not turn off the channel automatically in the LED-open state. Once the device detects an open fault, it latches the fault status in the DIAGn_OPEN fault register. The fault register value only recovers to normal when the LED fault disappears and the fault status is read back. Cycling $\overline{Gx}$ on and off does not clear the fault.

7.3.4.3 LED-Short Diagnostics

As depicted in *Configurable Outputs*, the DIAG0 channel monitors the LED anode voltage of DRAIN0. When the DRAIN0 channel is turned on, DIAG0 compares the DRAIN0 voltage with the internal threshold for LED short detection, $V_{(SC\_th)}$. When DRAIN0 is on and $V_{(DIAG0)}$ is continuously lower than $V_{(SC\_th)}$ for $t_{pd(deg\_short)}$, the device asserts an LED-short fault, sets the corresponding bit in the fault flag table, and pulls $\overline{ERR}$ low.

The device does not turn off the channel automatically in LED-short state. Once device detects a short fault, it latches the fault state in the DIAGn_SHORT fault register. The fault register value only recovers to normal when LED fault disappears and the fault status is read back. Cycling $\overline{Gx}$ on and off does not clear the fault.

7.3.5 Thermal Shutdown

The TLC6C5816-Q1 device has an internal thermal sensor that monitors device temperature. Once the thermal sensor detects device overtemperature, it disables all channel outputs and sets the TSD flag in the Fault Readback register. The fault register value only recovers to normal when the overtemperature fault disappears and the fault status is read back.

7.3.6 Command Error

The diagnostics configuration for $DRAIN_{n+1}$ and $DIAG_n$ cannot be set to open-drain output mode and diagnostics mode at the same time. If the device detects both of the registers have been set high for any channel, the device sets the CMD_ERR flag HIGH and pulls the open-drain error flag $\overline{ERR}$ pin low. Furthermore, the device ignores the $DIAG_n$ setting and drives the channel in open-drain output mode. To reset the CMD_ERR flag, correct the register configuration value and read out the fault register value.

7.3.7 Serial Communication Error

The device provides a cyclic redundancy check to verify register values in the shift registers. In readback mode, the device provides 6 bits of the CRC remainder. The MCU can read back the CRC remainder and check if the remainder is correct to determine whether the communication loop between MCU and device is good. *Shift-Register Communication-Fault Detection* gives a detailed description of the CRC check.

7.3.8 Error Feedback

If any of the fault flags is high, $\overline{ERR}$ is pulled down. The MCU can detect the device fault by this pin, read out fault flags, and take actions accordingly. The first RCK rising edge latches the fault registers into shift registers. The status information shifts toward SER OUT at the falling edge of SRCK.

7.3.9 Interface

The TLC6C5816-Q1 device contains a 24-bit shift-register serial interface that feeds a 24-bit D-type storage register. Data transfer through the shift and storage registers is on the rising edge of the shift register clock (SRCK) and register latch signal (RCK), respectively. The storage register transfers data to the output buffer when device enable ($\overline{EN}$) is low and shift register clear ($\overline{CLR}$) is high.

7.3.9.1 Register Write

The TLC6C5816-Q1 device has a 24-bit configuration register. Data transfers through the shift registers on the rising edge of SRCK and latches into the storage registers on the rising edge of RCK. The first 8 data bits control the diagnostics channel configuration, and the following 16 data bits control 16 open-drain outputs independently.

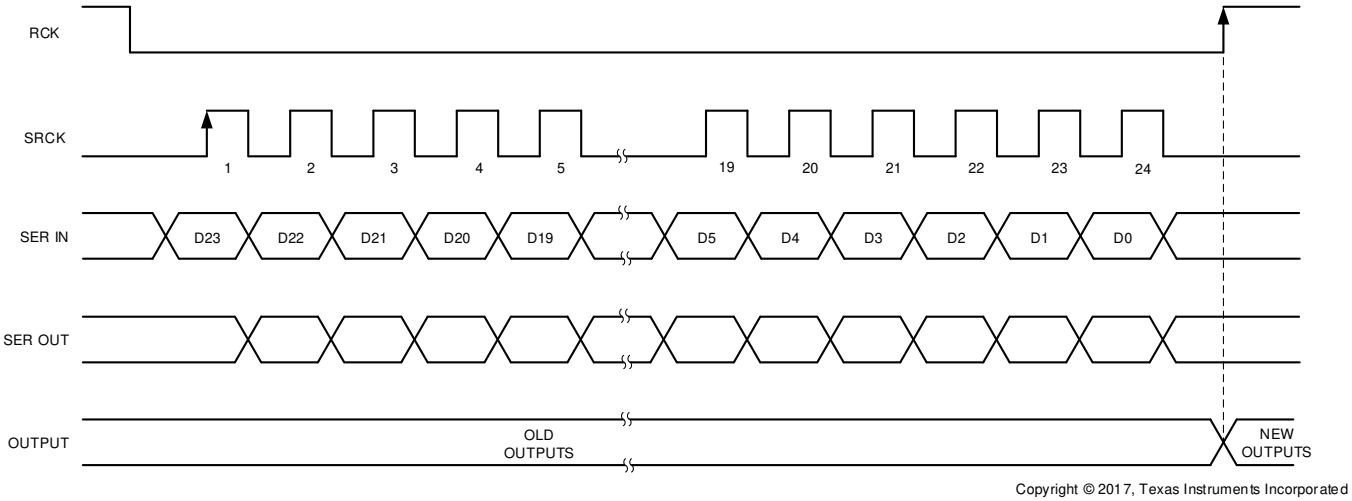


Figure 15. Register Write Timing Diagram

The $DRAIN_{n+1}$-$DIAG_n$ channel configuration is controlled by the $DIAG_n$ registers. These channels can be set to either open-drain output or diagnostics input mode. The TLC6C5816-Q1 device does not allow the user to set $DRAIN_{n+1}$ and $DIAG_n$ high at the same time, because the divider resistor for LED diagnostics can result in leakage current on the LED, which lights up the LED. If the DIAGn and DRAINn registers are set to high at the same time, the channel operates as an open-drain output instead of LED diagnostics, and a command error latches in the fault registers, which can be read back by the register readback function as explained in *Register Read*.

7.3.9.2 Register Read

The fault information loads to shift registers on the rising edge of RCK and can be read out on SER OUT. On the rising edge of the RCK signal, the MSB data DIAG14_OPEN appears on the SER OUT pin. On each falling edge of SRCK signal, there is 1 bit of data shifted out on the SER OUT pin. There is a total of 24 bits in the fault information registers. Register Maps describes the details.

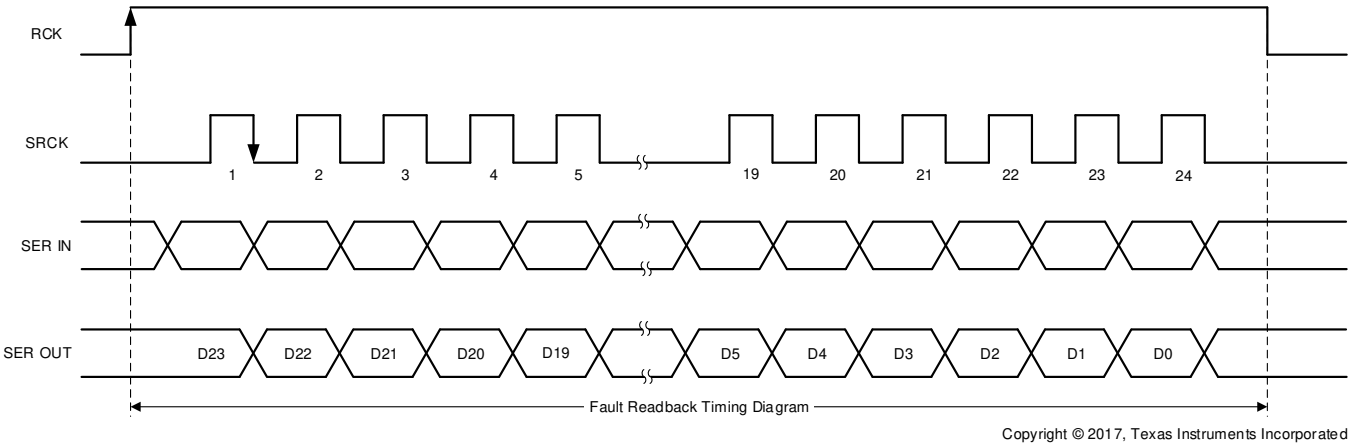


Figure 16. Register Read Timing Diagram

7.3.9.3 Shift-Register Communication-Fault Detection

The TLC6C5816-Q1 device provides a cyclic redundancy check to verify register values in the shift registers. In readback mode, the TLC6C5816-Q1 device provides 6 bits of the CRC remainder. The MCU can read back the CRC remainder and check if the remainder is correct. The CRC checksum provides a readback method to verify shift register values without altering them.

Polynomial: $x^6 + x + 1$ (1)

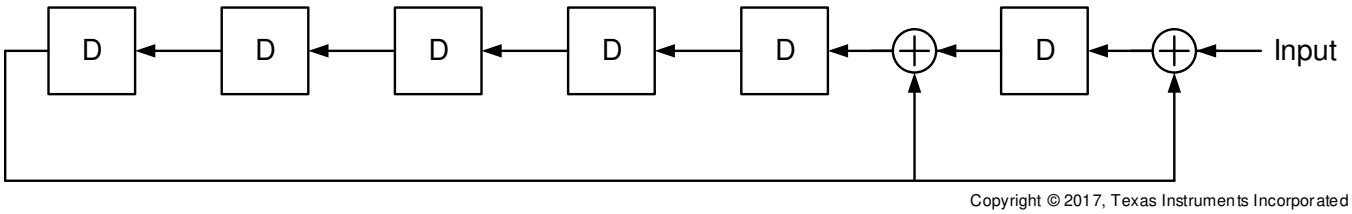


Figure 17. CRC Check Block Diagram

The TLC6C5816-Q1 device also checks the configuration register for faulty commands.

The TLC6C5816-Q1 configuration register consists of 24 bits. To generate the CRC checksum, the device first shifts left 6 bits and appends 0s, then bit-wise exclusive-ORs the 30 data bits with the polynomial to get the checksum.

For example, if the configuration data is 0xD7 0F68 and the polynomial is 0x43 (7'b100 0011), the CRC checksum is 0x19 (6'b01 1001).

The MCU can read back the CRC checksum and append it to the LSB of 24 bits, and then the 30 bits of data becomes 0x35C3 DA19. Performing the bit-wise exclusive-OR operation with the polynomial should lead to a residual of 0.

CRC reference: *CRC Implementation With MSP430*

7.3.9.4 Clear Register

A logic low on $\overline{CLR}$ clears all registers in the device. TI suggests clearing the device registers during power up or initialization.

7.3.9.5 Register Clock

RCK is the storage-register clock. Data in the storage register appears at the output whenever the output enable ($\overline{G1}$ and $\overline{G2}$) input signals are low.

7.4 Device Functional Modes

7.4.1 Normal Operation

To make the device operate normally, usually use a 3.3-V or 5-V power supply to power V_{CC}, connect the LED supply voltage to a regulated voltage or directly to the car battery, and make sure the channel current does not exceed 50 mA.

7.4.2 POR Reset

When V_{CC} is lower than $V_{(POR\text{-}falling)}$, the device stops working and enters the power-off mode. When V_{CC} is higher than $V_{(POR\text{-}rising)}$, the device starts to work and sets all registers to their default values.

7.4.3 Standby Mode

When V_{CC} is higher than $V_{(POR\text{-}rising)}$ and $\overline{EN}$ is high, the device enters the standby mode and sets all registers to their default values. The power consumption is very low.

7.5 Register Maps

Table 2. Register Map

CONFIGURATION REGISTER								
Bit	23	22	21	20	19	18	17	16
Field name	DIAG14	DIAG12	DIAG10	DIAG8	DIAG6	DIAG4	DIAG2	DIAG0
Default value	0h	0h	0h	0h	0h	0h	0h	0h
Bit	15	14	13	12	11	10	9	8
Field name	DRAIN15	DRAIN14	DRAIN13	DRAIN12	DRAIN11	DRAIN10	DRAIN9	DRAIN8
Default value	0h	0h	0h	0h	0h	0h	0h	0h
Bit	7	6	5	4	3	2	1	0
Field name	DRAIN7	DRAIN6	DRAIN5	DRAIN4	DRAIN3	DRAIN2	DRAIN1	DRAIN0
Default value	0h	0h	0h	0h	0h	0h	0h	0h
FAULT_READBACK REGISTER								
Bit	23	22	21	20	19	18	17	16
Field name	DIAG14_OPEN	DIAG14_SHORT	DIAG12_OPEN	DIAG12_SHORT	DIAG10_OPEN	DIAG10_SHORT	DIAG8_OPEN	DIAG8_SHORT
Default value	0h	0h	0h	0h	0h	0h	0h	0h
Bit	15	14	13	12	11	10	9	8
Field name	DIAG6_OPEN	DIAG6_SHORT	DIAG4_OPEN	DIAG4_SHORT	DIAG2_OPEN	DIAG2_SHORT	DIAG0_OPEN	DIAG0_SHORT
Default value	0h	0h	0h	0h	0h	0h	0h	0h
Bit	7	6	5	4	3	2	1	0
Field name	TSD	CMD_ERR	CRC					
Default value	0h	0h	0h					

7.6 Interface Registers

Table 3 lists the memory-mapped registers for the interface.

Table 3. Interface Registers

OFFSET	ACRONYM	REGISTER NAME	SECTION
0h	Config	Configuration Register	Go
1h	Fault_Readback	Fault Readback Register	Go

Complex bit access types are encoded to fit into small table cells. Table 4 shows the codes that are used for access types in this section.

Table 4. Interface Access Type Codes

	CODE	DESCRIPTION
Read type	R	Read-only
Read to clear	RC	Read to clear the fault
Write type	W	Write-only
Reset or Default Value	*-n*	Value after reset or the default value

7.6.1 Configuration Register (Offset = 0h) [reset = 0h]

Config is shown in Figure 18 and described in Table 5.

Return to Summary Table.

Figure 18. Configuration Register

23	22	21	20	19	18	17	16
DIAG14	DIAG12	DIAG10	DIAG8	DIAG6	DIAG4	DIAG2	DIAG0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
15	14	13	12	11	10	9	8
DRAIN15	DRAIN14	DRAIN13	DRAIN12	DRAIN11	DRAIN10	DRAIN9	DRAIN8
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h
7	6	5	4	3	2	1	0
DRAIN7	DRAIN6	DRAIN5	DRAIN4	DRAIN3	DRAIN2	DRAIN1	DRAIN0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

Table 5. Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
23	DIAG14	W	0h	Diagnostics configuration bit for DRAIN15 and DIAG14 HIGH = Diagnostics enabled as DIAG14 LOW = Diagnostics disabled as DRAIN15
22	DIAG12	W	0h	Diagnostics configuration bit for DRAIN13 and DIAG12 HIGH = Diagnostics enabled as DIAG12 LOW = Diagnostics disabled as DRAIN13
21	DIAG10	W	0h	Diagnostics configuration bit for DRAIN11 and DIAG10 HIGH = Diagnostics enabled as DIAG10 LOW = Diagnostics disabled as DRAIN11
20	DIAG8	W	0h	Diagnostics configuration bit for DRAIN9 and DIAG8 HIGH = Diagnostics enabled as DIAG8 LOW = Diagnostics disabled as DRAIN9
19	DIAG6	W	0h	Diagnostics configuration bit for DRAIN7 and DIAG6 HIGH = Diagnostics enabled as DIAG16 LOW = Diagnostics disabled as DRAIN7
18	DIAG4	W	0h	Diagnostics configuration bit for DRAIN5 and DIAG4 HIGH = Diagnostics enabled as DIAG4 LOW = Diagnostics disabled as DRAIN5

Table 5. Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17	DIAG2	W	0h	Diagnostics configuration bit for DRAIN3 and DIAG2 HIGH = Diagnostics enabled as DIAG2 LOW = Diagnostics disabled as DRAIN3
16	DIAG0	W	0h	Diagnostics configuration bit for DRAIN1 and DIAG0 HIGH = Diagnostics enabled as DIAG0 LOW = Diagnostics disabled as DRAIN1
15	DRAIN15	W	0h	Open-drain output control bit for DRAIN15 and DIAG14 HIGH = Output power switch enabled LOW = Output power switch disabled
14	DRAIN14	W	0h	Open-drain output control bit for DRAIN14 HIGH = Output power switch enabled LOW = Output power switch disabled
13	DRAIN13	W	0h	Open-drain output control bit for DRAIN13 and DIAG12 HIGH = Output power switch enabled LOW = Output power switch disabled
12	DRAIN12	W	0h	Open-drain output control bit for DRAIN12 HIGH = Output power switch enabled LOW = Output power switch disabled
11	DRAIN11	W	0h	Open-drain output control bit for DRAIN11 and DIAG10 HIGH = Output power switch enabled LOW = Output power switch disabled
10	DRAIN10	W	0h	Open-drain output control bit for DRAIN10 HIGH = Output power switch enabled LOW = Output power switch disabled
9	DRAIN9	W	0h	Open-drain output control bit for DRAIN9 and DIAG8 HIGH = Output power switch enabled LOW = Output power switch disabled
8	DRAIN8	W	0h	Open-drain output control bit for DRAIN8 HIGH = Output power switch enabled LOW = Output power switch disabled
7	DRAIN7	W	0h	Open-drain output control bit for DRAIN7 and DIAG6 HIGH = Output power switch enabled LOW = Output power switch disabled
6	DRAIN6	W	0h	Open-drain output control bit for DRAIN6 HIGH = Output power switch enabled LOW = Output power switch disabled
5	DRAIN5	W	0h	Open-drain output control bit for DRAIN5 and DIAG4 HIGH = Output power switch enabled LOW = Output power switch disabled
4	DRAIN4	W	0h	Open-drain output control bit for DRAIN4 HIGH = Output power switch enabled LOW = Output power switch disabled
3	DRAIN3	W	0h	Open-drain output control bit for DRAIN3 DIAG2 HIGH = Output power switch enabled LOW = Output power switch disabled
2	DRAIN2	W	0h	Open-drain output control bit for DRAIN2 HIGH = Output power switch enabled LOW = Output power switch disabled
1	DRAIN1	W	0h	Open-drain output control bit for DRAIN1 DIAG0 HIGH = Output power switch enabled LOW = Output power switch disabled
0	DRAIN0	W	0h	Open-drain output control bit for DRAIN0 HIGH = Output power switch enabled LOW = Output power switch disabled

7.6.2 Fault Readback Register (Offset = 1h) [reset = 0h]

Fault_readback is shown in Figure 19 and described in Table 6.

Return to Summary Table.

Figure 19. Fault_Readback Register

23	22	21	20	19	18	17	16
DIAG14_OPEN	DIAG14_SHORT	DIAG12_OPEN	DIAG12_SHORT	DIAG10_OPEN	DIAG10_SHORT	DIAG8_OPEN	DIAG8_SHORT
RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h
15	14	13	12	11	10	9	8
DIAG6_OPEN	DIAG6_SHORT	DIAG4_OPEN	DIAG4_SHORT	DIAG2_OPEN	DIAG2_SHORT	DIAG0_OPEN	DIAG0_SHORT
RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h	RC-0h
7	6	5	4	3	2	1	0
TSD	CMD_ERR	CRC					
RC-0h	RC-0h	R-0h					

Table 6. Fault Readback Register Field Descriptions

Bit	Field	Type	Reset	Description
23	DIAG14_OPEN	RC	0h	LED-Open fault flag for DRAIN15 and DIAG14, read to clear the fault HIGH = LED-open fault detected LOW = LED-open fault not detected
22	DIAG14_SHORT	RC	0h	LED-short fault flag for DIAG15 and DIAG14, read to clear the fault HIGH = LED-short fault detected LOW = LED-short fault not detected
21	DIAG12_OPEN	RC	0h	LED-open fault flag for DRAIN13 and DIAG12, read to clear the fault HIGH = LED open fault detected LOW = LED-open fault not detected
20	DIAG12_SHORT	RC	0h	LED-short fault flag for DIAG13 and DIAG12, read to clear the fault HIGH = LED-short fault detected LOW = LED-short fault not detected
19	DIAG10_OPEN	RC	0h	LED-open fault flag for DRAIN11 and DIAG10, read to clear the fault HIGH = LED-open fault detected LOW = LED-open fault not detected
18	DIAG10_SHORT	RC	0h	LED-short fault flag for DIAG11 and DIAG10, read to clear the fault HIGH = LED-short fault detected LOW = LED-short fault not detected
17	DIAG8_OPEN	RC	0h	LED-open fault flag for DRAIN9 and DIAG8, read to clear the fault HIGH = LED-open fault detected LOW = LED-open fault not detected
16	DIAG8_SHORT	RC	0h	LED-short fault flag for DIAG9 and DIAG8, read to clear the fault HIGH = LED-short fault detected LOW = LED-short fault not detected
15	DIAG6_OPEN	RC	0h	LED-open fault flag for DRAIN7 and DIAG6, read to clear the fault HIGH = LED-open fault detected LOW = LED-open fault not detected
14	DIAG6_SHORT	RC	0h	LED-short fault flag for DIAG7 and DIAG6, read to clear the fault HIGH = LED-short fault detected LOW = LED-short fault not detected
13	DIAG4_OPEN	RC	0h	LED-open fault flag for DRAIN5 and DIAG4, read to clear the fault HIGH = LED open fault detected LOW = LED-open fault not detected
12	DIAG4_SHORT	RC	0h	LED-short fault flag for DIAG5 and DIAG4, read to clear the fault HIGH = LED-short fault detected LOW = LED-short fault not detected

Table 6. Fault Readback Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
11	DIAG2_OPEN	RC	0h	LED-open fault flag for DRAIN3 and DIAG2, read to clear the fault HIGH = LED-open fault detected LOW = LED-open fault not detected
10	DIAG2_SHORT	RC	0h	LED-short fault flag for DIAG3 and DIAG2, read to clear the fault HIGH = LED-short fault detected LOW = LED-short fault not detected
9	DIAG0_OPEN	RC	0h	LED-open fault flag for DRAIN1 and DIAG0, read to clear the fault HIGH = LED-open fault detected LOW = LED-open fault not detected
8	DIAG0_SHORT	RC	0h	LED-short fault flag for DIAG1 and DIAG0, read to clear the fault HIGH = LED-short fault detected LOW = LED-short fault not detected
7	TSD	RC	0h	Thermal-shutdown detection flag, read to clear the fault HIGH = Thermal shutdown detected LOW = Thermal shutdown not detected
6	CMD_ERR	RC	0h	Serial-interface command error, read to clear the fault HIGH = Command error detected in last serial-interface communication LOW = No command error detected in last serial-interface communication
5–0	CRC	R	0h	CRC checksum of configuration registers

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLC6C5816-Q1 device usually is used to drive LED indicators in automotive cluster applications to convey different kinds of information, such as airbag alert, engine fault, and so forth. Typically there are two types LED indicators, general-purpose indicators and safety-related indicators. General indicators only require a simple turnon and turnoff function. Safety-related indicators require not only LED on-off control, but also LED-open and -short diagnostics. The TLC6C5816-Q1 device is very flexible, as it has 8 configurable LED diagnostics pins, which can be configured as open-drain outputs or LED open- and short-diagnostics pins. By configuring corresponding channels for the LED diagnostics function, the TLC6C5816-Q1 device can provide LED open and short diagnostics to improve the system safety level. The following section describes a typical cluster application.

8.2 Typical Application

Following is a typical automotive cluster application which contains 24 LEDs. Two TLC6C5816-Q1 devices connected in series drive the total of 24 LEDs. The first device drives 8 safety-critical LEDs which require LED diagnostics, and the second device drives 16 general-purpose LEDs which only require simple on-and-off control. An MCU, which controls the two devices through a serial interface and GPIOs, controls channel on-off, PWM dimming, and LED diagnostics functions.

Typical Application (continued)

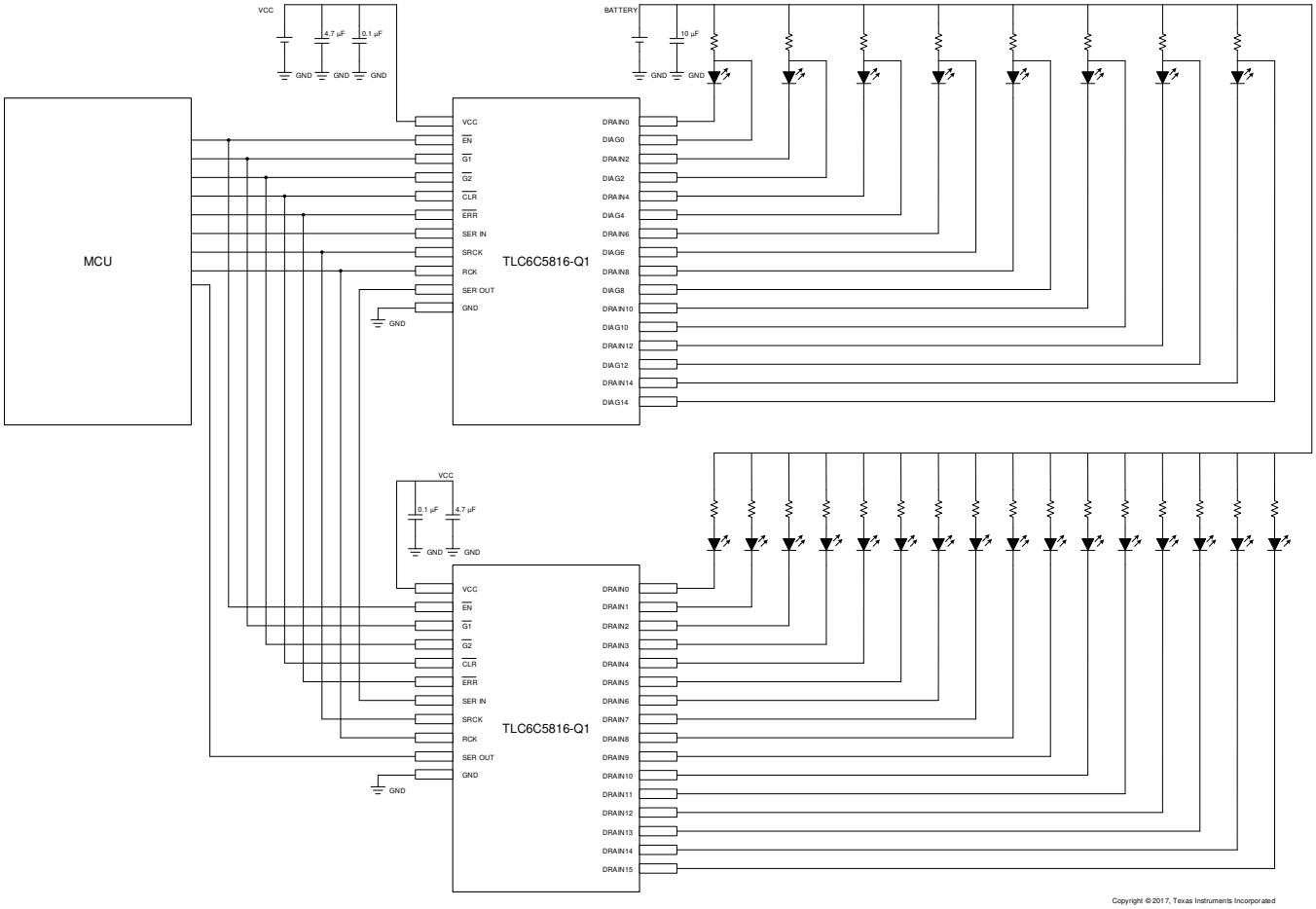


Figure 20. Typical Application Circuit

8.2.1 Design Requirements

Here are the design requirements for the system. The device is powered by 3.3-V voltage. The LED supply is an automotive battery, 12 V typical. Target LED current is 10 mA typical.

Table 7. Design Requirements

Parameter	Value
V_{CC}	3.3 V
$V_{BATTERY}$	12 V typical
I_{LED}	10 mA typical

8.2.2 Detailed Design Procedure

Based on the LED supply voltage, LED forward voltage, and LED output current, calculate the value for the current-setting resistor.

Assume the LED forward voltage is 2 volts, current-setting resistor R = ($V_{BATTERY}$ – V_{LED}) / I_{LED} = 1 kΩ.

8.2.3 Application Curves

This section shows the device normal control waveform and error-state waveform.

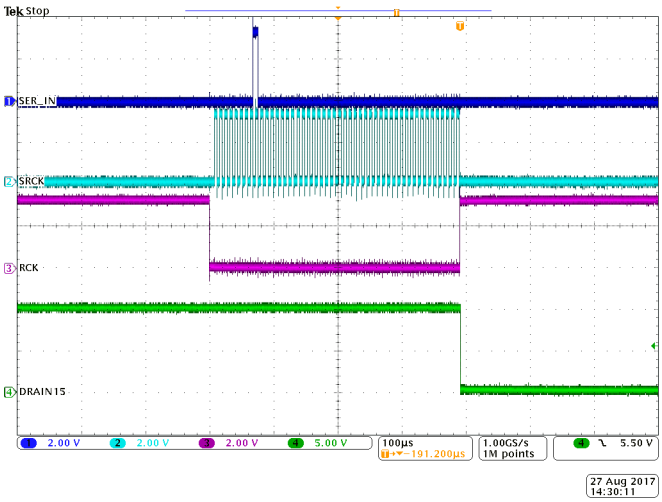


Figure 21. Waveform for Turning On Cascading Device DRAIN15

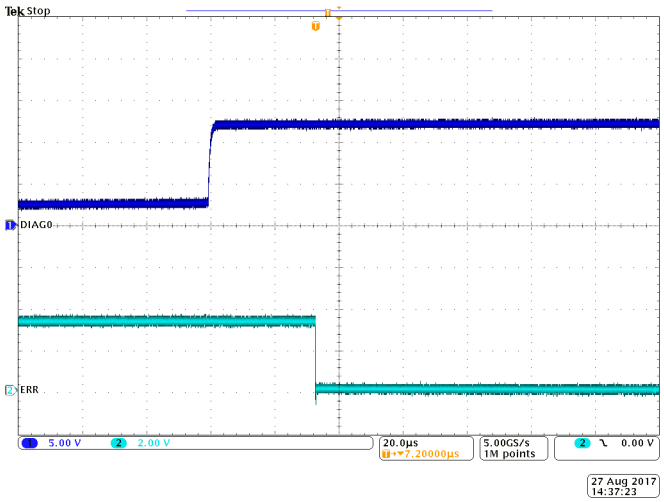


Figure 22. First Device Drain0 Open Waveform

9 Power Supply Recommendations

The supply voltage range is from 3 V to 5.5 V for the TLC6C5816-Q1 device, which typically uses the same supply voltage as the microcontroller, 3.3 V or 5 V. The LED supply voltage can be up to 40 V, so the LED supply can use a car battery directly. Ensure the LED current is no greater than 50 mA during load dump conditions. As the car battery varies a lot, to achieve stable LED brightness, a regulated voltage, for example 5 V, is preferred for the LED supply.

10 Layout

10.1 Layout Guidelines

To enhance the thermal performance, the TLC6C5816-Q1 device is designed with a thermal pad. TI recommends to reserve enough copper area for a heat sink. To minimize the noise interference, it is recommended to put the filter capacitor near the V_{CC} pin. For a detailed layout example, see the following example.

10.2 Layout Example

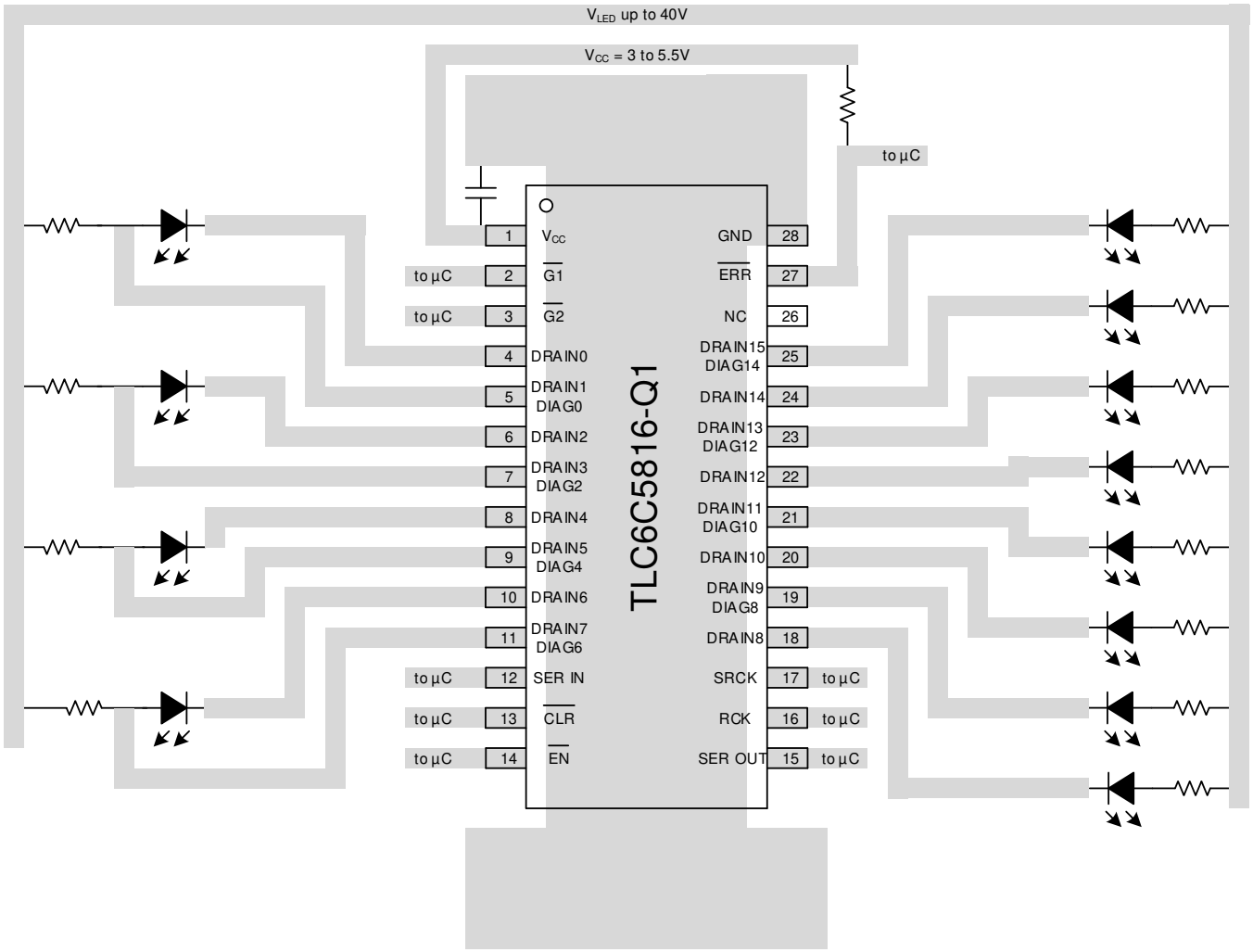


Figure 23. Layout Example

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC6C5816QPWPRQ1	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TLC6C5816	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

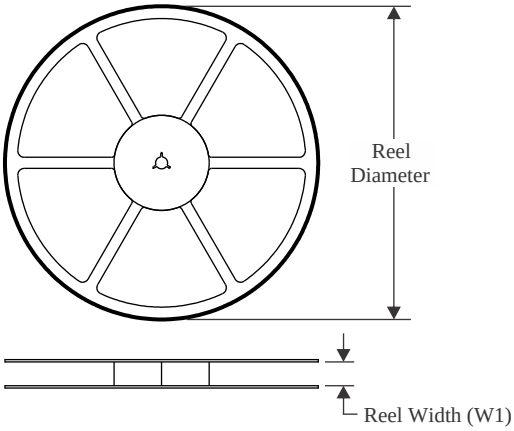
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

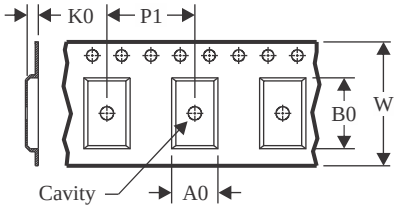
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

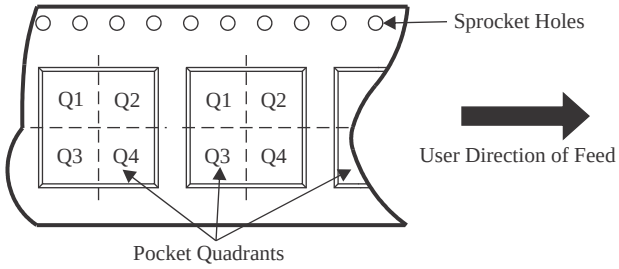


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

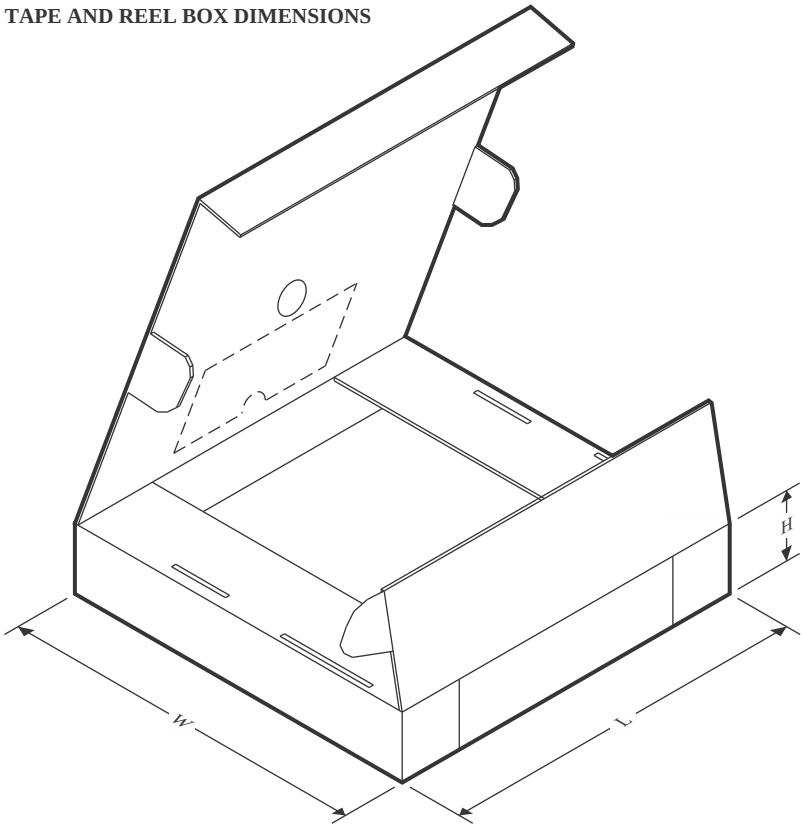
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC6C5816QPWPRQ1	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC6C5816QPWPRQ1	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

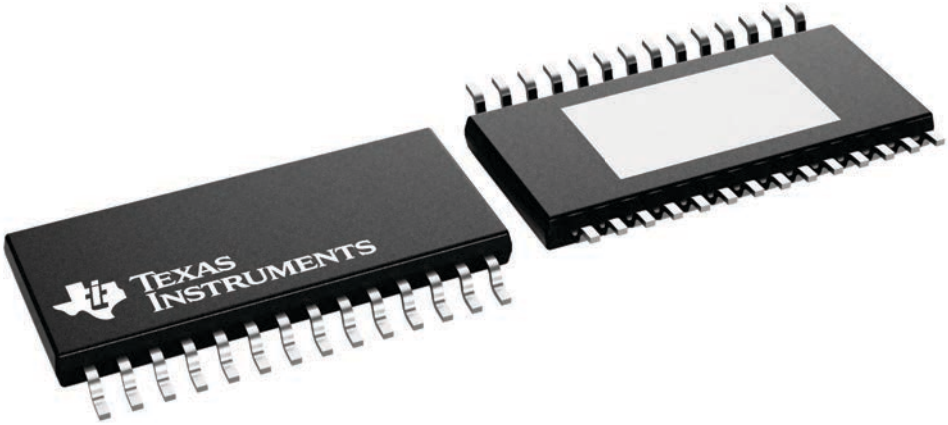
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

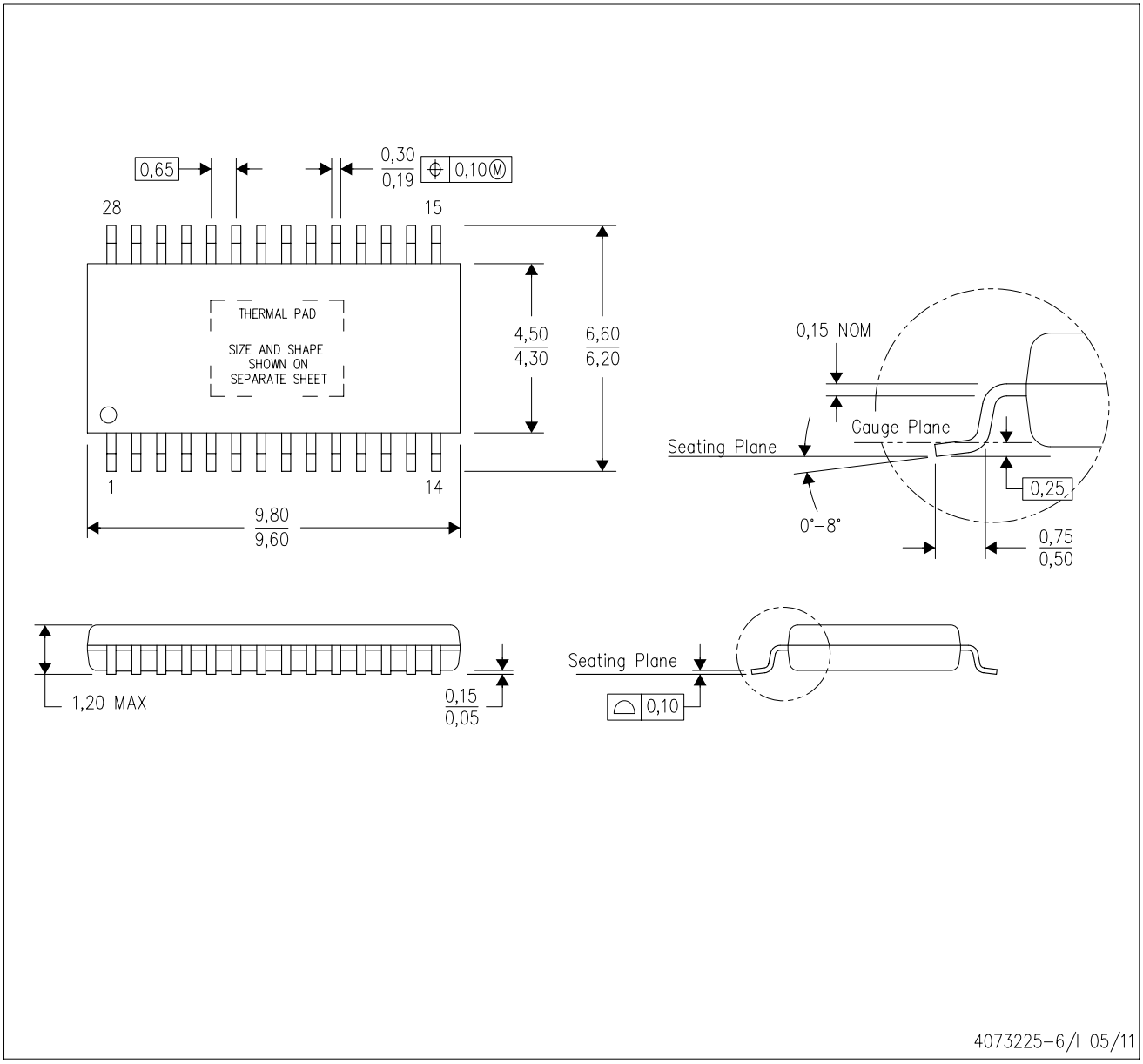
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224765/B

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

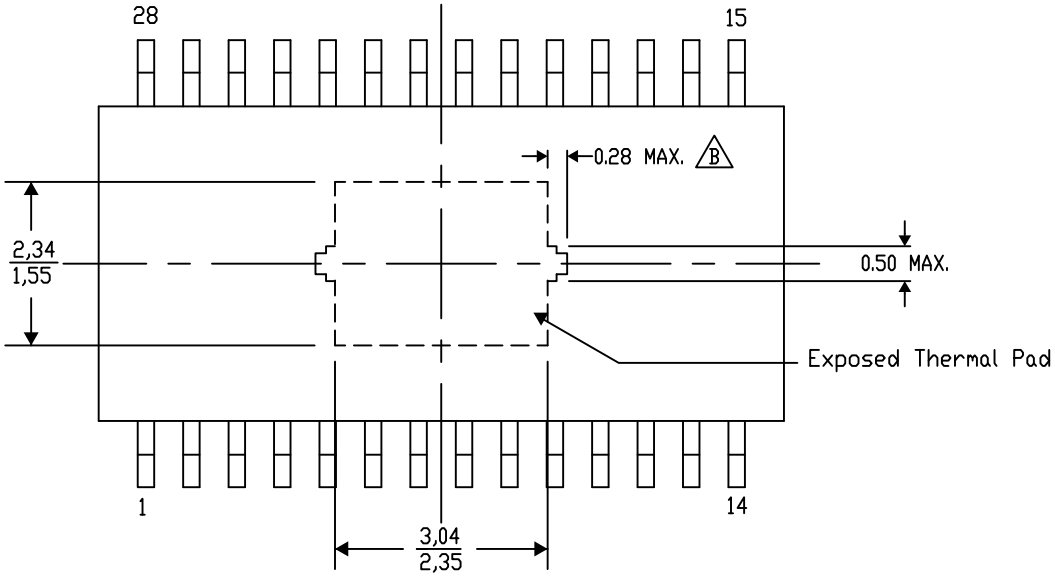
PWP (R–PDSO–G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

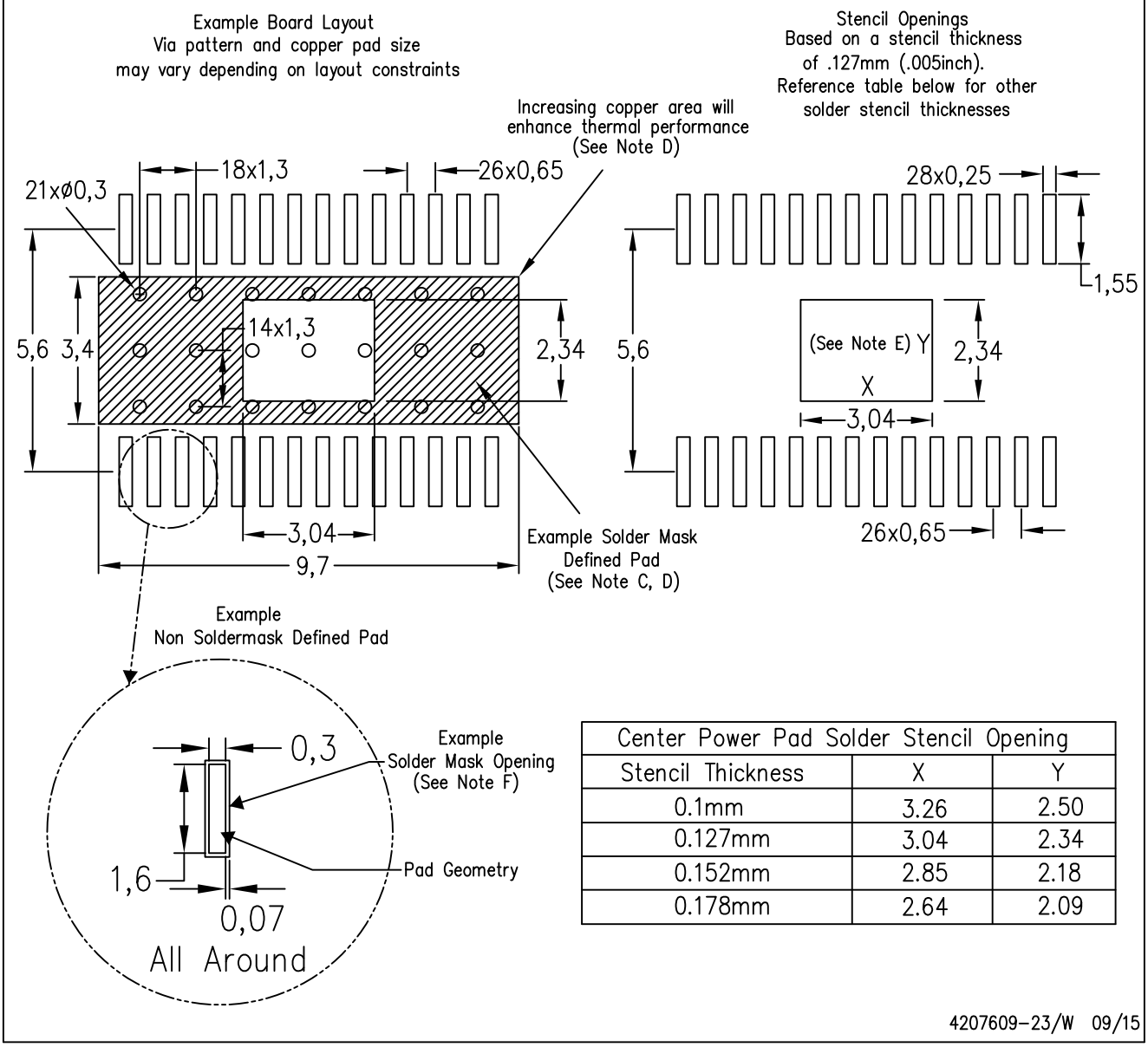
4206332–39/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G28) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.26	2.50
0.127mm	3.04	2.34
0.152mm	2.85	2.18
0.178mm	2.64	2.09

4207609–23/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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