Overtemperature Protection in RS-485 Line Circuits

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ABSTRACT

This application report describes the motivation for, behavior of, and reliability of overtemperature protection in RS-485 line circuits for TIA/EIA-485 physical layer line circuits. The behavior of the bus I/Os during an overtemperature event in the SN65LBC176A RS-485 line circuit is described.

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1 Introduction

Thermal shutdown (TSD) circuitry is implemented as an overtemperature protection circuit on certain physical layer line circuits. The low impedance output driver in RS-485 physical layer line circuits requires a TSD in order to protect them against fault events or improper use. The basic function of the TSD circuit is to sense when the junction temperature (packaged silicon temperature) of a line circuit is above allowable levels and turn off the driver output circuits in order to lower the temperature of the junction back to allowable levels.

TSD circuits should not interfere with normal operation of the line circuit. Specifically, if the line circuit junction temperature does not exceed recommended operating conditions (as specified in the device data sheet of the line circuit), then the TSD should not turn on. TSD turnon during normal operation could cause data transmission to be interrupted because low impedance outputs are typically turned off by a 3-state condition when the TSD triggers. TSD circuits are typically used with other means of fault protection. Because triggering of the TSD is disruptive to data transmission, the TSD is the last mechanism to save the line circuit from destruction.

Having knowledge of how overtemperature protection works as implemented by a TSD can help the reader properly design a system to avoid false triggering of the TSD. With this application report, the reader can become familiar with the reliability of TSDs and with the conditions under which TSD turnon does not occur and its limitations.

2 What is the Motivation for Overtemperature Protection?

2.1 Fault Conditions

2.1.1 Short Circuits

The most common fault condition that causes a TSD to trigger in a line circuit is a short-circuit condition. Short circuits have the potential to raise line circuit junction temperature rapidly to levels beyond recommended operating conditions. The short may be a hard (low-impedance) short or a soft (moderate-impedance) short. The short may occur between a line circuit bus pin and the power supplies (battery, regulated power, or ground) or from a bus-to-bus pin. Figure 1 shows examples of these cases. Hard shorts generally always cause the TSD to trigger in a line circuit with low impedance outputs. This is because the amount of current sunk or sourced by a driver output greatly exceeds the normal current levels. Currents that are an order of magnitude greater than normal operation are typical during hard shorts. For example, RS-485 drivers typically drive about 30 mA during normal operation but can exceed 200 mA during a short. Soft shorts that have moderate impedances may or may not cause the TSD to trigger in a line circuit. Whether the TSD triggers depends on several factors, including impedance of the short, the short voltage, strength of the driver output, the line circuit package and board thermal characteristics, and the duration of the short. Ultimately, when the junction temperature exceeds the TSD trigger point, the TSD turns on and turns off the line driver outputs.

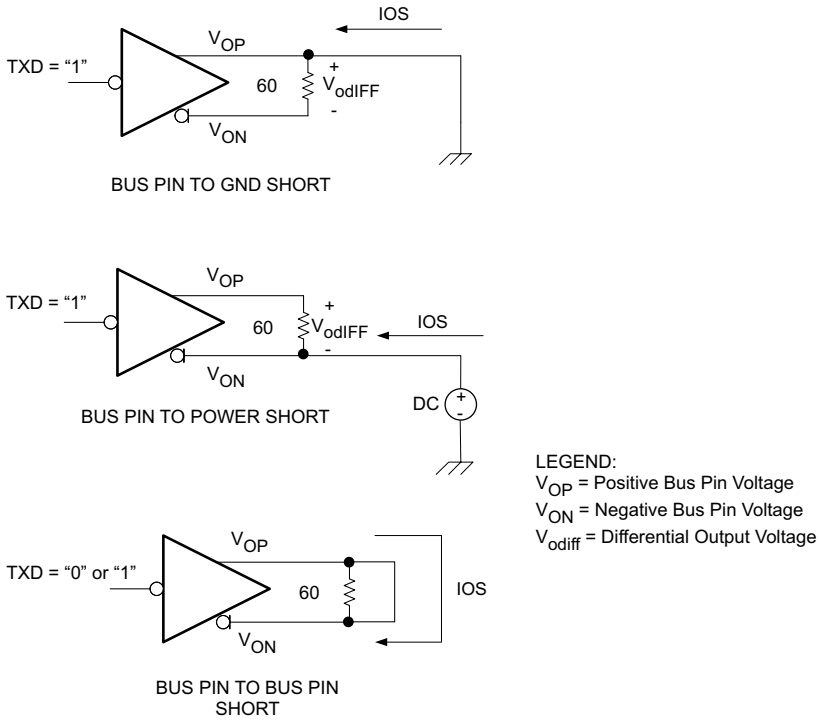


Figure 1. Examples of Short Faults on Line Circuit Driver Outputs (Dual 120-Ω Termination Equivalent Circuit Model)

2.1.2 Bus Contention

Bus contention is a fault event on a data transmission bus that can cause the TSD to trigger in a line circuit. Bus contention occurs when two or more drivers on a single data bus try to drive the bus to opposite states at the same time as shown in Figure 2. This event is simply another form of a short-circuit but it occurs between the bus pins of two or more drivers rather than between bus pins and a power supply or between bus pins of the same driver. Bus contention can be exacerbated by ground offsets as shown in Figure 2. The higher the ground offset, the higher the potential difference between the drivers which can cause higher short-circuit currents up to the point where the driver goes into short-circuit current limiting. The higher the short-circuit current limit, the higher the junction temperature in the line circuit for a given ground offset up to the point where the TSD triggers and regulates the line circuit junction temperature.

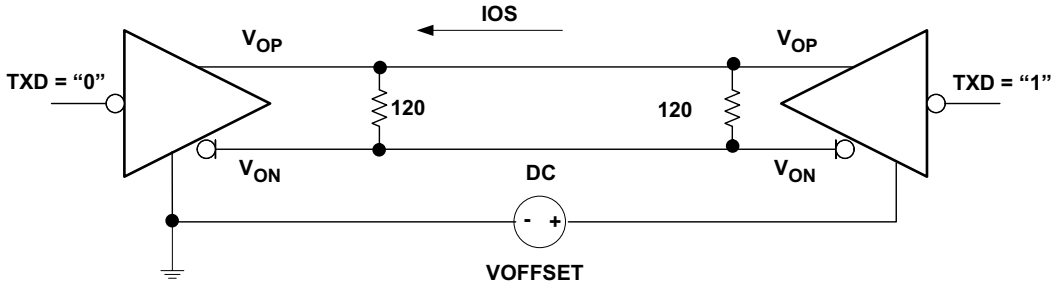
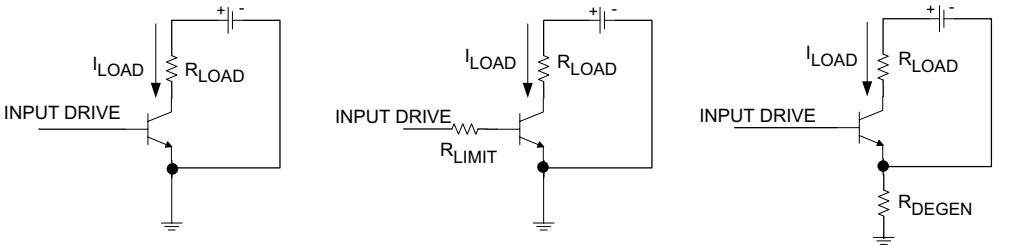


Figure 2. Bus Contention Event Between Two Drivers With a Ground Offset VOFFSET

2.2 Thermal Runaway of the Bipolar Transistor

The bipolar transistor collector current I_C has a positive temperature coefficient. Specifically, if the temperature of a bipolar transistor is higher, then it is able to drive more output current I_C. Higher temperature conditions cause more intrinsic carriers n_i to be available for the bipolar transistor. More current conducts for the same input voltage Vbe because I_C is proportional to n_i.

Because the bipolar transistor drives more output current when it is hotter, it is prone to thermal runaway if the circuit is designed improperly to limit the output current. A simple example is shown in Figure 3a. The bipolar transistor is configured as a common-emitter, low-side driver with a low-valued resistive load. In the case that the current driven by the bipolar transistor in the on-state is such that it causes a junction temperature rise, then the bipolar in turn is able to drive more current. If the higher current causes further junction temperature rise, then a positive feedback mechanism forms that causes the temperature and current to rise without limit until the bipolar transistor is destroyed due to thermal breakdown. This situation can be avoided in several ways, including short-circuit current limiting, emitter degeneration, and/or thermal shutdown. It is not advisable to use a TSD alone to avoid thermal runaway of the bipolar. Short-circuit current (IOS) limiting and emitter degeneration are the first lines of defense against this potentially destructive condition as shown in Figure 3b and Figure 3c. A TSD circuit should be used with these or other effective techniques for maximum fault tolerance to bipolar thermal runaway.



(a) NPN Driving Resistive Load

(b) NPN With IOS Limiting Implemented in Base

(c) NPN With Resistor Degeneration to Lower Gain and Limit IOS

Figure 3. Thermal Runaway Example

2.3 High Ambient Temperatures or High Signaling Rates

High ambient temperatures that cause the junction temperature of a line circuit to go beyond absolute maximum ratings (as specified in the device data sheet of the line circuit) during data transmission is another cause of an overtemperature event. The TSD works to lower the junction temperature of the line circuit if the line circuit is powered and pulling enough supply current to raise the junction temperature significantly above ambient temperature. Because the TSD circuit is designed to turn off drivers, the TSD can help lower the junction temperatures only if the driver of the line circuit is transmitting data.

High signaling rates that cause the junction temperature of a line circuit to go beyond absolute maximum ratings during data transmission is yet another cause of an overtemperature event. The TSD generally works to lower the junction temperature of the line circuit in this case because the high signaling rate of the drivers is the major cause of high line circuit power dissipation. Receivers are typically much lower power than drivers, so when running at high signaling rates, receivers do not cause the junction temperature to rise significantly.

These two potential causes of an overtemperature event can be avoided by following the recommendations of the line circuit supplier to control ambient temperatures, loading conditions, signaling rates, and the thermal environment of the line circuit on the application board. The supplier should give recommended operating conditions and guidelines that bound these parameters such that the line circuit avoids an overtemperature event.

3 Behavior of Overtemperature Protection

3.1 Behavior of Driver Output Current Versus Junction Temperature in the SN65LBC176A

Line circuits are designed with TSD circuits in order to protect against certain fault events. The most common fault events that cause a high junction temperature are short circuits and bus contention. In either case, placing the driver output in a 3-state condition keeps the line circuit from failing permanently due to a thermal event because it regulates the high junction temperature caused by the short circuit or bus contention event to allowable short-term levels. Figure 4 shows the output current of a driver versus junction temperature. The TSD signals the driver to enter a 3-state condition when the increasing junction temperature trip point is reached, and thus the driver output current is lowered to 0 mA and the junction temperature falls accordingly. Then, when the decreasing junction temperature trip point is reached, the driver turns back on as shown in Figure 4. Note that the hysteresis between the increasing junction temperature trigger point and the decreasing junction temperature trigger point results in the avoidance of chattering and bounce of the TSD circuit output.

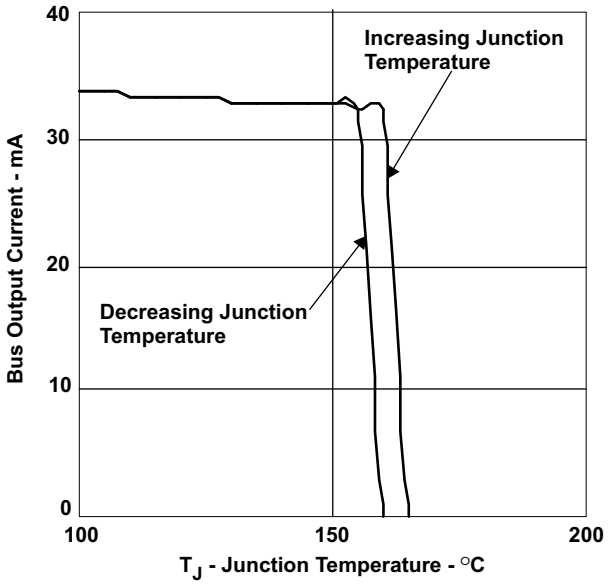


Figure 4. Driver Output Current vs Junction Temperature

3.2 Behavior of Driver Output Current vs Time in the SN65LBC176A During a Short-Circuit Fault Condition

Figure 5 shows the behavior of the output current of the Texas Instruments SN65LBC176A driver versus time under a short-circuit fault event. The test setup is shown in Figure 6. Channel 1 of the oscilloscope plot is the bus pin voltage Vbus. Channel 2 is the short-circuit current Ios in the bus pin that is shorted. At point A, the TSD triggers due to the heating effect of the short circuit on the junction temperature of the line circuit and lowers the current to 0 mA by signaling the driver to enter a 3-state condition. After about 2 µs, the line circuit junction temperature has cooled down and the driver turns back on at point B. If the fault has been removed within about 2 µs after point A, then the driver turns back on and functions normally. However, in this case the short is not removed, so the TSD continues to cycle on and off until the short is removed. Removal of the short returns the driver to normal operation without requiring a power cycling of the line circuit.

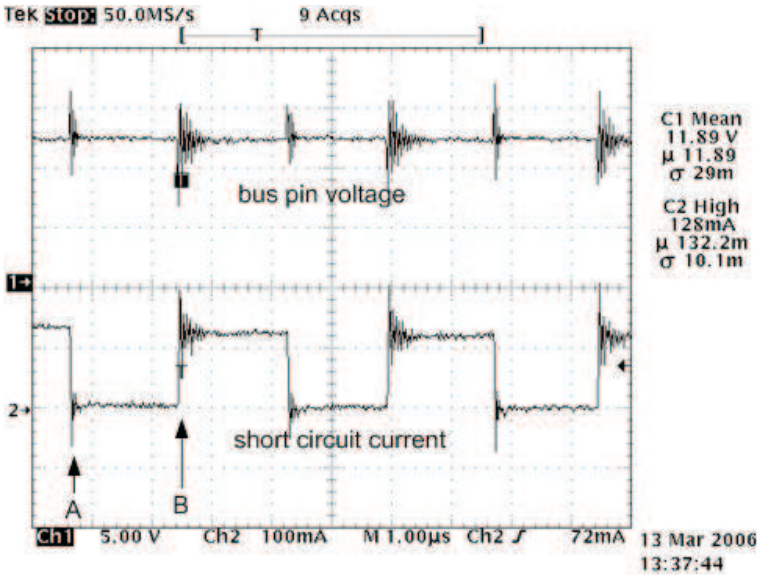


Figure 5. Driver Output Current vs Time During a Short-Circuit Fault

As can be seen in Figure 5, the period of the TSD cycle is about 4 µs. This is calculated by doubling the amount of time between points A and B in the short-circuit current waveform because it is an approximate 50% duty cycle. The power dissipation in the line circuit before the TSD triggers is the voltage times the current to the left of point A which is 12 V × 0.128 A = 1.54 W. Between points A and B, the current is reduced to zero, so the power dissipated in the line circuit due to the short becomes 0 W. Because the duty cycle of the short-circuit current waveform is about 50%, the average power dissipation in the line circuit due to the short is about 0.77 W. This particular data was taken with an ambient temperature of 27°C. Higher ambient temperatures cause the TSD to trigger faster, and the duty cycle of the short-circuit current waveform is reduced, and thus the power dissipated in the line circuit is reduced. The TSD allows less power dissipation at higher ambient temperatures.

Both the current and voltage waveforms in Figure 5 show a noisy signal on transition. This is due to parasitic inductance, bus capacitance, and resistance in the test setup. The parasitic inductance causes an inductive kick which causes the bus voltage to fly high initially. Following the initial voltage kick, the parasitic inductance, bus capacitance, and resistance in the test setup cause the voltage and current waveforms to oscillate and decay by the LRC time constant. This effect is not as pronounced in actual applications where the parasitic inductance is minimized due to transmission line effects.

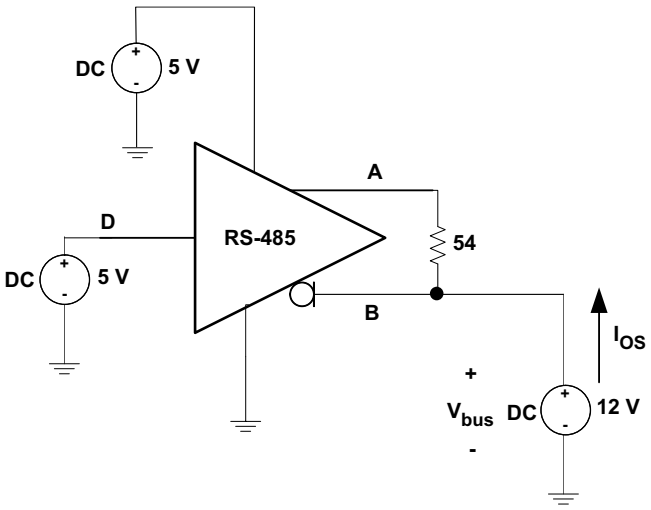


Figure 6. Test Setup for Driver Output Current vs Time During a Short-Circuit Fault Event

3.3 Intended Purpose of Thermal Shutdown Circuits in Line Circuits

Although the TSD circuit prevents destruction of the line circuit under certain short-term fault conditions, it may not keep a line circuit from failing due to long-term reoccurrence of these types of fault events like that shown in Figure 5. For example, a TSD circuit is intended to keep a line circuit from failing due to certain short-term faults and only aids in extending long-term reliability. Therefore, the user of line circuits is encouraged to limit the number of short-term fault events to avoid long-term reliability issues.

3.4 Techniques That Aid in Junction Temperature Regulation

Short-circuit (IOS) limiting, voltage mode sensing, and current foldback are three techniques that aid in junction temperature regulation. IOS limiting is often required by data transmission standards such as TIA/EIA-485 (formerly known as RS-485). The intention is to avoid large current draw from power supplies that power line circuits and keep the line circuits from failing immediately due to fault events. Because TSD circuits have long time constants as compared to IOS limiting circuits, the IOS limiting acts as the first line of defense against fault events. IOS circuits essentially work immediately whereas TSD circuits could take 100s of milliseconds to a few seconds to trigger.

Voltage-mode sensing also can be used to turn off driver outputs when the bus I/Os of the line circuit exceed the recommended operating conditions. For example, when a bus pin on an RS-485 line circuit goes beyond +12 V or –7 V, the output can be placed in a 3-state condition under the assumption that a low-impedance fault to a damaging potential is present on the bus. A more often used voltage-mode sensing used with IOS limiting is termed current foldback. As the voltage on the bus is increased beyond the power supplies of the line circuit, the output current of the driver is turned down as shown in Figure 7.

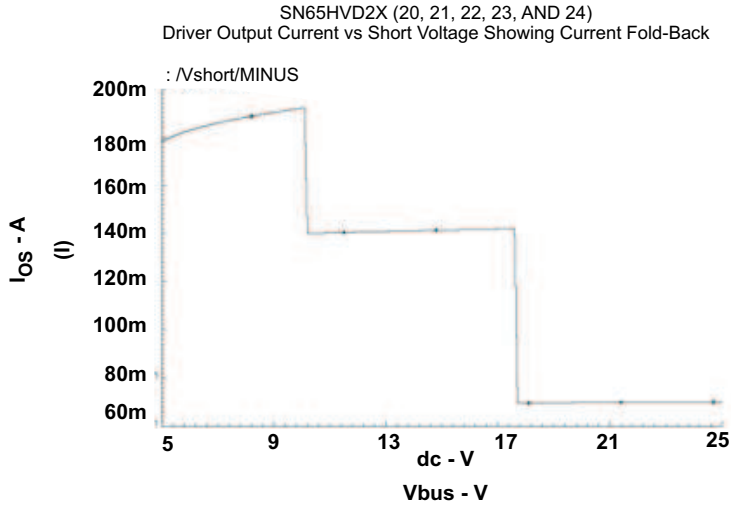


Figure 7. Driver Output Current Foldback vs Short Voltage

Current foldback regulates the amount of power dissipated in the line circuit because as Vbus is increased, Ios is decreased. This type of short-circuit limiting is available on the Texas Instruments SN65HVD2X series of devices, i.e., the SN65HVD20, SN65HVD21, SN65HVD22, SN65HVD23, and SN65HVD24. The idea behind the foldback is not only to limit the power but to keep the driver on when driving into wide common loads such as those supported by the SN65HVD2X series of devices, –20V to +25V. A voltage-mode-only sense would not kick in until beyond the –20-V to +25-V range and would not limit the power within the supported common-mode range. The foldback circuit leads to better reliability of the line circuits versus a voltage-mode-only sense because power is regulated as the common mode is extended.

4 How Reliable is Overtemperature Protection?

In order to properly protect a line circuit, the overtemperature protection as implemented by a TSD needs to be reliable. TSD circuits have been shown to be a reliable means of guarding against overtemperature events in line circuits due to certain fault events as well as many other circuits including voltage regulators. This section discusses the reasons why TSD circuits are reliable.

4.1 Variability of Thermal Shutdown Trigger Points

The theoretical variability of TSD trigger points is a major consideration in judging how reliable the TSD is for protecting against overtemperature events. If the TSD triggers at a temperature that is too high, over-heating could compromise the reliability of the line circuit. If the TSD triggers at a temperature that is too low, it interferes with normal operation of the line circuit. The exact manner in which the TSD is built determines its variability in trigger points. A typical trigger point range is between 150°C and 190°C junction temperature. With a typical value of 165°C, this range represents a variability of about –10% to 15%.

Thermal shutdown trigger points are generally not guaranteed in specifications for line circuits. The reason for this is two-fold. First, a production test on the TSD trigger point would be so long that it would be cost-prohibitive. TSDs can take several hundred milliseconds to a few seconds to trigger due to the thermal time constant of silicon. Typical test time for the entire line circuit is in the low 100s of ms for a RS-485 line circuit; therefore, TSD trigger points are not production-tested. Second, a simulation or manual calculations of the extremes of TSD trigger points are usually not accurate. The reason is that simulation model and process technology data is generally limited to 150°C and below. Because TSD circuits trigger above 150°C, they are not well-modeled in simulators or by manual calculation. TSD

circuits are typically designed by simplified equations, characterized manually, and then adjusted in silicon to the specified trigger point. Simulators can give information on the relative variability of TSD trigger points if the nominal trigger point is purposely adjusted down below 150°C. However, they can not give accurate information on the absolute trigger point unless they are designed to be below 150°C which is not the typical case in a line circuit.

4.2 Semiconductor Materials Maximum Allowed Temperatures

4.2.1 Silicon and Diffusions

Silicon itself is capable of withstanding temperatures much, much greater than 150°C. The melting point of silicon is 1415°C [1]. However, the useful temperature range of silicon is limited by critical temperatures much lower than this. Depending on the doping concentration, a semiconductor goes intrinsic somewhere above 150°C and well below 1415°C in a process technology designed for 150°C operation. When a semiconductor goes intrinsic, it means the doping concentration of the impurities that form the semiconductor junctions are no longer the dominant carrier concentrations because the intrinsic (semiconductor starting material) carriers dominate. Basically, the semiconductor ceases to operate properly. Because packaging materials are the current limiting factor in RS-485 line circuits, the exact temperature when a semiconductor goes intrinsic is not important for this discussion. Packing materials are discussed in section 4.2.3.

4.2.2 Metal System and Latch-Up

Two other considerations for high-temperature operation are electromigration and latch-up. Electromigration is a phenomenon that causes the metal systems, or interconnects, of a semiconductor to become higher resistance when exposed to elevated temperatures and high-current duty cycles for extended periods of time. If enough current is applied long enough at any given temperature, the metal becomes resistive and eventually fuses open and causes a line circuit failure. Elevated temperatures aggravate electromigration problems. Electromigration is a long-term reliability concern and is not associated with short-term faults such as those TSDs are designed to protect against. Line circuits from Texas Instruments are designed to withstand 10 years at 150°C junction temperature with a failure rate of < 50 FITs under duty cycle conditions typical for the application.

Latch-up is a phenomena by which an I/O or the power supply of the line circuit draws a large amount of current, typically 100s of mAs, from a source connected to the I/O or the line circuit power supplies. Latch-up can happen when a pin is taken beyond its absolute maximum ratings for too long or by an AC signal coupling mechanism. Examples are transients on the power supplies that trigger a latch-up within the line circuit and ringing on I/Os that couple in enough energy to latch-up the I/O. Latch-up can be destructive or merely disruptive depending on the impedance of the latched pin, the impedance and compliance of the source or power supplies involved in the latch-up, and the junction temperature. By definition, a soft latch-up does not destroy a line circuit, but a power reset is necessary to clear it. Because latch-up events are caused by bipolar junctions within a semiconductor, they are easier to induce at elevated temperatures because bipolar gain is an increasing function of temperature. A TSD circuit can help prevent latch-up by keeping the junction temperature of a line circuit at a reasonable level, but this is not the TSD circuit's main purpose.

4.2.3 Packaging Materials

Packaging materials in leaded packages such as the lead-frame, mold compound, and bond-wires require consideration for overtemperature stress. These materials are typically good for short-term thermal events such as soldering well above 200°C. Emerging green and lead-free mold compounds that support high-temperature soldering enable soldering at 260°C with a moisture sensitivity level of 1 for many products. This means no special storage (controlled temperature and humidity) is necessary to solder at 260°C for a limited number of cycles. However, green and lead-free mold compounds also can introduce lower ratings for high-temperature storage life (HTSL). Non-lead-free mold compounds in an 8-pin SOIC packages are typically rated between 145°C–150°C for 10 years. This means the IC can be stored or

operated with a junction temperature of about 145°C–150°C for 10 years without suffering any significant reliability issues. The emerging green and lead-free mold compounds limit the HTSL to about 140°C maximum for 10 years unless other steps are taken to raise this performance level such as using Cu bond-pads (as opposed to standard Cu-doped aluminum). Research for obtaining 150°C of HTSL for 10 years with a new green mold compound without using Cu bond-pads is a work-in-progress.

4.2.4 Effect of Long-Term Stress at Elevated Temperatures

As mentioned, the emerging green and lead-free mold compounds limit the HTSL performance to about 140°C for 10 years unless other steps are taken to raise this performance level. The first failure mechanism noted in reliability testing is caused by a phenomenon known as Kirkendall voiding. Over time, the ball-bonds that connect the bond-wires to the pads on the semiconductor are weakened by agents in the mold compound. Once the ball-bonds are weakened enough, they become open circuits and ultimately cause the line circuit to fail. Bonding to Cu is far better for resisting Kirkendall voiding than Cu-doped aluminum pads.

Negative bias temperature instability (NBTI) is also a major potential contributor to high-temperature failure of line circuits. NBTI is a phenomenon by which pMOS transistors have large parametric drifts. During NBTI testing, the pMOS is biased with its gate negative and all other terminals at ground potential (see Figure 8) and a high ambient temperature is applied. Parametrics of the pMOS are measured at time zero and throughout testing to determine how far they drift under these conditions, thus the designation NBTI. At high-enough temperatures and biases, pMOS NBTI can limit or completely compromise transistor performance. Notable drifts in threshold voltage Vt, current drive Id, sat, and gate capacitance Cg have been noted [2] due to pMOS NBTI among other effects. nMOS PBTI, that is positive bias temperature instability, is also a minor consideration but pMOS NBTI is typically far worse. pMOS NBTI is especially troublesome in today's submicron technologies and have limited 100% duty cycle junction temperatures to 105°C. RS-485 line circuits are not fabricated in these technologies due to the demands for higher voltage components. NBTI is much less of an issue in the BiCMOS processes that these line circuits are fabricated in, but do at times need consideration.

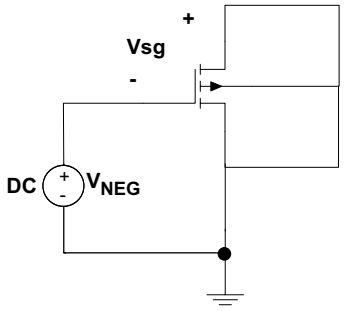


Figure 8. pMOS NBTI Stress Test Configuration

4.2.5 Summary of Semiconductor Materials Maximum Allowed Temperatures

Many factors can be potential issues for line circuits at high junction temperatures. However, HTSL in green and lead-free packaging with standard Cu-doped aluminum bond-pads has the most potential to cause long-term reliability problems because the temperature onset of Kirkendall voiding is lower than electromigration. Latch-up is probably the worst short-term reliability concern because it can cause system interrupts or line circuit destruction.

A TSD circuit regulates the junction temperature in a line circuit but is intended to protect against certain short-term faults such as short circuits. The TSD also aids in latch-up prevention. TSD circuits do have the potential to raise long-term reliability, depending on use conditions. For example, if short circuits are constantly applied to a line circuit, the TSD helps the line circuit last longer, but the TSD cannot be expected to allow a line circuit to operate under fault conditions forever. Per the limitation stated in the absolute maximum ratings of line circuit data sheets, exposure to absolute maximum rated conditions for extended periods may affect device reliability. When a line circuit is in thermal shutdown, this condition qualifies as being beyond absolute maximum ratings because the junction temperature exceeds absolute maximum ratings for junction and/or storage temperature.

5 Summary

TSD circuits in line circuits are designed to avoid destruction of the line circuit under certain short-term faults conditions. Although TSDs may help with long-term reliability, they are not specifically designed to avoid long-term reliability issues. Proper use within the recommended operating conditions of a line circuit is the only reliable way to avoid long-term reliability issues. Short-term operation within the absolute maximum ratings is allowable under fault conditions, but exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Most TSD circuits are designed from empirical measurements because simulators are limited to temperatures lower than TSD trip points. The TSD circuit has a reasonably tight range of trip points and while it should protect a line circuit, it should not interfere with normal operation. Several techniques that react faster than a TSD can be employed to help limit junction temperature in a line circuit. TSDs are the last mechanism to save a line circuit from immediate destruction.

6 References

1. *Microelectronic Circuits and Devices*, M. Horenstein. Prentice Hall (1990), p. 826.
2. *Impact of Negative Bias Temperature Instability on Digital Circuit Reliability*, V. Reddy et al. Microelectronics Reliability 45, (2005) pp. 31-38.

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