Application Report
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TMDS171 Schematic Checklist

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ABSTRACT

This schematic checklist provides a brief explanation of each TMDS171 device pin, and the recommended configuration of TMDS171 device pins for default operation. The TMDS171 device is an HDMI signal to transition-minimized differential signal (TMDS) redtimer supporting digital video interface (DVI) 1.0 and high-definition multimedia interface (HDMI) 1.4 b output signals. The TMDS171 supports four TMDS channels and Digital Display Control (DDC) interfaces. The TMDS171 has the ability to be configured through pin strap or I2C. Use this information to check the connectivity for each TMDS171 device on a system schematic.

This document is intended to aid design at the system level for general applications, but must not be the only resource used. In addition to this list, use the information in the *TMDS171/I 3.4 Gbps TMDS RETIMER*, *TMDS171 RGZ EVM User's Guide* , and associated documents to gain a full understanding of device functionality.

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PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATIONS
Main Link Input Pins				
IN_D[0:2]p/n	2, 3, 5, 6, 8, 9	Main link differential input		Direction connection from sink connector/GPU to TMDS171
IN_CLKp/n	11, 12	Main link clock differential input	Direct connection from sink connector/GPU to TMDS171	
Main Link Output Pins				
OUT_D[0:2]p/n	28, 29, 31, 32, 34, 35	TMDS data differential output	Direct connection from TMDS171 to source connector/sink	
OUT_CLKp/n	25, 26	TMDS clock differential output	Direct connection from TMDS171 to source connector/sink	
Configuration and Miscellaneous Pins				
SDA_SRC	47	Source side TMDS bidirectional DDC data line	Snoop mode, tie it to GND.	
SCL_SRC	46	Source side TMDS bidirectional DDC clock line	Snoop mode, tie it to GND	
SDA_SNK	39	Sink side TMDS bidirectional DDC data line	SDA/SCL from the source is connected directly to the SDA/SCL sink. The TMDS171 needs its SDA_SNK and SCL_SNK pins connected to this link in order to correctly configure the TMDS_CLOCK_RATIO_STATUS bit. Sink application: 47 k pullups to 5 V Source application: 2 k pullups to 5 V	Consider adding an external I2C buffer for DDC capacitance isolation.
SCL_SNK	32	Sink side TMDS bidirectional DDC clock line	SDA/SCL from the source is connected directly to the SDA/SCL sink. The TMDS171 needs its SDA_SNK and SCL_SNK pins connected to this link in order to correctly configure the TMDS_CLOCK_RATIO_STATUS bit. Sink application: 47 k pullups to 5 V Source application: 2 k pullups to 5 V	Consider adding an external I2C buffer for DDC capacitance isolation.
SPDIF_IN	45	SPDIF signal input	500 k pulldown to GND if ARC is not used	
ARC_OUT	44	Audio return channel output	Implementation specific 55 Ω pulldown to GND — resistor may not be needed if it is implemented elsewhere	Leave floating if unused
HOT PLUG DETECT PINS				
HPD_SNK	33	Hot plug detect input from sink side	Connect to HPD output of the display or source connector. For snoop mode: Connect directly to GPU of the sink (check GPU supported voltage). Directly connected HPD line HPD_SNK has internal 190 k pulldown. Consider adding an external switch to isolate potential leakage voltage from sink HPD when sink is off.	Consider adding an external switch to isolate potential leakage voltage from sink HPD when sink is off.
HPD_SRC	4	Hot plug detect output to source side	If HPD_SRC goes to the source connector, a level shifter from 3.3 V to 5 V is needed. If HPD_SRC goes to GPU, check the supported GPU voltages. If HPD snoop mode is implemented, leave HPD_SRC floating.	
CONTROL PINS				
OE	42	Enable/reset pin	Start with 0.2 µF, tune depending on the RC time constant delay (Tr) requirement in regards to power ramp up time.	See Table 1 for different timing values based on capacitance.

PIN NAME	PIN NUMBER(S)	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATIONS
V_{sadj}	22	TMDS-compliant voltage swing control resistor	Start with 7.09 k resistor to ground, resistor value tuning depends on compliance result	
SCL_CTL	15	I2C clock signal	For pin strap mode, 1 k pulldown to GND	2 k pullups to 3.3 V or value required by I2C master in I2C mode
SDA_CTL	16	I2C data signal	For pin strap mode, 1 k pulldown to GND	2 k pullups to 3.3 V or value required by I2C master in I2C mode.
I2C_EN/PIN	10	I2C control mode	65 k (+/- 10%) pulldown to GND for pin strap mode 0 - 65 k (+/- 10%) pullup to 3.3 V for I2C mode	
EQ_SEL/A0	21	I2C address bit 0 or receiver equalization control	For pin strap mode, 65 k (+/- 10%) pullup to 3.3 V, 0 - 65 k (+/- 10%) pulldown to GND, or NC EQ_SEL/A0 = L, Fixed EQ at 7.5 dB EQ_SEL/A0 = NC, Adaptive EQ EQ_SEL/A0 = Fixed EQ at 14 dB	Set address bit 0 in I2C mode
A1	27	I2C address bit 1	For pin strap mode, leave unconnected	Set address bit 1 in I2C mode
SIG_EN	17	Signal detector circuit enable	For pin strap mode, 65 k (± 10%) pullup to 3.3 V or 65 k (+/- 10%) pulldown to GND SIG_EN = L: Signal detect circuit disabled, termination resistors always connected SIG_EN = H: Signal detect circuit enabled, device enters tandby mode when no valid clock detected	
TX_TERM_CTL	16	Transmitter termination control	For pin strap mode, 65 k (± 10%) pullup to 3.3 V or NC TX_TERM_CTL = L, Reserved TX_TERM_CTL = NC, automatically selects termination impedance TERM = H, No transmit termination	Do not pulldown
NC	18, 40	No connect	Leave unconnected	
PRE_SEL	20	De-emphasis control	For pin strap mode, 0 - 65 k (± 10%) pulldown to GND or NC PRE_SEL = L, -2 dB PRE_SEL = NC, 0 dB PRE_SEL = H, Reserved	Do not pullhigh
SWAP/POL	1	Receive Polarity Swap and Receive Lane Swap control	For pin strap mode, 65 k (± 10%) pullup to 3.3 V, 0 - 65 k (+/- 10%) pulldown to GND, or NC SWAP/POL = L, Receive lanes swap (retimer and redriver mode) SWAP/POL = NC, Normal operation SWAP/POL = H, Receive lanes polarity swap (retimer mode only)	
POWER PINS				
VCC	13, 43	3.3 V power supply	One 100 nF cap on each power pin. 4.7 pF and 10 pF on each power node. One bulky cap per power node	
VDD	14, 23, 24, 37, 48	1.2 V power supply	One 100 nF cap on each power pin. 4.7 pF and 10 pF on each power node. One bulky cap per power node	
GND	7, 19, 30, 41	Ground	Connect to board ground	
Thermal Pad	49	Ground	Connect to board ground	

Table 1. Enable (OE) Pin Timing Based on Capacitance

RISE TIME (T_r) (ms)	CAPACITOR VALUE (µF)
25	0.1
50	0.2

Table 1. Enable (OE) Pin Timing Based on Capacitance (continued)

RISE TIME (T_r) (ms)	CAPACITOR VALUE (µF)
100	0.4
200	0.8
500	2

2 References

- *TMDS171/I 3.4 Gbps TMDS RETIMER Datasheet*
- *TMDS171 RGZ Evaluation Module User's Guide*

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