

DP159 and DP149 Configuration Guide

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ABSTRACT

The purpose of this document is to provide a quick start-up guide for the SNx5DP159 and SNx5DP149 devices.

Contents

| | | |
|---|----------------------------------|---|
| 1 | Device Configuration Guide | 1 |
| 2 | Summary..... | 2 |

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1 Device Configuration Guide

1. Choose I2C mode or pin-strap mode via I2C_EN:

- When I2C_EN is high, the device is in I2C mode and the configuration is done through I2C.
- When I2C_EN is low, the device is in pin-strap mode and the configuration is done through the device pins.

2. Choose video mode via HDMI_SEL#:

- In pin-strap mode, when HDMI_SEL# is low, the device is configured for HDMI. If HDMI_SEL# is high, the device is configured for DVI.
- HDMI_SEL# can also be configured with bit 5 in register 0x0Bh in I2C mode. 1'b0 selects HDMI (default) and 1'b1 selects DVI.

3. Choose functional mode via DEV_FUNC_MODE:

In pin-strap mode, the device can automatically configure itself as a redriver at low data rates (<1.0 Gbps) or as a retimer above this data rate. Additional configuration is available using the DEV_FUNC_MODE bits ([1:0] in register 0x0Ah) when the device is in I2C mode.

The DEV_FUNC_MODE bits select the device working function mode:

- 00 – Redriver mode: 250 Mbps – 3.4 Gbps
- 01 – Automatic redriver to retimer crossover at 1.0 Gbps (default)
- 10 – Automatic retimer when HDMI2.0a based upon TMDS_CLOCK_RATIO_STATUS (reserved for SNx5DP149)
- 11 – Retimer mode across full range 250 Mbps to 6 Gbps

The difference between configuration of 0x01 and 0x10 is the crossover frequency for configuration of 0x01 is 1 Gbps while the crossover frequency for configuration of 0x10 is 3.4 Gbps.

When changing between the device configuration modes via Dev_Func_Mode, it is required to toggle the PD_EN bit or the external HPD_SNK for the change to take effect.

When in automatic redriver to retimer mode, it is not required to toggle the PD_EN bit or the external HPD_SNK when the device changes from the redriver to retimer or vice versa.

4. Choose transmit termination via TX_TERM_CTL:

In pin-strap mode (RGZ package only for the DP159), when the TX_TERM_CTL pin is configured as NC, TX_TERM_CTL automatically selects the termination impedance.

- For data rates greater than 3.4 Gbps, TX_TERM_CTL will be set to 75- to 150-Ω differential near-end termination.

- For data rates between 2 Gbps and 3.4 Gbps, TX_TERM_CTL will be set to 150- to 300-Ω differential near-end termination.

- For data rates less than 2 Gbps, TX_TERM_CTL will be set to no termination.

When configured in I2C mode, TX_TERM_CTL bits (Register 0x0Bh, bits [4:3]) need to be set manually.

For data rates less than 3.4 Gbps, TX_TERM_CTL will be set to no termination (value of 0x00h) or 150- to 300-Ω (value of 0x01h) differential near-end termination. For data rates greater than 3.4 Gbps, TX_TERM_CTL will be set to 75- to 150-Ω differential near-end termination (value of 0x11h, DP159 only).

APPLY_RXTX_CHANGES (bit 2 in register 0x0Ah) needs to be set after any changes to the TX_TERM_CTL field.

5. Choose slew rate settings via SLEW_CTL:

- In pin-strap mode, when the SLEW_CTL pin is configured as NC, the slew rate will be at its slowest value of 10 ps. This is recommended as the default setting as the starting point.
- When SLEW_CTL is connected low, the slew rate is 5 ps. When SLEW_CTL is connected high, the slew rate will be at its fastest.
- SLEW_CTL can also be configured with bits [7:6] in register 0x0Bh in I2C mode. 2'b00 is the fastest and 2'b11 is the slowest. APPLY_RXTX_CHANGES (bit 2 in register 0x0Ah) needs to be set after any changes to the SLEW_CTL field.

6. Choose input receive equalization via EQ_SEL:

- In pin-strap mode, when the EQ_SEL pin is configured as NC, the equalization is adaptive. It is recommended to keep this pin as NC to enable adaptive equalization.
- When EQ_SEL is connected low, the equalization is fixed at 7.5 dB. When EQ_SEL is high, the equalization is fixed at 14 dB.
- Equalization control can also be configured in register 0x0Dh in I2C mode.
- APPLY_RXTX_CHANGES (bit 2 in register 0x0Ah) needs to be set after any changes to this register.

7. Choose de-emphasis settings via PRE_SEL:

- In pin-strap mode, when the PRE_SEL pin is configured as NC, no de-emphasis is applied. When PRE_SEL is connected low, 2 dB de-emphasis is applied.
- De-emphasis settings can also be configured with fields [7:5] and [4:2] in register 0x0Ch in I2C mode.
- APPLY_RXTX_CHANGES (bit 2 in register 0x0Ah) needs to be set after any changes to this register.

2 Summary

The guidelines in this application report serve as a starting point for configuring the SNx5DP149 and SNx5DP159 devices for your application.

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