Handshaking Between Adjustable HVDCP Adapters and Battery Chargers

ABSTRACT

Today's battery-powered systems are demanding longer run times. Thanks to higher capacity cells, this goal can be achieved. Additionally, battery technology improvements enable cells to withstand higher charge currents. The combination of these creates a need for fast charging. Adapters are becoming more sophisticated and are providing a higher range of operating voltages to meet the fast charging demand. Examples include high-voltage dedicated charging port (HVDCP) adapters that provide different voltage outputs, such as 5 V, 9 V, or 12 V. Others also offer adjustable voltage output that can be changed on the fly by handshaking with the charger. Achieving a balance in these systems between high-charging currents and charge efficiency can be a complex matter. Texas Instruments provides charger solutions that allow handshaking between adjustable high voltage adapters in order to fine-tune charge efficiency, which achieves better thermal performance overall in fast charging applications.

Trademarks

1 Introduction

This application report showcases one of the implementations for handshaking between an adjustable high-voltage adapter and the bq25890H. This single cell fast charger incorporates a programmable D+/D– output driver in addition to its input current detection scheme that provides the flexibility needed to control adjustable adapters.

2 Programmable D+/D– Output Driver

The bq25890H allows each of the D+/D– lines to be controlled independently to output one of the preset voltage levels (0 V, 0.6 V, 1.2 V, 2.0 V, 2.7 V, 3.3 V, and HiZ). Each line can be set to one of these presets over I^2C. This allows the implementation of a handshaking protocol between the charger and an adapter with an interface that allows adjusting the voltage, such as the CHY100 and CHY103 interfaces.

Since the adapter voltage is controllable, the operating point of the charger can be fine-tuned to ensure high efficiency during charging. In addition, higher voltages allow enabling efficient high-charge currents. As a byproduct, charge time is decreased, making it even more appealing for high-capacity cells.

Register01 of the bq25890H includes the bits needed to control the D+/D– output driver. The host processor can communicate via I^2C to the charger, and modify this register to emulate the relevant adapter interface. This register also includes the bits to enable detection of HVDCP and MaxCharge adapters during the input current detection.

Table 1. Relevant D+/D– Bits in REG01

Bit	Field	Type	Reset	Description
7	DP_DAC[2]	R/W	by REG_RST	D+ Pin Output Driver 000 – HiZ mode (Default) 001 – 0 V (V_{0P0_VSRC}) 010 – 0.6 V (V_{0P6_VSRC}) 011 – 1.2 V (V_{1P2_VSRC}) 100 – 2.0 V (V_{2P0_VSRC}) 101 – 2.7 V (V_{2P7_VSRC}) 110 – 3.3 V (V_{3P3_VSRC}) 111 – Reserved Register bits are reset to default values when input source is plugged in and can be changed after D+/D– detection is completed
6	DP_DAC[1]	R/W	by REG_RST	
5	DP_DAC[0]	R/W	by REG_RST	
4	DM_DAC[2]	R/W	by REG_RST	D– Pin Output Driver 000 – HiZ mode (Default) 001 – 0 V (V_{0P0_VSRC}) 010 – 0.6 V (V_{0P6_VSRC}) 011 – 1.2 V (V_{1P2_VSRC}) 100 – 2.0 V (V_{2P0_VSRC}) 101 – 2.7 V (V_{2P7_VSRC}) 110 – 3.3 V (V_{3P3_VSRC}) 111 – Reserved Register bits are reset to default values when input source is plugged in and can be changed after D+/D– detection is completed
3	DM_DAC[1]	R/W	by REG_RST	
2	DM_DAC[0]	R/W	by REG_RST	
1	EN_12V	R/W	by REG_RST	Enable 12-V detection for MaxCharge and HVDCP 0 – Disable 12-V detection (Default) 1 – Enable 12-V detection

3 Implementation Using an MSP430F5529 as the Host Processor

The following were used for this exercise:

- Host Processor: MSP430F5529 (Any microcontroller with at least one I^{2}C port works.)
- HVDCP adapter: Anker PowerPort+1 QC3.0 adapter: 3.6-V to 12-V output voltage
- Charger: bq25890H

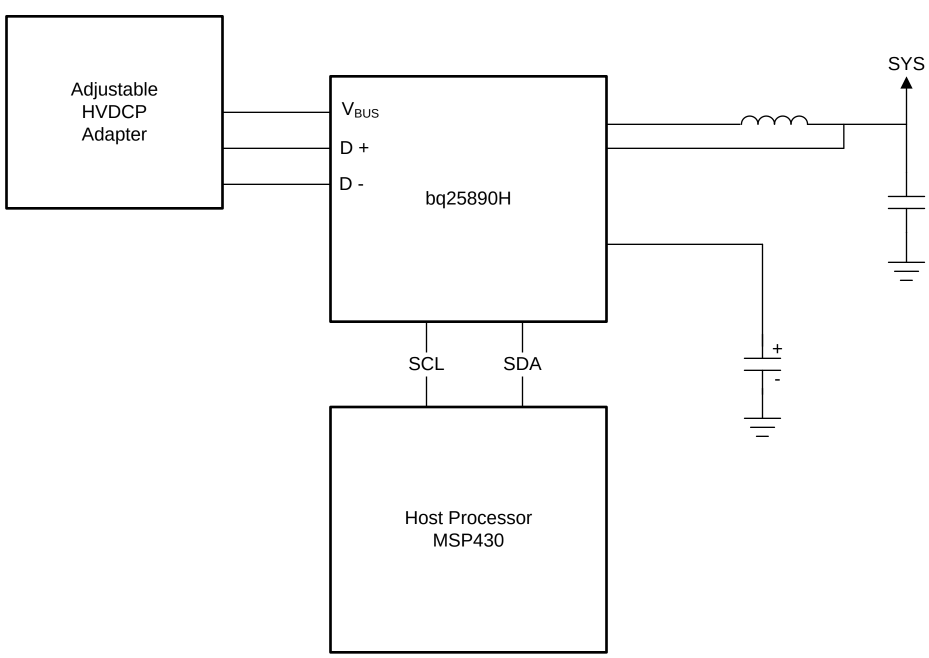

Figure 1. Connection Between Charger, Adapter, and Host

4 Software Control Loop

The bq25890H provides operating information based on its integrated control loops. The MSP430 uses this information to control the D+/D– lines through the charger to let the adapter know what voltage to provide. If a MaxCharge or HVDCP adapter is detected during charging, the host monitors the status of the INDPM loop. For a fixed charge current setting, the host instructs the adapter by means of the D+/D– output driver of the charger to decrease the voltage just before the device enters INDPM. This way, the adapter is providing the necessary power to the charger while operating with higher efficiency than a fixed output adapter. Refer to Figure 2 and Figure 3 for an overview of the handshaking.

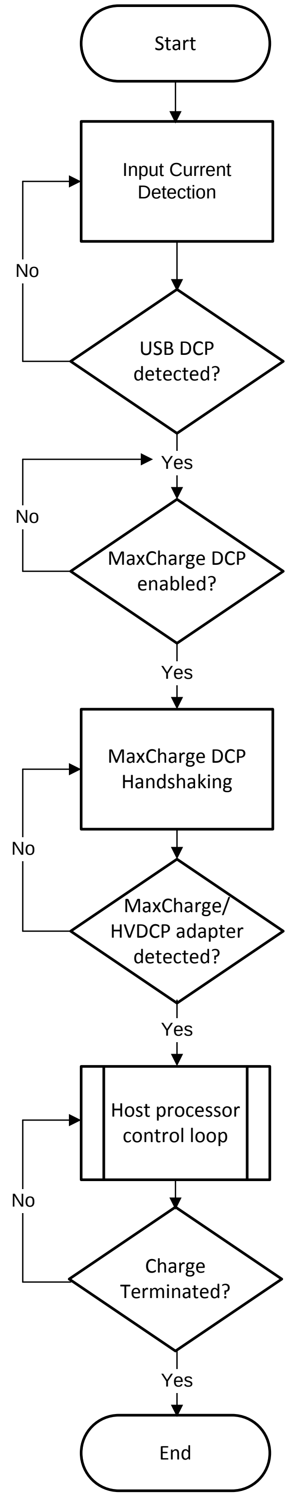

Figure 2. Main Control Loop

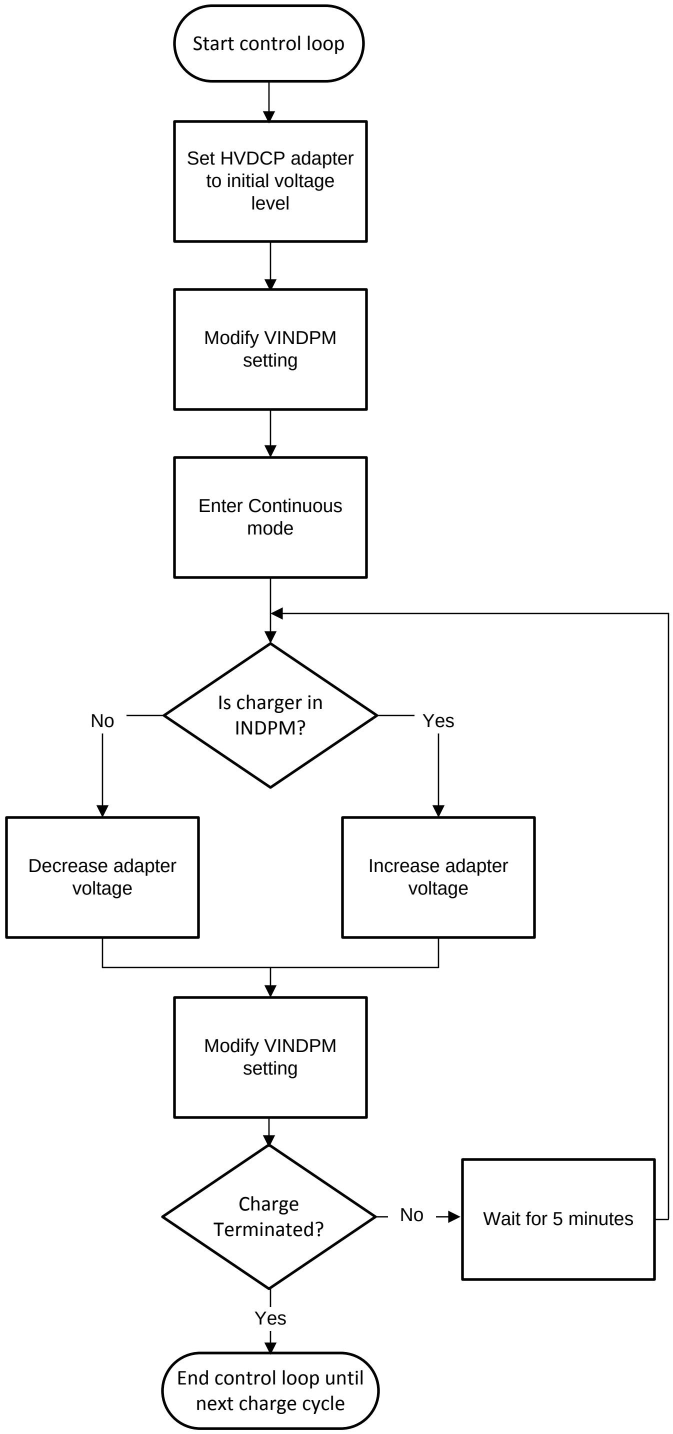

Figure 3. Handshaking Flowchart

5 Example of Controlling a High-Voltage Adjustable Adapter using the D+/D– Driver

For this exercise, assume the interfacing adapter has the following specifications:

- Voltage range: 5 V to 8 V
- Current: 1.5 A
- Adjustable voltage with 500-mV steps
- Interfaces via D+/D– lines

D+	D–	Mode Selected
0.6	1.2	Set output to 5 V
0.6	2.7	Set output to 8 V
0.6	0.6	Adjustable mode

Once in adjustable mode, to increase the voltage a step on the D+ from 0.6 V to 3.3 V with a duration of at least 2 ms forces the output to increase by 500 mV (ΔV). To decrease the voltage, the same applies but on the D– line.

Several functions can be implemented to modify Register 01 to control the D+ or D– lines. These functions can be tailored to work with multiple adjustable adapters:

- **SetDPlus():** sets the D+ line voltage to one of the presets
- **SetDMinus():** sets the D– line voltage to one of the presets
- **setAdapterVoltage():** instructs the adapter to set the output voltage
- **increaseVoltage():** instructs the adapter to increase the voltage by one step
- **decreaseVoltage():** instructs the adapter to decrease the voltage by one step

An example implementation follows showing how to use the voltage steps to increase the voltage to 6 V:

```
void increaseVoltage(){
        setAdapterVoltage(0.6, 0.6); // Enter adjustable mode

        setDPlus(3.3); //Modify D+
        wait_ms(2);   // Duration of step
        setDPlus(0.6); //Revert to original level
}

//Increase to 6V

setAdapterVoltage(0.6, 1.2); // Set adapter to 5V

int i = 0;

for(; i <= 1; i++){
        increaseVoltage(); //2 steps, 500mV each
}
```

Figure 4 represents an example of how this behavior looks after implementing the increase or decrease functions, where Dx_y represents the specific D+ or D– thresholds based on the protocol used and ∆V, the resolution of the output voltage steps.

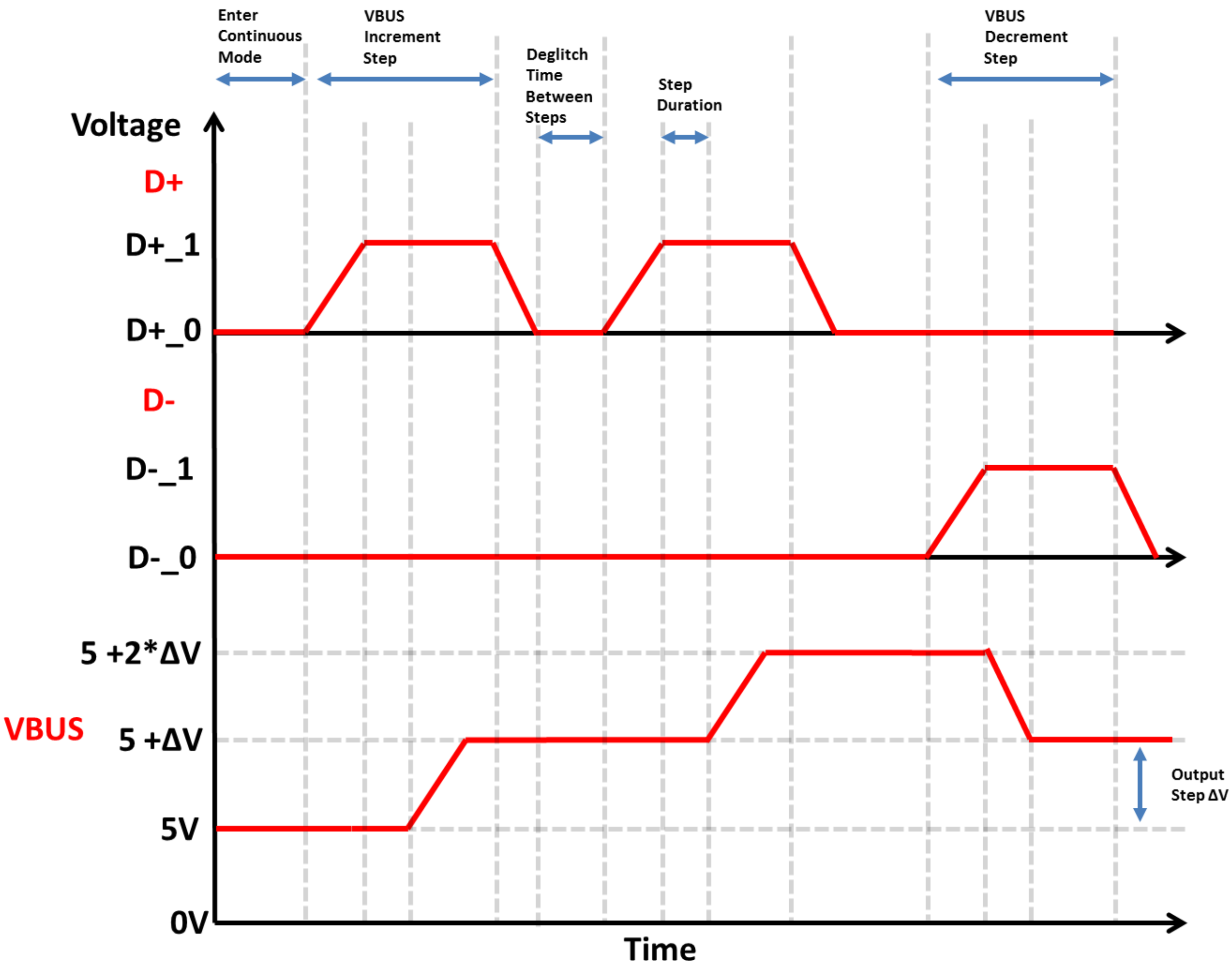

Figure 4. Adjustable Adapter Output Steps

6 Efficiency on the bq25890H With an Adjustable Adapter

Figure 5 presents efficiency values for common charge current thresholds using an adjustable HVDCP adapter and the bq25890H. This showcases how the software control loop discussed previously fine-tuned the charging efficiency using an adjustable voltage through the D+/D– interface. In this example, we can see that the efficiency peaked around VBUS = 6.4 V.

Further robustness can be added to the software of the application to account for varying charger currents and as the battery voltage changes during operation.

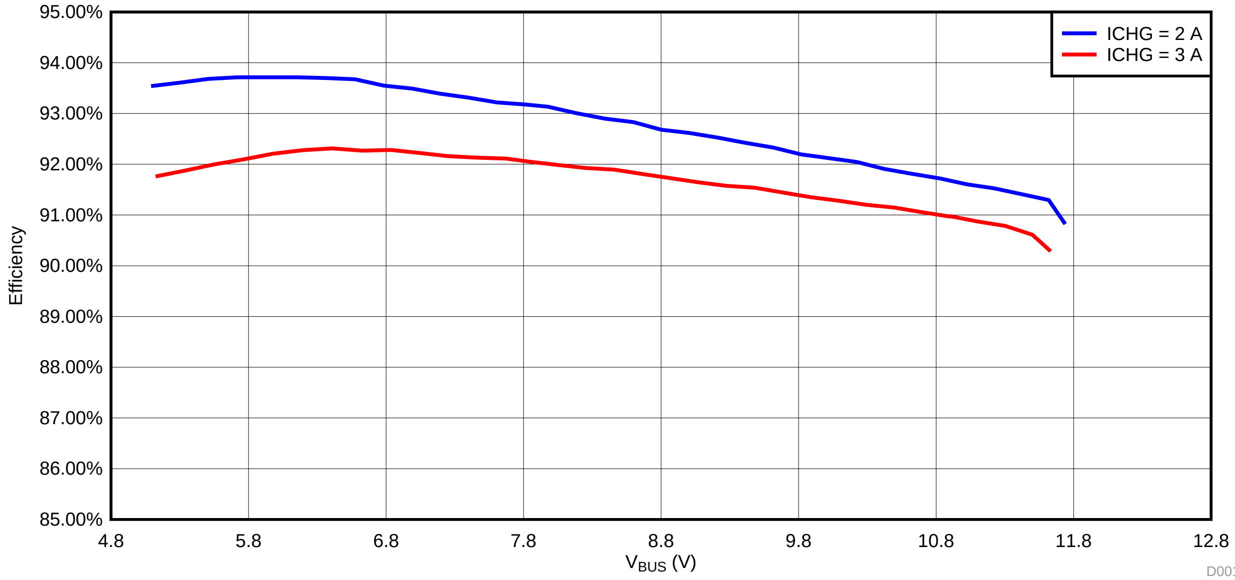

Figure 5. bq25890H Charge Efficiency Using Anker QC3.0 Adapter, V_{BAT} = 3.8 V, Inductor = 1 µH / 10 mΩ

7 Conclusion

The bq25890H provides a flexible, easy way to fine-tune charging efficiency by means of interfacing with a high-voltage adjustable adapter using the integrated D+/D– driver. It allows the design to be simple or robust to meet efficiency requirements by leveraging the *Power-Path* functionality of the charger.

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