Power MOSFET Gate Driver Bias Optimization

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Gate drive voltage plays a significant role in the power dissipation of switch-mode converters and is one of the primary considerations when designing for system optimum performance, efficiency, and speed of the circuit. Lower gate drive voltages are especially impactful on light load efficiency, where most efficiency gains can be made due to the high proportion of time systems spend in idle operation. Despite the rise of wide-bandgap semiconductors such as silicon carbide, silicon MOSFETs still occupy a majority of the industry. TI offers a variety of cost-optimized gate drivers designed to drive MOSFETs up to 18V.

Before discussing the impact of drive voltage, sources of loss and where they occur must be understood. This tech note focuses on the losses present in the control MOSFET of a non-synchronous buck converter, which can be broadly separated into three primary sources: conduction loss, switching loss, and gate charge loss.

Conduction losses are measured as the I^2R losses due to conduction of current through the channel $R_{DS(on)}$ of the MOSFET. Conduction losses can be calculated using the following formula:

$$P_C = I_{OUT}^2 \times R_{DS(on)} \times D \quad (1)$$

- P_C is conduction losses
- I_{OUT} is output current
- $R_{DS(on)}$ is the MOSFET channel resistance
- D is the duty cycle

Switching loss is the loss that occurs during the hard switching transition between the open and closed states, and overlap of drain current and drain to source voltage waveforms. The triangle formed by the overlap of drain current and drain to source voltage can be approximated as

$$P_{SW}=½ \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times F_{SW} \quad (2)$$

- P_{SW} is switching losses
- V_{IN} is input voltage
- I_{OUT} is output current
- t_r and t_f are the MOSFET rise and fall time respectively
- F_{SW} is the switching frequency

Gate charge loss is the loss due to charging and discharging the equivalent gate capacitance each switching cycle. Gate charge loss can be expressed in the equation:

$$P_G = Q_G \times V_{GS} \times F_{SW} \quad (3)$$

- P_G is gate charge loss
- Q_G is the equivalent total gate charge
- V_{GS} is the gate charge voltage
- F_{SW} is the switching frequency

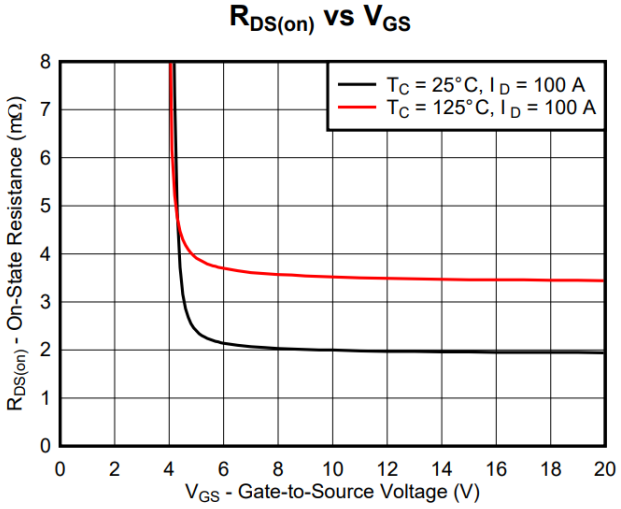

Figure 1. $R_{DS(on)}$ vs Gate Drive Voltage

The primary effect of higher gate drive voltage is a decrease in conduction losses that occurs as a result of lower $R_{DS(on)}$ resistance brought about by higher V_{GS}. This decrease in conduction loss is subject to diminishing returns, a relationship observable in the $R_{DS(on)}$ vs V_{GS} electrical characteristics curve of a MOSFET (Figure 1).

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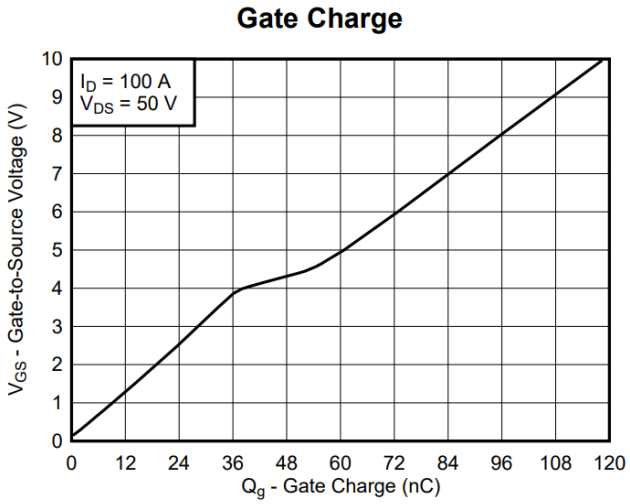

Figure 2. Gate Drive Voltage vs Gate Charge

The secondary effect of increased V_{GS} is increased gate charge losses. After driving through the Miller plateau, the relationship between V_{GS} and gate charge (Qg) is mostly linear (Figure 2). This increase in total charge leads to higher power dissipation as the gate is continuously charged and discharged.

Using Equation 1, conduction losses are proportional to $R_{DS(on)}$, duty cycle, and the square of the output current. This relationship means conduction loss scale far more with higher output power than $R_{DS(on)}$ and even less with V_{GS} due to the flattening of the curve at higher gate drive voltages in Figure 1. Gate charge losses are proportional to the equivalent total gate charge, V_{GS} and switching frequency. Since Q_G also scales linearly with V_{GS} after the Miller plateau, gate charge loss will scale quadratically with V_{GS}. A more in-depth exploration of switching loss is outside of the scope of this tech note and the approximation outlined above in Equation 3 will suffice for this example.

Figure 3 and Figure 4 utilize equations outlined above with a 5-V input voltage, the $R_{DS(on)}$ and Q_G characteristics, and the gate drive characteristics of the UCC21220/UCC21540/UCC5304. Figure 3 compares the different sources of power loss over gate drive voltage at 1-A output current.

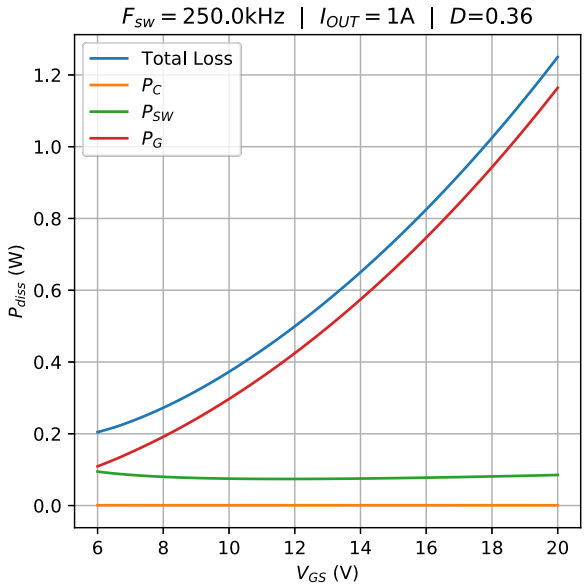

Figure 3. Light Load Power Dissipation

The data in Figure 3 highlights the issues higher gate drive voltages can present to power loss considerations. At lower currents and lighter loads, gate charge loss makes up the largest portion of the total loss while conduction loss remains minimal.

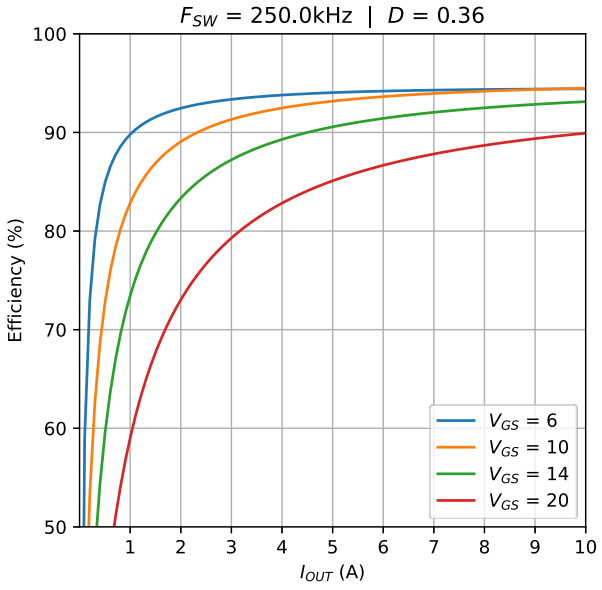

Figure 4. Output Efficiency over Load

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Figure 4 displays the efficiency curves for different gate drive voltages. While they begin to converge at higher loads, the efficiency differences at lower currents are dramatic.

Taking this example into account, designers should keep gate drive voltage in mind when designing their own systems. The higher a MOSFET's equivalent gate charge and the lower its $R_{DS(on)}$ the more gate charge losses dominate total losses at light loads. By understanding how gated drive voltage impacts both of these MOSFET parameters, designers can more readily leverage the light load efficiency gains of lower gate drive voltage and more easily meet their system efficiency goals.

Table 1. Adjacent Tech Notes

Optimized MOSFET characteristics by adjusting gate drive amplitude
MOSFET power losses and how they affect power-supply efficiency

References

CSD19536KTT, MOSFET used in example

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