TEXAS INSTRUMENTS

TPS79733EVM

LDO Regulator Evaluation Module

User's Guide

May 2003 — Power Management Products Low Power

SLVU064A

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DYNAMIC WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 1.8 – 3.3 V and the output current range of 0 mA to10 mA.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85°C. The EVM is designed to operate properly with certain components above 85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

About This Manual

This user's guide describes the TPS79733EVM LDO regulator evaluation module. Each EVM contains an SLVP199 test board with a TPS79733DCK regulator as well as supporting passive components. The EVM provides a convenient method of evaluating the performance of the TPS797xx linear regulator family as well as other SC–70/SOT–323 packaged linear regulators with the similar pin-out.

How to Use This Manual

- Chapter 1—Introduction
- Chapter 2—EVM Test Setup
- Chapter 3—Test Results

Related Documentation From Texas Instruments

- TPS797xx data sheet (literature number SLVS332)

Contents

Figures

Tables

Chapter 1

Introduction

This user's guide describes the TPS79733EVM LDO regulator evaluation module. Each EVM package contains an SLVP199 test board with a TPS79733DCK low dropout linear regulator as well as supporting passive components.

Topic **Page**

1.1 TPS797xx Family of LDO Regulators

The TPS797xx family of LDO regulators consists of small SOT–323/PICO packaged regulators capable of delivering 10 mA of output current. Features of the part include:

- 10-mA low dropout regulator
- Ultralow 1.2-μA quiescent current at 10 mA
- 5-pin SC–70/SOT–323 (DCK) package
- Integrated power good output
- Stable with any capacitor (>0.47-μF)
- Dropout voltage (typically 105 mV at 10 mA)
- Over current limitation
- –40°C to 85°C operating junction temperature range

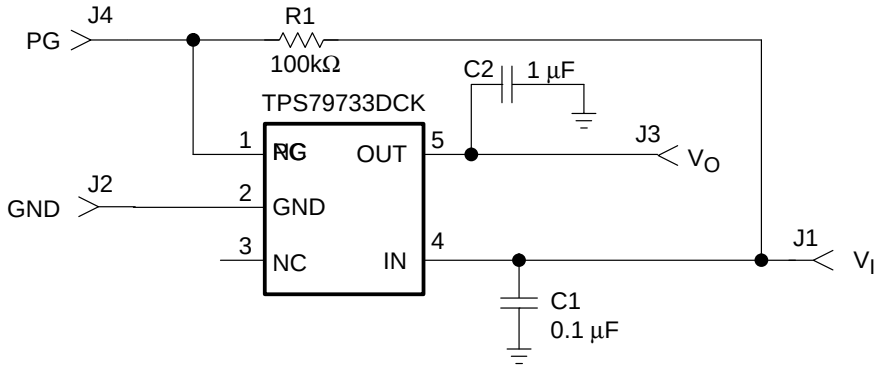
1.2 EVM Design Strategy

The purpose of this EVM is to facilitate evaluation of the TPS797xx family of LDO regulators. Each EVM package contains an SLVP199 test board with a TPS79733DCK low dropout linear regulator as well as supporting passive components. Also, the board's small size and side clips facilitate attaching it to other PCB's as a power module.

1.3 Schematic

Figure 1–1 shows the SLVP199 PCB schematic diagram, which is used in the TPS79733EVM.

Figure 1–1. TPS79733EVM Schematic Diagram



1.4 Bill of Materials

Table 1–1 lists materials required for the TPS79733 EVMs.

Table 1–1. TPS79733EVM Bill of Materials

Qty	Ref Des	Description	Size	MFR	Part Number
1	C1	Capacitor, ceramic, 0.1-µF, 6.3 V, X5R, 10%	603	Murata	GRM188R71E104KA01
1	C2	Capacitor, ceramic, 1.0-µF, 25 V, X7R, 10%	603	Murata	GRM188R60J105KA01
4	J1 thru J4	Clip, surface-mount, 0.040 board, 0.090 standoff	0.100”	NAS Interplex	CA26DA-D36W-0FC
1	R2	Resistor, chip, 100.0 kΩ, 1/16 W, 1%	603	Std	Std
1	U1	IC, ultralow noise, 10 mA, LDO regulator	SOP–5 (DCK)	TI	TPS79733DCK

1.5 Board Layout

Figures 1–2 and 1-3 show the board layout of the SLVP199 PCB used for the TPS79733EVM.

Figure 1–2. Top Layer

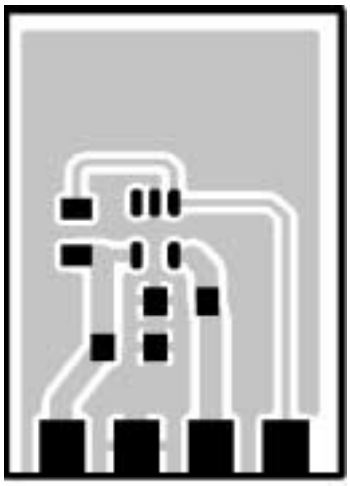


Figure 1–3. Bottom Layer

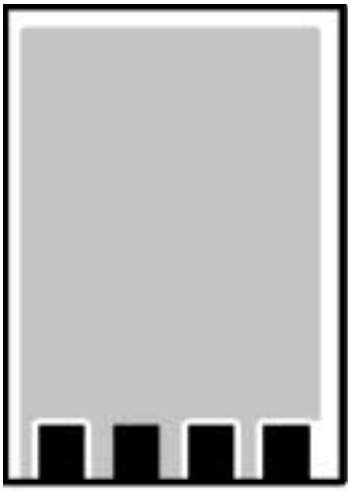
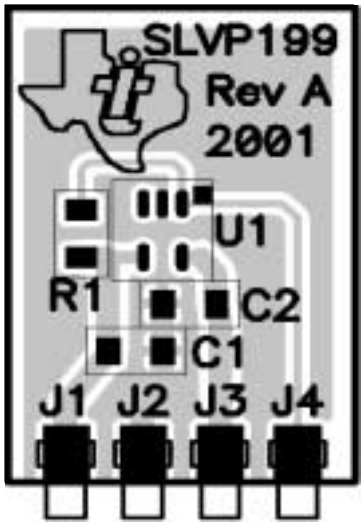


Figure 1–4. Assembly Drawing—Top

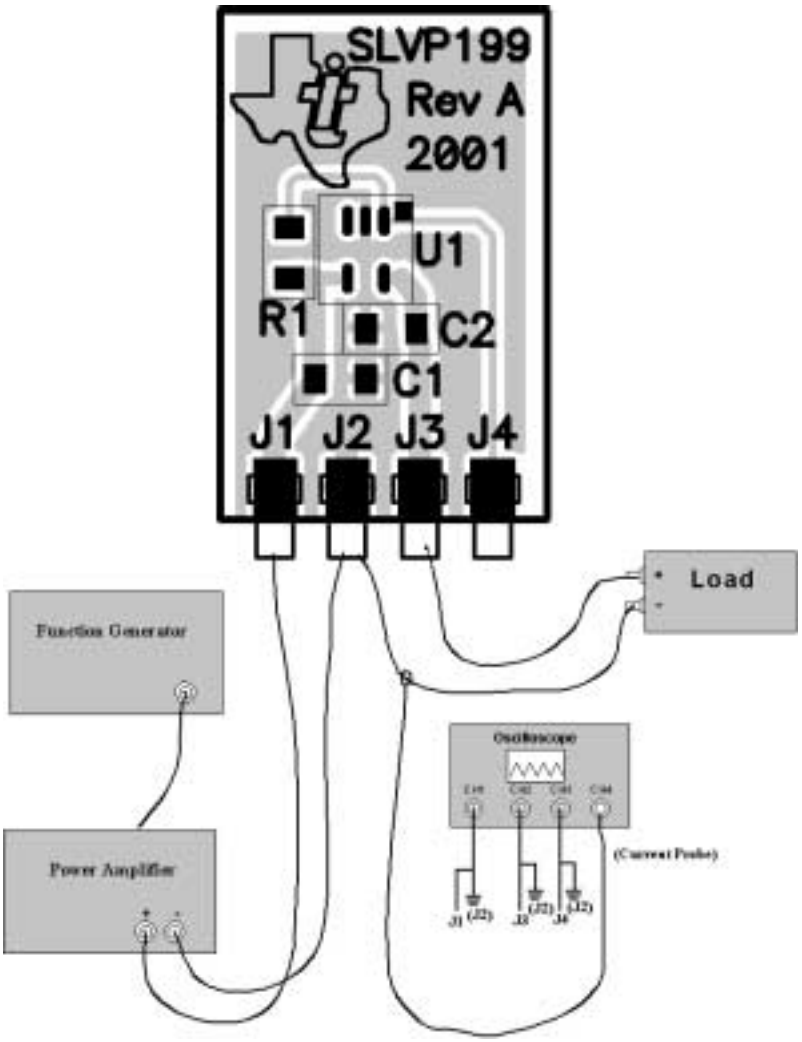


Chapter 2

EVM Test Setup

This chapter provides recommended test equipment and procedure for performing evaluations using the TPS79733EVM. Figure 2–1 shows the test setup.

Figure 2–1. Recommended TPS79733EVM Test Setup



The settings for the test equipment shown in Figure 2–1 are described below:

- Function generator is set to output a 5.5-V square wave with rise and fall times of 2 ms, top width of 5 ms, and a period of 1 ms.
- Power amplifier is set to a gain of 1 dB and a minimum slew rate of 2500 V/μs.
- Power supply capable of ±10-V swing and a 0.5-A current limit to power the power amplifier.
- A four-channel oscilloscope with channel one's voltage probe connected to J1 (IN), channel two's voltage probe connected to J3 (OUT), and channel three's voltage probe connected to J4 (PG). Connect channel four's current probe around the output load resistance. Set the scope to trigger off of channel one so that one full waveform is displayed on the screen.
- A 330-Ω resistance for 10-mA of output current (or 10-mA electronic load) connected between J3 (OUT) and J2 (GND).

After powering on the amplifier, the input voltage, output voltage, and output current is displayed.

Chapter 3

Test Results

This chapter gives laboratory test results of the TPS79733EVM obtained for the recommended test procedures in Chapter 2.

Figure 3–1 shows the input voltage ramp from 0 to 5.5 V (CH1), the 3.3-V regulated output voltage (CH2), the PG signal (CH3), and 10-mA output current (CH4). The scale on CH4 is 10 mA/div.

Figure 3–1. Input Voltage Ramp