Application Note

TDP2004 Schematic Checklist

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ABSTRACT

This schematic checklist provides a brief explanation of each TDP2004 device pin, and the recommended configuration of TDP2004 device pins for default operation. The TDP2004 is a DisplayPort™ (DP) linear redriver. The device complies with the VESA DisplayPort standard Version 1.4, 2.0, and 2.1; and supports a 1-4 lane Main Link interface signaling up to UHBR20 (20Gbps per lane). Additionally, this device is position independent. The TDP2004 can be placed inside source, cable, or sink, effectively providing a *negative loss* component to the overall link budget. The TDP2004 has the ability to be configured via GPIO, I2C, or EEPROM.

This document is intended to aid design at the system level for general applications, but must not be the only resource used. In addition to this list, use the information in the *TDP2004 Four-Channel 20Gbps DisplayPort 2.1 Linear Redriver*, *TDP2004 Evaluation Module*, and associated documents to gain a full understanding of device functionality.

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Trademarks

1 Introduction

This document includes the functionality, provides a recommendation, and provide additional considerations for each pin of the TDP2004. This data is encapsulated in Table 2-1.

2 TDP2004 Schematic Checklist

Table 2-1. TDP2004 Schematic Checklist

PIN NAME	PIN NUMBERS	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATIONS
Main Link Input Pins				
RX[0:3] P/N	30, 29, 33, 32, 37, 36, 40, 39	DisplayPort main link differential input	AC-coupled connection from GPU to the TDP2004	In the case of the DP connector connected to the TDP2004 input, the AC-coupling cap can already be populated on the GPU side. If so, then the TDP2004 input can be DC-coupled. If the TDP2004 input is still AC-coupled, please make sure the total capacitance does not violate the DP specification.
Main Link Output Pins				
TX[0:3] P/N	19, 20, 16, 17, 12, 13, 9, 10	DisplayPort main link differential output	75nF to 200nF AC-coupled connection from the TDP2004 to the sink or the connector	
Control Pins				
MODE	25	Selects between configuration modes: L0: Pin-strap mode L1: SMbus/ I2C primary mode L2: SMBus/ I2C secondary mode	Tie 1kΩ to ground for pin-strap mode Tie 8.25kΩ to ground for EEPROM control Tie 24.9kΩ to ground for external I2C control	
DONEn	7	Indicates completion of valid EEPROM register load operation.	Only required for SMBus/ I2C primary mode. If not using this mode leave floating	If using SMBus/ I2C Primary mode, external 4.7kΩ pull-up required for operation.
READ_EN_N	33	This pin controls the initiation of the SMBus/ I2C primary mode EEPROM read operation	Only required for SMBus/ I2C primary mode. If not using this mode leave floating	If using SMBus/ I2C Primary mode: After power up, when the pin is low, the device initiates the SMBus / I2C Primary mode EEPROM read function.
EQ0/ ADDR0	23	In pin-strap mode this pin selects the linear equalization (CTLE) for channels 0-3. This pin is sampled at power-up only. In SMBus/ I2C secondary mode, this pin sets the I2C secondary address. This pin is sampled at power-up only.	Tie 1kΩ to ground for pin-strap mode	See table 6-4 in data sheet for SMBus/ I2C secondary mode

Table 2-1. TDP2004 Schematic Checklist (continued)

PIN NAME	PIN NUMBERS	PIN DESCRIPTION	RECOMMENDATION	ADDITIONAL PIN CONSIDERATIONS
EQ1/ ADDR1	24	In pin-strap mode this pin selects the linear equalization (CTLE) for channels 0-3. This pin is sampled at power-up only. In SMBus/ I2C secondary mode, this pin sets the I2C secondary address. This pin is sampled at power-up only.	Tie 24.9kΩ to ground for pin-strap mode	See table 6-4 in data sheet for SMBus/ I2C secondary mode
GAIN/ SDA	27	In pin-strap mode this pin selects the flat gain (AC & DC) from the input to the output. This pin is sampled at power-up only. In SMBus/ I2C mode this pin serves as serial data and an external pull-up is required	Leave floating in pin-strap mode	External 4.7kΩ pull up resistor required for SMBus/ I2C mode
TEST/ SCL	26	In pin-strap mode this is a TI internal test In SMBus/ I2C mode this pin serves as serial clock	This needs to be pulled down via a 10kΩ resistor in pin-strap mode	External 4.7kΩ pull up resistor required for SMBus/ I2C mode
PD	6	2-level logic controlling the operating state of the redriver. Active in all device control modes. The pin has internal 1MΩ weak pull-down resistor.	Leave floating	
VCC	14, 15, 34, 35	Power supply pins. VCC = 3.3V ±10%	The VCC pins on this device must be connected through a low-resistance path to the board VCC plane	Install a decoupling capacitor to GND near each VCC pin
GND	1, 8, 11, 18, 21, 28, 31, 38, EP	Ground reference for the device	The exposed pad must be connected to one or more ground planes	

3 Summary

Please follow the guidelines found in this schematic checklist when designing the TDP2004, but also consider the surrounding system as well. Additionally, when designing the TDP2004 in a system is very important to consider functional flexibility. Having the option for pin-strap and I2C mode when implementing the device allows for much easier debug and better control of the configuration and status of the TDP2004.

4 References

- Texas Instruments, *TDP2004 Four-Channel 20Gbps DisplayPort 2.1 Linear Redriver*, data sheet.
- Texas Instruments, *TDP2004 Evaluation Module*, user's guide.

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