User's Guide
SNVU596–October 2018

LP8752x-Q1 Configuration Guide

This configuration guide is designed to help one understand how to use a micro-controller unit (MCU) to configure an LP8752x-Q1 PMIC. Instead of requiring a new one time programmable configuration (OTP) for each design, a specific LP8752x-Q1 variants described in this configuration guide can be configured at startup through I^2C bus to meet design requirements.

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1 Introduction

The LP8752x-Q1 contains four step-down DC/DC converter cores, which are configured as 4-phase single output, 3-phase and single phase outputs, 1 dual phase and 2 single phase outputs, 4 single phase outputs or two dual phase outputs. The device is controlled by an I^2C-compatible serial interface and by enable signals. Typically the settings such as output voltages, startup/shutdown sequences etc. for the LP8752x-Q1 PMIC are programmed during IC manufacturing by a one time programmable memory (OTP). However, with an MCU this device can also be configured after each start up to fit different design requirements. Default values for the configuration registers (volatile memory) are loaded from the OTP during device power-up, and through I^2C bus the registers can be updated to desired values.

This guide explains how to set up an LP8752x-Q1 PMIC to be configured at start up so that it can be used in different designs, without the need for a new OTP. Specific OTP versions described in this document have been designed to allow the PMIC to be easily configured at each power-up. For device specifications and detailed functionality, please refer to the device datasheet.

2 Setup

There are a few important connections to ensure the LP8752x-Q1 is configured correctly, each of which are described in this section. A good example of how to connect an MCU to the LP8752x-Q1 PMIC is shown in .

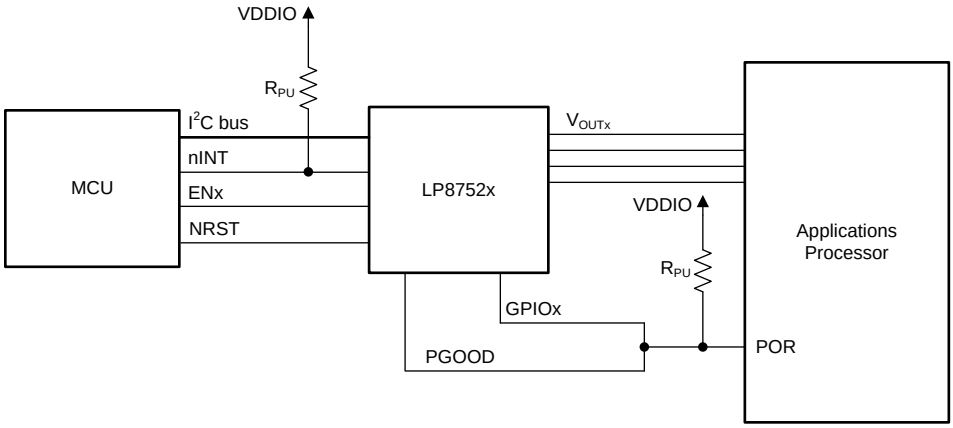

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Figure 1. Typical MCU Connection to LP8752x-Q1 for Start-Up Configuration

2.1 SCL/SDA Pins

The SCL and SDA lines (pins 5 & 6, respectively) are used to communicate between the MCU and the LP8752x-Q1 PMIC using an I^2C compatible Interface. The I^2C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the serial data line (SDA), and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock SCL. The SCL and SDA lines must each have a pullup resistor placed on the line and remain HIGH even when the bus is idle. The LP8752x-Q1 supports standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz), and high-speed mode (3.4 MHz). For all I^2C protocol details refer to the device datasheet.

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2.2 NRST Pin

The NRST pin (pin 20) is used to reset the device logic/enable device internal logic and IO interface. When the NRST voltage is below threshold level all power switches, references, controls, and bias circuitry of the LP8752x-Q1 device are turned off. When NRST is set to high level (and VANA is above UVLO level) this initiates power-on-reset (POR), OTP reading and enables the system I/O interface. The I^2C host must allow at least 1.2 ms before writing or reading data to the LP8752x-Q1. Device enters STANDBY-mode after internal startup sequence. The host can change the default register setting by I^2C if needed. The regulator(s) can be enabled/disabled by ENx pin(s) or by I^2C interface.

2.3 ENx (GPIOx) Pins

Enable pins EN1 (GPIO1), EN2 (GPIO2), EN3 (GPIO3) (pins 7, 15, 2) are I^2C configurable GPIO pins. The direction, function, and output type (open-drain or push-pull) are programmable for the GPIOs. When configured as EN pin, they can be used to start the buck converter startup sequence based on programmed timing. Shutdown times can be programmed as well. It is recommended that the ENx pins be driven low to until the device is configured to the desired settings. Drive these pins low to disable and high to enable when programmed as enable signal.

2.4 nINT

The nINT pin (pin 19) is an open-drain, active low output from the LP8752x-Q1 PMIC, and should be connected to a pullup resistor. In the default OTP an interrupt is generated on this pin whenever the RESET_REG_INT bit is set high. The RESET_REG_INT bit is set high when either the VANA supply voltage has decreased below the undervoltage threshold level or the host has requested a reset using the SW_RESET bit in the RESET register or device is reset by NRST. By monitoring the nINT pin, the MCU will know when the PMIC registers are reset to the values determined by the OTP, and can take the necessary actions to ensure that the PMIC is configured as needed.

After a power-on reset the LP8752x-Q1 PMIC requires a delay of 1.2ms before there can be any communication through the I^2C interface. This required delay can be ensured by monitoring the nINT pin. After a power-on reset the nINT pin is driven high while the registers are reset and the OTP is read to set the registers to their initial values. After 1.2ms the nINT pin is driven low, signaling that the registers have been reset and can be configured to fit the design requirements.

NOTE: To monitor the nINT pin correctly, the MCU must clear all interrupts before enabling all of the outputs on the LP8752x-Q1 PMIC. Write a 1 to the RESET_REG bit in the INT_TOP2 register to clear this interrupt. If all interrupts are not cleared before enabling the LP8752x-Q1 PMIC ouputs, then there will be no change on the nINT pin when an interrupt is generated and the MCU will not be able to detect a register reset.

3 Configuration

This section describes the default OTP settings, and how to configure these settings to meet design requirements.

3.1 Configuration Sequence

Using the setup described in Section 2 allows the MCU to easily configure the LP8752x-Q1 PMIC after a power-on reset, or after any event causing a register reset. To ensure this is done correctly follow the sequence described in this section. The following list shows the actions to take in order to ensure the LP8752x-Q1 PMIC is configured correctly. These actions should be taken after a power-on reset or a register reset.

1. Power on PMIC. (V_{VANA} > $VANA_{UVLO}$)
2. Set NRST high
3. Wait for nINT line to be set low. (Check RESET_REG bit, and set ENx pin low if necessary)
4. Set new configuration using I^2C communication in recommended order. See Section 3.3
    1. Voltage settings

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2. Regulator settings
3. GPIO settings
4. Clock sync functions
5. PGOOD settings
6. Interrupt settings
7. Startup / shutdown settings
8. Set ENx pin control bits
9. Set EN_BUCKx bits

5. Clear Interrupts.
6. Set ENx pin high to startup sequence.

Upon a power-on reset, waiting for the nINT line to be set low ensures that the PMIC is ready for I^2C communication. Waiting for the nINT line to be set low at any other time allows the PMIC to know when a register reset has occurred. The timing diagrams in Figure 2 and Figure 3 show how to configure the LP8752x-Q1 PMIC after a power-on reset or register reset has occurred. Once all of the I^2C writes are finished the interrupts should be cleared and the PMIC enabled by the MCU. The MCU can do this by writing a 1 to the RESET_REG bit to clear the interrupt and by pulling the ENx pin high to turn on the PMIC outputs.

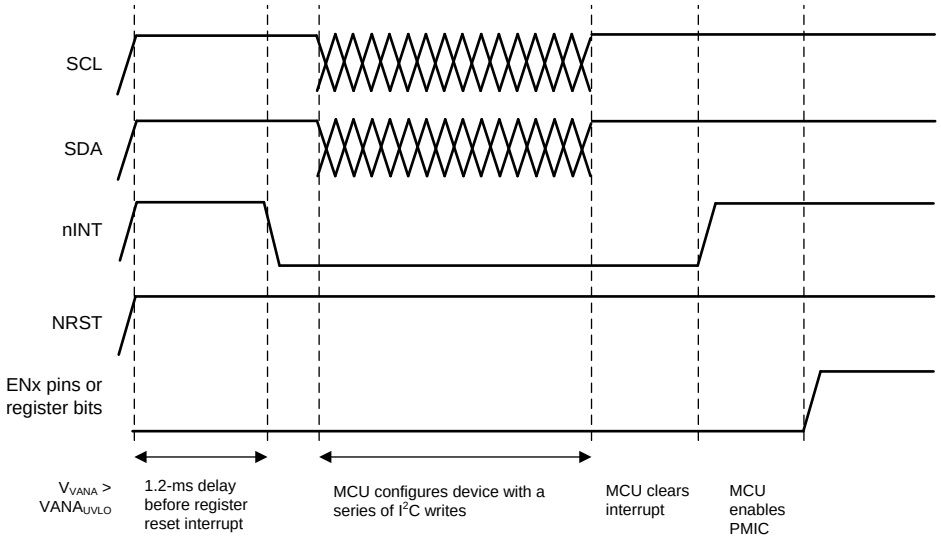

Figure 2. Configuration Sequence During Startup

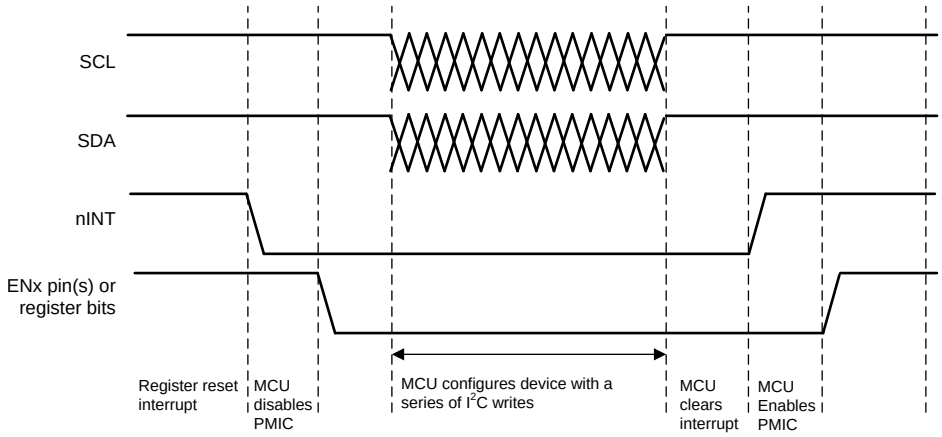

Figure 3. Configuration Sequence During Reset

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3.2 Default OTP Configurations

All LP8752x-Q1 PMIC resource settings are stored in the form of volatile registers. These settings define, for example, buck output voltages, GPIO functionality, and power-up and power-down sequences. The OTP by default has no sequencing so that the user can configure the desired sequence. Refer to the datasheet for a full list of the setting registers. Different OTP is needed for each 5 possible phase configuration. Phase configuration is not I^2C configurable.

Each device has predefined values stored in OTP which control the default configuration of the device. The tables in this section list the OTP-programmed values for each device.

Table 1 shows device settings for BUCK0, BUCK1, BUCK2, BUCK3. Maximum allowed slew-rate for BUCKx depends on the output capacitance. Refer to the device data sheets for output capacitance boundary conditions.

Table 1. BUCK0, BUCK1, BUCK2, BUCK3 OTP Settings

	Description	Bit Name	LP8752x-Q1	Configurable
General settings	Buck phase configuration (e.g. four single phase denoted as 1+1+1+1, four phase single output denoted as 4 ph). For multiphase configuration master buck defines the output voltage, startup/shutdown times etc. See datasheet for more details.		LP875210 - 4 ph LP875220 - 3+1 LP875230 - 2+1+1 LP875240 - 1+1+1+1 LP875250 - 2+2	No
	Switching frequency		2 MHz	No
	Spread spectrum	EN_SPREAD_SPEC	No	Yes
	Startup and shutdown delay range, 0...4.8ms / 0... 10ms / 0...15ms / 0...30ms	DOUBLE_DELAY, HALF_DELAY	0...15 ms	Yes
BUCK0	Output voltage	BUCK0_VSET	600 mV	Yes
	Enable, ENx-pin or I^2C register	EN_PIN_CTRL0	I^2C	Yes
	Control for BUCK0	EN_BUCK0	Low	Yes
	Force PWM mode or auto mode	BUCK0_FPWM	auto	Yes
	Force multiphase mode or auto mode	BUCK0_FPWM_MP	auto	Yes
	Peak current limit	-	LP875210 3.5A LP875220 3.5A LP875230 3.5A LP875240 5A LP875250 3.5A	No
	Slew rate	SLEW_RATE0	3.8 mV/µs	Yes
	Startup Delay	BUCK0_STARTUP_DELAY	0 ms	Yes
	Shutdown Delay	BUCK0_SHUTDOWN_DELAY	0 ms	Yes
BUCK1	Output voltage	BUCK1_VSET	600 mV	Yes
	Enable, EN-pin or I^2C register	EN_PIN_CTRL1	I^2C	Yes
	Control for BUCK1	EN_BUCK1	Low	Yes
	Force PWM mode or auto mode	BUCK1_FPWM	auto	Yes
	Peak current limit	-	LP875210 3.5A LP875220 3.5A LP875230 3.5A LP875240 2A LP875250 3.5A	No
	Slew rate	SLEW_RATE1	3.8 mV/µs	Yes
	Startup Delay	BUCK1_STARTUP_DELAY	0 ms	Yes
	Shutdown Delay	BUCK1_SHUTDOWN_DELAY	0 ms	Yes

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Table 1. BUCK0, BUCK1, BUCK2, BUCK3 OTP Settings (continued)

	Description	Bit Name	LP8752x-Q1	Configurable
BUCK2	Output voltage	BUCK2_VSET	600 mV	Yes
	Enable, ENx-pin or I^2C register	EN_PIN_CTRL2	I^2C	Yes
	Control for BUCK0	EN_BUCK2	Low	Yes
	Force PWM mode or auto mode	BUCK2_FPWM	auto	Yes
	Force multiphase mode or auto mode	BUCK2_FPWM_MP	auto	Yes
	Peak current limit	-	LP875210 3.5A LP875220 3.5A LP875230 3.5A LP875240 4A LP875250 3.5A	No
	Slew rate	SLEW_RATE2	3.8 mV/µs	Yes
	Startup Delay	BUCK2_STARTUP_DELAY	0 ms	Yes
	Shutdown Delay	BUCK2_SHUTDOWN_DELAY	0 ms	Yes
BUCK3	Output voltage	BUCK3_VSET	600 mV	Yes
	Enable, EN-pin or I^2C register	EN_PIN_CTRL3	I^2C	Yes
	Control for BUCK1	EN_BUCK3	Low	Yes
	Force PWM mode or auto mode	BUCK3_FPWM	auto	Yes
	Peak current limit	-	LP875210 3.5A LP875220 3.5A LP875230 3.5A LP875240 3A LP875250 3.5A	No
	Slew rate	SLEW_RATE3	3.8 mV/µs	Yes
	Startup Delay	BUCK3_STARTUP_DELAY	0 ms	Yes
	Shutdown Delay	BUCK3_SHUTDOWN_DELAY	0 ms	Yes

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Table 2 lists the device settings for GPIOs.

Table 2. EN, CLKIN and GPIO Pin Settings

	Description	Bit Name	LP8752x-Q1	Configurable
EN1 (GPIO1) pin	EN1 (GPIO1) pin pulldown resistor enable or disable	EN1_PD	Enabled	Yes
EN2 (GPIO2) pin	EN2 (GPIO2) pin pulldown resistor enable or disable	EN2_PD	Enabled	Yes
EN3 (GPIO3) pin	EN3 (GPIO3) pin pulldown resistor enable or disable	EN3_PD	Enabled	Yes
CLKIN pin	CLKIN pin pull-down resistor enable or disable	CLKIN_PD	Enabled	Yes
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	2 MHz	Yes
	Mode for the internal PLL. When PLL disabled, internal RC OSC is used	PLL_MODE[1:0]	Disabled	Yes
EN1 (GPIO) control	Enable or GPIO	GPIO1_SEL	EN	Yes
	Input or output in GPIO mode	GPIO1_DIR	Output	Yes
	Output type open drain or push-pull	GPIO1_OD	Open drain	Yes
	Default state of GPIO output	GPIO1_OUT	Low	Yes
EN2 (GPIO) control	Enable or GPIO	GPIO2_SEL	EN	Yes
	Input or output in GPIO mode	GPIO2_DIR	Output	Yes
	Output type open drain or push-pull	GPIO2_OD	Open drain	Yes
	Default state of GPIO output	GPIO2_OUT	Low	Yes
	Pin control of GPIO, EN2 or EN3	EN_PIN_CTRL_GPIO2, EN_PIN_SELECT_GPIO2	Disabled	Yes
	Startup Delay	GPIO2_ STARTUP_DELAY	0 ms	Yes
	Shutdown Delay	GPIO2_ SHUTDOWN_DELAY	0 ms	Yes
EN3 (GPIO) control	Enable or GPIO	GPIO3_SEL	EN	Yes
	Input or output in GPIO mode	GPIO3_DIR	Output	Yes
	Output type open drain or push-pull	GPIO3_OD	Open drain	Yes
	Default state of GPIO output	GPIO3_OUT	Low	Yes
	Pin control of GPIO, EN2 or EN3	EN_PIN_CTRL_GPIO3, EN_PIN_SELECT_GPIO3	Disabled	Yes
	Startup Delay	GPIO3_ STARTUP_ DELAY	0 ms	Yes
	Shutdown Delay	GPIO3_ SHUTDOWN_ DELAY	0 ms	Yes

Table 3 shows device settings for PGOOD.

Table 3. PGOOD OTP Settings

	Description	Bit Name	LP8752x-Q1	Configurable
Signals monitored by PGOOD	BUCKx output voltage / voltage and current (master bucks)	PGx_SEL	Voltage	Yes
PGOOD mode selections	PGOOD thresholds for BUCKx (Undervoltage / Window (undervoltage and overvoltage))	PGOOD_WINDOW	Window	Yes
	PGOOD valid debounce time	PGOOD_SET_DELAY	7 µs	Yes
	PGOOD signal mode (status / latched until fault source read)	EN_PGFLT_STAT	Status	Yes
	PGOOD output mode (push-pull or open drain)	PGOOD_OD	OD	Yes
	PGOOD polarity (active high / active low)	PGOOD_POL	Active high (power valid)	Yes

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Table 4 lists the device settings for thermal warning. Also refer to Table 6 for interrupt settings.

Table 4. Protections OTP Settings

	Description	Bit Name	LP8752x-Q1	Configurable
Protections	Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	137°C	Yes
	Input over-voltage protection		Enabled	No

Table 5 shows device settings for I^2C and OTP revision ID values.

Table 5. Device Identification and I^2C Settings

	Description	Bit Name	LP8752x-Q1	Configurable
I^2C slave ID (7-bit)		LP875210 - 4 ph LP875220 - 3+1 LP875230 - 2+1+1 LP875240 - 1+1+1+1 LP875250 - 2+2	0x68 0x69 0x70 0x71 0x72	No

Table 6 lists device settings for interrupts. When interrupt from an event is unmasked, an interrupt is generated to nINT pin.

Table 6. Interrupt Mask Settings

	Interrupt event	Bit Name	LP8752x-Q1	Configurable
General	Sync clock appears or disappears	SYNC_CLK_MASK	Masked	Yes
	Thermal warning	TDIE_WARN_MASK	Masked	Yes
	Load measurement ready	I_LOAD_READY_MASK	Masked	Yes
	Register reset	RESET_REG_MASK	Unmasked	Yes
BUCK0	Buck0 PGOOD has reached threshold level	BUCK0_PG_MASK	Masked	Yes
	Buck0 current limit triggered	BUCK0_ILIM_MASK	Masked	Yes
BUCK1	Buck1 PGOOD has reached threshold level	BUCK1_PG_MASK	Masked	Yes
	Buck1 current limit triggered	BUCK1_ILIM_MASK	Masked	Yes
BUCK2	Buck2 PGOOD has reached threshold level	BUCK2_PG_MASK	Masked	Yes
	Buck2 current limit triggered	BUCK2_ILIM_MASK	Masked	Yes
BUCK3	Buck3 PGOOD has reached threshold level	BUCK3_PG_MASK	Masked	Yes
	Buck3 current limit triggered	BUCK3_ILIM_MASK	Masked	Yes

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3.3 Recommended Order of Configuring Registers Through I²C

This section goes through the main settings that can be changed to fit a specific design, in the recommended order. Refer to the datasheet and Section 3.2 for all of these settings and their corresponding bits/registers.

3.3.1 Voltage Settings

By default all of the voltage settings for the bucks are set to their smallest values. These settings can be changed by writing to the fields listed below. Refer to the datasheet to see how the values of these registers correspond to different voltages. Depending on phase configuration only master buck voltage needs to be set.

- BUCK0_VSET field in BUCK0_VOUT register
- BUCK1_VSET field in BUCK1_VOUT register
- BUCK2_VSET field in BUCK2_VOUT register
- BUCK3_VSET field in BUCK3_VOUT register

3.3.2 Other Regulator Settings

Each buck has 2 CTRL registers that can be used to set slew rates as well as enable their output discharge resistors or set auto/forced PWM mode and auto/forced multiphase mode. Included in these registers is an EN_PIN_CTRLx, EN_BUCKx, and BUCKx_EN_PIN_SELECT[1:0] bits for each regulator. It is recommended to set the EN_PIN_CTRLx, EN_BUCKx, and BUCKx_EN_PIN_SELECT[1:0] bits last to avoid any regulators turning on before configuration is complete. These regulator setting fields are summarized in Figure 1. Refer to the datasheet for a full description of all registers and their settings.

Table 7. Regulator Control Settings Registers

Regulator	Register	Fields that should be configured	Fields that should not be configured until the PMIC is ready to be powered up (Section 3.3.8)
BUCK0	BUCK0_CTRL_1	EN_ROOF_FLOOR0, EN_RDIS0, BUCK0_FPWM, BUCK0_FPWM_MP	BUCK0_EN_PIN _CTRL, EN_BUCK0, BUCK_0_EN_PIN_SELECT[1:0]
	BUCK0_CTRL_2	SLEW_RATE0[1:0]	
BUCK1	BUCK1_CTRL_1	EN_ROOF_FLOOR1, EN_RDIS1, BUCK1_FPWM	BUCK1_EN_PIN _CTRL, EN_BUCK1, BUCK_1_EN_PIN_SELECT[1:0]
	BUCK1_CTRL_2	SLEW_RATE1[1:0]	
BUCK2	BUCK2_CTRL_1	EN_ROOF_FLOOR2, EN_RDIS2, BUCK2_FPWM, BUCK2_FPWM_MP	BUCK2_EN_PIN _CTRL, EN_BUCK2, BUCK_2_EN_PIN_SELECT[1:0]
	BUCK2_CTRL_2	SLEW_RATE2[1:0]	
BUCK3	BUCK3_CTRL_1	EN_ROOF_FLOOR3, EN_RDIS3, BUCK3_FPWM	BUCK3_EN_PIN _CTRL, EN_BUCK3, BUCK_3_EN_PIN_SELECT[1:0]
	BUCK3_CTRL_2	SLEW_RATE3[1:0]	

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3.3.3 GPO Settings

The LP8752x-Q1 device supports up to 3 GPIO signals. The GPIO signals are multiplexed with enable signals. The selection between enable and GPIO function is set with GPIOx_SEL bits in PIN_FUNCTION register. When the pin is selected for GPIO function, additional bits defines how the GPIO operates:

- GPIOx_DIR defines the direction of the GPIO, input or output (GPIO_CONFIG register)
- GPIOx_OD defines the type of the output when the GPIO is set to output, either push-pull with VANA level or open-drain (GPIO_CONFIG register)

When the GPIOx is defined as output, the logic level of the pin is set by GPIOx_OUT bit (in GPIO_OUT register). When the GPIOx is defined as input, the logic level of the pin can be read from GPIOx_IN bit (in GPIO_IN register). The control of the GPIOs configured to outputs can be included to start-up and shutdown sequences. The GPIO control for a sequence with ENx signal is selected by EN_PIN_CTRL_GPIOx and EN_PIN_SELECT_GPIOx bits (in PIN_FUNCTION register). The delays during start-up and shutdown are set by GPIOx_STARTUP_DELAY[3:0] and GPIOx_SHUTDOWN_DELAY[3:0] bits (in GPIOx_DELAY register) in the same way as control of the regulators. The GPIOx signals have a selectable pull-down resistor. The pull-down resistors are selected by ENx_PD bits (in CONFIG register). Refer to the datasheet for more information on each of the fields in the GPIO registers.

3.3.4 Clock Sync Functions

The LP8752x-Q1 device contains a CLKIN input to synchronize switching clock of the buck regulator with the external clock. Depending on the PLL_MODE[1:0] bits (in PLL_CTRL register) and the external clock availability, the external clock is selected and interrupt is generated. The interrupt can be masked with SYNC_CLK_MASK bit in TOP_MASK1 register. The nominal frequency of the external input clock is set by EXT_CLK_FREQ[4:0] bits (in PLL_CTRL register) and it can be from 1 MHz to 24 MHz with 1-MHz steps. The external clock must be inside accuracy limits (–30%/+10%) for valid clock detection. Refer to the datasheet for more information on this function.

3.3.5 PGOOD Settings

The PGOOD output can be used to monitor several signals and has multiple settings to configure as listed below.

- Monitoring of regulator output voltage (Individual regulators can be selected)
- Undervoltage only or undervoltage and overvoltage monitoring
- Monitoring output current
- Debounce time setting
- Push-pull or open drain output
- Gated or continuous operating mode
- Adjustable polarity

Refer to the datasheet for more information on the PGOOD signal functionality.

3.3.6 Interrupt Settings

The LP8752x-Q1 PMIC has many interrupt signals that can be used to indicate different events including regulator overcurrent events, regulator PGOOD events, regulator short-circuit events, and clock events. The registers containing all of these interrupts are listed as follows:

- INT_TOP1 register
- INT_TOP2 register
- INT_BUCK_0_1 register
- INT_BUCK_2_3 register

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These interrupts can all be masked or unmasked using the registers below. By default the OTPs defined specifically for I²C configuration has only RESET_REG_INT unmasked to allow the MCU to know when the PMIC registers are reset to the values determined by the OTP, so the MCU can take the necessary actions to ensure that the PMIC is configured as needed. Other interrupts can be unmasked as is needed. However, unmasking other interrupts will mean that when an interrupt is generated on the nINT line, the interrupt registers must be read to determine what caused the interrupt.

- TOP_MASK1 register
- TOP_MASK2 register
- BUCK_0_1_MASK register
- BUCK_2_3_MASK register

3.3.7 Startup and Shutdown Sequence

Each of the bucks and GPOs on the LP8752x-Q1 can be set to startup and shutdown in a specific sequence. To configure the desired sequence the STARTUP_DELAY and SHUTDOWN_DELAY fields for each output need to be set to a value between 0x0 and 0xF. The delay time that this value corresponds to depends on the DOUBLE_DELAY bit and the HALF_DELAY bit located in the CONFIG register. A value of 0 on both of these bits will allow a delay ranging from 0 ms to 15 ms with 1ms steps. Figure 4 shows an example of how these delays can be used to configure a startup and shutdown sequence, in this case with EN1 signal. Refer to the datasheet for a full description of all registers and their settings.

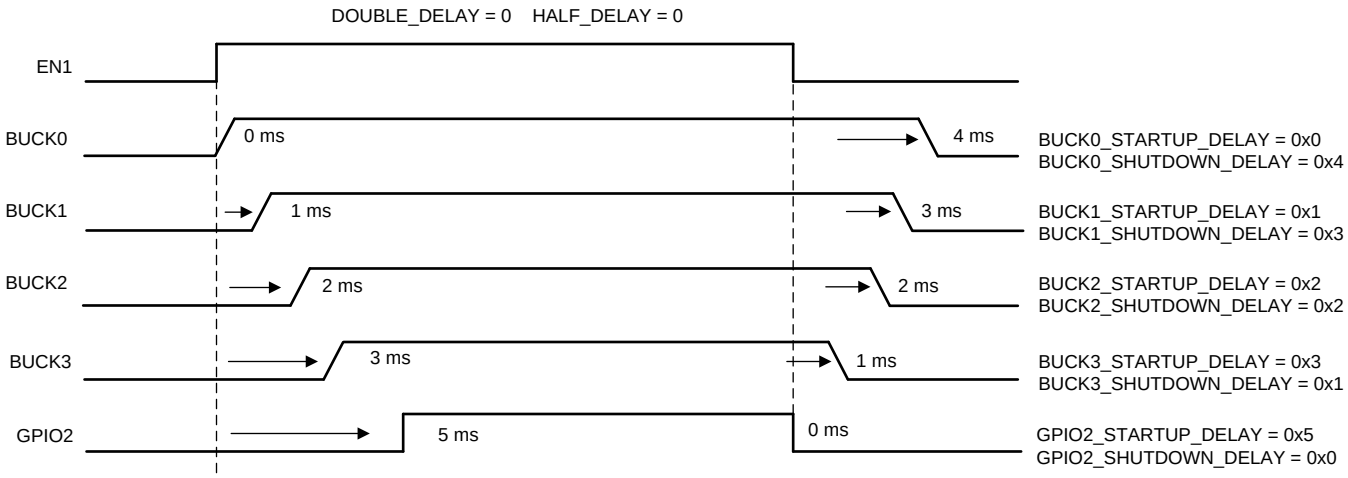

Figure 4. Startup and Shutdown Sequence Timing Diagram

3.3.8 Set ENx Pin Control Bits

Each output can be controlled by either I²C communication, or a combination of I²C communication and an ENx pin, as determined by each output's EN_PIN_CTRLx and BUCKx_EN_PIN_SELECT[1:0] bits. When controlled via I²C (EN_PIN_CTRLx = 0) the selected output is turned on using the corresponding EN_BUCKx bits. Note that the sequencing delay settings will not be effective in this case. When controlled using a combination of I²C an the ENx pin (EN_PIN_CTRLx = 1), both the ENx pin (set with BUCKx_EN_PIN_SELECT[1:0]) and the corresponding EN_BUCKx bit must be set high in order to turn on an output. By default the OTP has the EN_BUCKx bit and EN_PIN_CTRLx bit set low for each output. This prevents the ENx pin from accidentally setting an output high, and allows the user to choose which outputs to turn on with the ENx pin(s).

Once all of the other device settings have been set, the EN_PIN_CTRLx bit should be set high for each output that needs to be turned on for the design, allowing the ENx pin(s) to control each desired output.

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3.3.9 Set EN_BUCKx Bits

Once the EN_PIN_CTRLx bits are set high for each output that needs to be turned on for the design, the EN_BUCKx bits for each corresponding output can also be set high. It is important that the EN_PIN_CTRLx bits are set before the EN_BUCKx bits so that no outputs are turned on accidentally. Once the EN_BUCKx bits are set high the MCU must be finished with the required I^2C commands and can move on to clearing interrupts and setting the ENx pin high to start startup sequence as described in Section 3.1.

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2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

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東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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