Application Note

Digital Control Implementation for Hybrid Hysteretic Control LLC Converter

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ABSTRACT

To address the challenge of traditional voltage mode control for LLC to meet the high load transient response requirements, HHC (hybrid hysteretic control) scheme was proposed to achieve the best-in-class transient performance with the analog controller. This application note discusses the key implementation details on how to design the HHC LLC with C2000, from the software and hardware perspective.

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1 Introduction

Voltage mode control has been typically used for LLC resonant converter where the output voltage loop directly controls the switching frequency. However, the compensation design is relatively challenging since the frequency response of the LLC converter with voltage mode control shows very complicated characteristics with multiple poles, and the location of the poles changes with input voltage and load conditions. [1]

With the higher requirement of load transient response requirements in power supply applications, some control methods like HHC (hybrid hysteretic control) or current mode control attract more attention in LLC converters. HHC scheme is proposed to achieve the best-in-class transient performance by overcoming the disadvantage of charge control and avoiding unstable condition by adding in a frequency ramp compensation [2]. It has changed the LLC plant transfer function to an equivalent first order system, characterized by a relatively stable cross frequency and small variation of DC gains, which has made the loop design easy to achieve higher bandwidth with enough phase margin.

Analog controllers, like UCC25640x series, are mature designs with HHC control schemes and widely used in the market. However, how to implement HHC LLC control scheme with digital controller has been requested for a long time from the market, especially for server PSU, which requires digital controllers for more flexible system design. The application report can discuss the design details on HHC LLC scheme with latest F2800x C2000 devices. Additional details can be found in the PMP41081 reference design, and the software of this design is available inside the latest C2000Ware Digital Power SDK.

2 HHC LLC Control Architecture and Logic Diagram

Figure 2-1 is a simplified schematic diagram of an LLC converter with HHC scheme. Compared to the voltage mode control, it is required to sense the voltage of resonant capacitor (VCR) and control the swing amplitude for HHC, which works as an inner loop in addition to the voltage control loop. Similar to the peak current control, the VCR control is used to controlling the energy transferred from resonant tank to the output for LLC. For the VCR sensing circuits, it can also leverage the existed current sense transformer, which is explained in the later section.

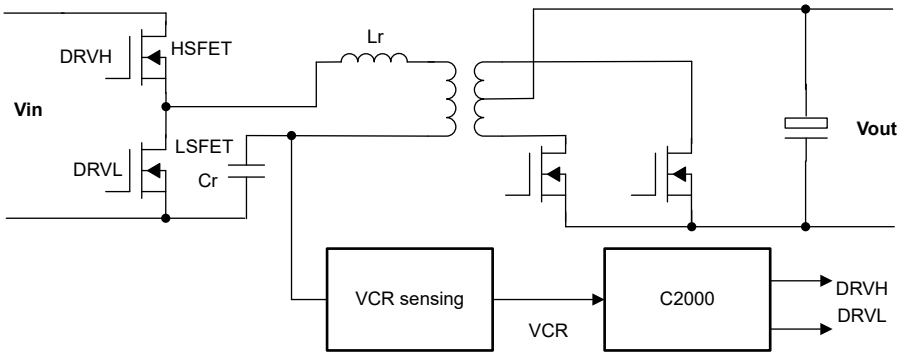

Figure 2-1. HHC LLC Schematic Diagram

Figure 2-2 shows the HHC control architecture within the C2000 MCU, which includes the outer voltage loop and hardware-based VCR loop. The voltage loop compensator generates the control value to the ramp generator of comparator subsystem module (CMPSS), based on the error from sensed voltage and reference voltage. The CMPSS compares the sensed VCR voltage with the ramp generator value, and generates events to control the PWM signal for the high side FET. CLB is used to create the PWM signal for the low side FET with a specific logic from the high side PWM.

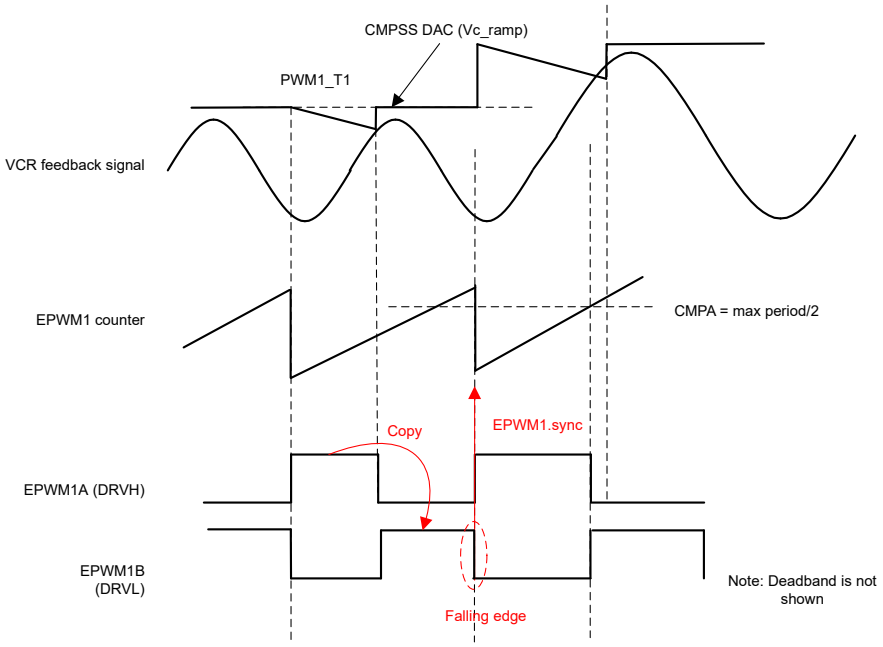

Figure 2-2. HHC LLC Control Architecture

Different from the traditional peak current mode control on buck, boost or phase shift full bridge topologies, which run with fixed switching frequency, while HHC LLC implements the peak current mode control for variable switching condition. Figure 2-2 shows the HHC switching waveform. When the VCR voltage swings up and comparator event is triggered, the high side FET can be turned off, and the low side FET can be turned on. In the later half cycle, the low side FET's on-time is kept as the same as the high side FET's. Similar with peak current mode control, a compensating slope is added to keep the control loop stable during the light load, when the VCR swing amplitude is very small.

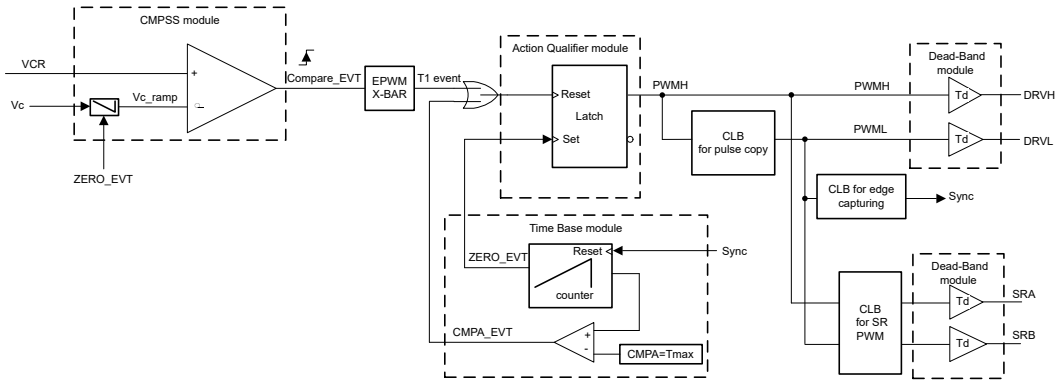

Figure 2-3. Block Diagram of the System Control Logic Within C2000

Figure 2-3 shows the block diagram of the HHC control logic, which mainly includes three peripherals of C2000.

2.1 CMPSS

CMPSS module receives the control value (Vc) calculated by voltage loop ISR (interrupt service routine), and set to the initial value of the internal ramp generator, which can provide the down-sloped VCR limitation (Vc_ramp) as the DAC value, based on the slope setting. CMPSS module compares the analog signal of VCR, and generates the trigger event (COMPARE_EVT) to trigger the ePWM module through ePWM X-BAR.

2.2 EPWM

All the submodules of Action Qualifier (AQ), Timer Base (TB), and Dead Band (DB) belongs to ePWM peripheral in C2000, and playing different roles in the HHC control logic. The DB module is commonly used to insert dead band between high side and low side PWM. And the dead band can be also used as the duty adjusting, and shutdown the PWM by setting the dead band to a large value. The AQ module is mainly used as a RS flip-flop, and set the PWMH to low at the moment of T1_event, which is same with COMPARE_EVT before the ePWM XBAR. The TB module is used to set the maximum on time of PWMH (Tmax), which refers to the setting of minimum switching frequency. The CMPA_EVT event can also clear the PWMH to low, when the time base counter is equal to the CMPA value.

2.3 Configurable Logic Block (CLB)

One CLB module is used to generate the symmetrical pulse from PWMH to PWML, and generate the sync event for all ePWM module to start the next switching cycle. Another CLB module is used to create the SR PWM signals for secondary FETs, which is independent to the HHC control.

3 C2000 Configurations in HHC LLC

3.1 CMPSS Configurations

To avoid sub-harmonics oscillation, slope compensation is required to induced for the inner current loop [1]. For C2000 devices, each CMPSS provides the ramp generator dedicated for slope compensation. As shown in Figure 3-1, the ramp generator produces a falling ramp waveform for the high-reference 12-bit DAC as the negative input of CMPSS. The calculated value from voltage control loop compensator is used to decide the initial value of the ramp register RAMPSTS. After receiving the selected ramp source signal (EPWM1SYNCE in this case), the defined slope value, is subtracted from RAMPSTS on every subsequent CPU cycle. In addition, to filter out the unexpected noise at the VCR signal, the suggestion is to enable the digital filter, which is helpful to avoid the unexpected comparator actions by switching noise. The recommendation is to select the latch output option of CMPSS for the further PWM control, since the latch feature ensures only the 1st comparator event can take effect, regardless of any further events within the same switching cycle. The latched output status of CMPSS is required to be cleared by the same EPWMxSYNCPER signal, to monitor the VCR signal in the new switching cycle.

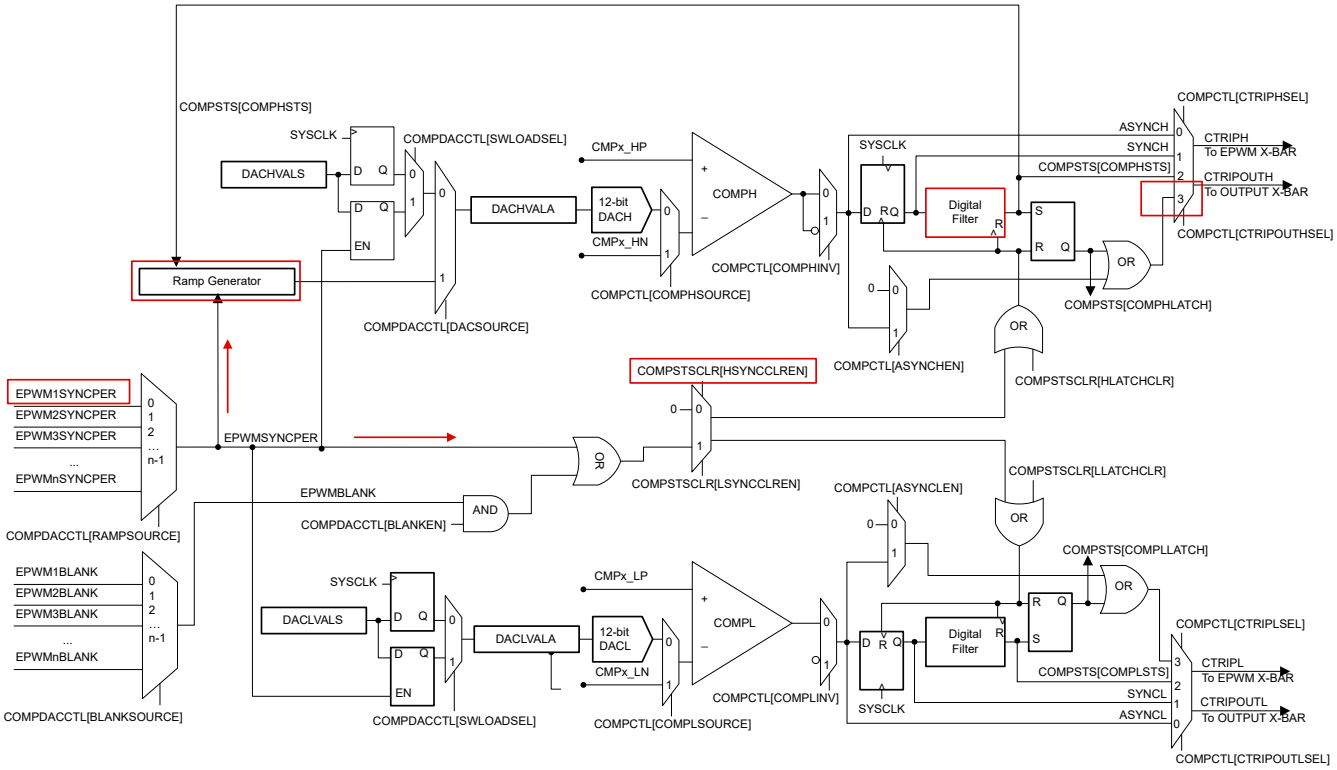

Figure 3-1. CMPSS Block Diagram

3.2 EPWM Configurations

The action qualifier (AQ) submodule of EPWM is configured as a RS latch, which controls the actions for the high side FET only. In this example, as shown in Figure 2-2, within the AQ module, EPWM1A is configured to set high at CTR= 0 event, and clear low at the comparator event, when the VCR signal and CMPSS ramp value intersect. To link the comparator event to EPWM, latest Type 4 EPWM provides the option to select the comparator event as the source for T1 event of AQ module. Note that the traditional trip action for peak current mode control with Trip Zone(TZ) module cannot apply for this case, since the TZ submodule is the final stage for the EPWM, so it cannot add the deadtime between EPWM1A and EPWM1B with the dead band (DB) module, while the AQ module is right before the DB module. More details regarding new T1/T2 features can refer to the technical reference manual.

For EPWM1B,the requirement is to generate the same pulse width as EPWM1A to achieve symmetry control. With the present EPWM features, it is difficult to make sure the same pulse width for EPWM1B automatically. Thus, CLB module is used in this design to generate the AQ output signal for EPWM1B.

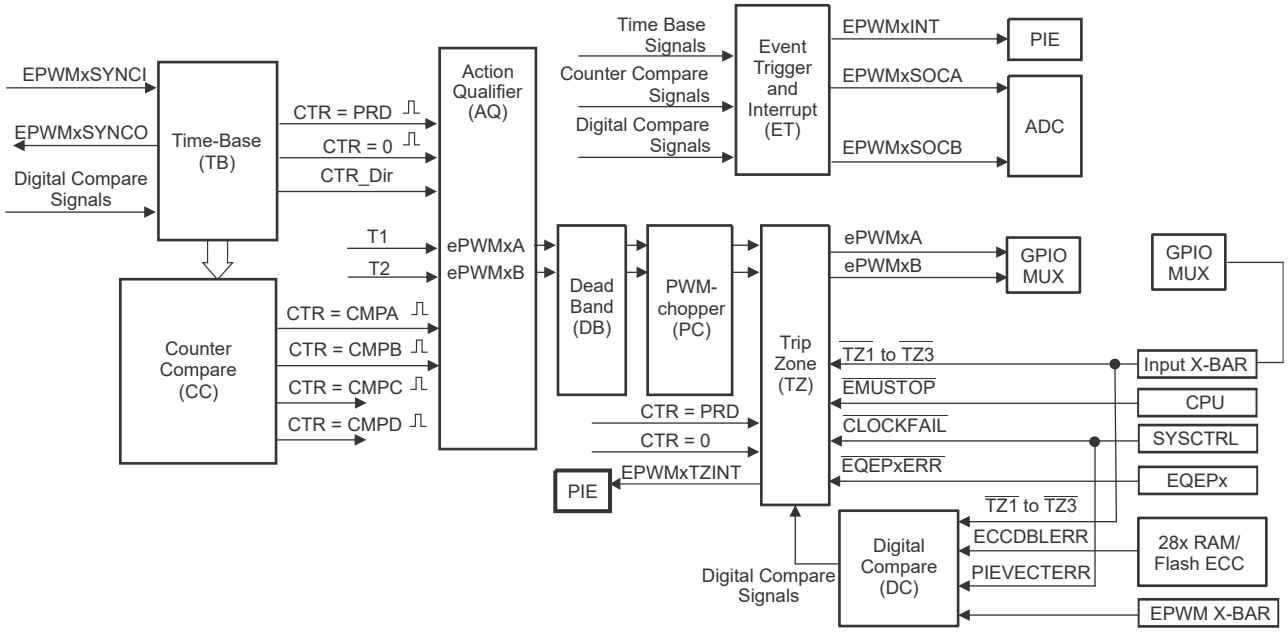

Figure 3-2. Action Qualifier Submodule

3.3 CLB Configurations

CLB is a peripheral on C2000 MCUs consisting of a number of look-up tables (LUTs), finite-state machines (FSMs) and counters which can be configured to perform complex logic operations. The LUT submodule can be used to implement simple combinatorial logic such as inverting a signal or ANDing multiple signals together. The FSM submodule can be used to implement state-based logic, such as an SR latch. The counter submodule features a 32-bit count register and can be used to perform operations such as counting the number of cycles a signal is high as well as dividing a clock signal. Interconnecting these submodules together can enable countless functions in a variety of applications. Each CLB tile contains a high-level controller (HLC) which can be triggered by signals within the CLB to perform set instructions. These instructions can include adding registers, subtracting registers, moving data between registers in the CLB, signaling interrupts to the CPU, and sending and receiving data from the CPU.

In the HHC LLC design, 2 CLB tiles are required. As for the synchronous rectification (SR) control, the challenge is to define the on time for SR PWM using normal EPWM configurations in advance, since the comparator event decides the turn-off timing of the primary-side PWM. Thus, CLB is leveraged to simplify the SR control for HHC LLC. For more details, please refer to Hardware-Based Synchronous Rectification Control with CLB.

For the primary side PWM configurations, CLB is used to make sure the identical pulse width of the high side and low side PWM signals (EPWM1A and EPWM1B). As shown in Figure 3-3, CLB is used to generated the AQ module output signal for EPWM1B, based on EPWM1A's AQ module output signal. EPWM1A's AQ module output signal is used to control the counter direction of CLB counter, which can start to count down after EPWM1A clears low. The natural way is to generate the symmetry counter signal. Then, by leveraging the falling edge of EPWM1A and the counter = 0 events, the expected signal for the EPWM1B can be generated by FSM.

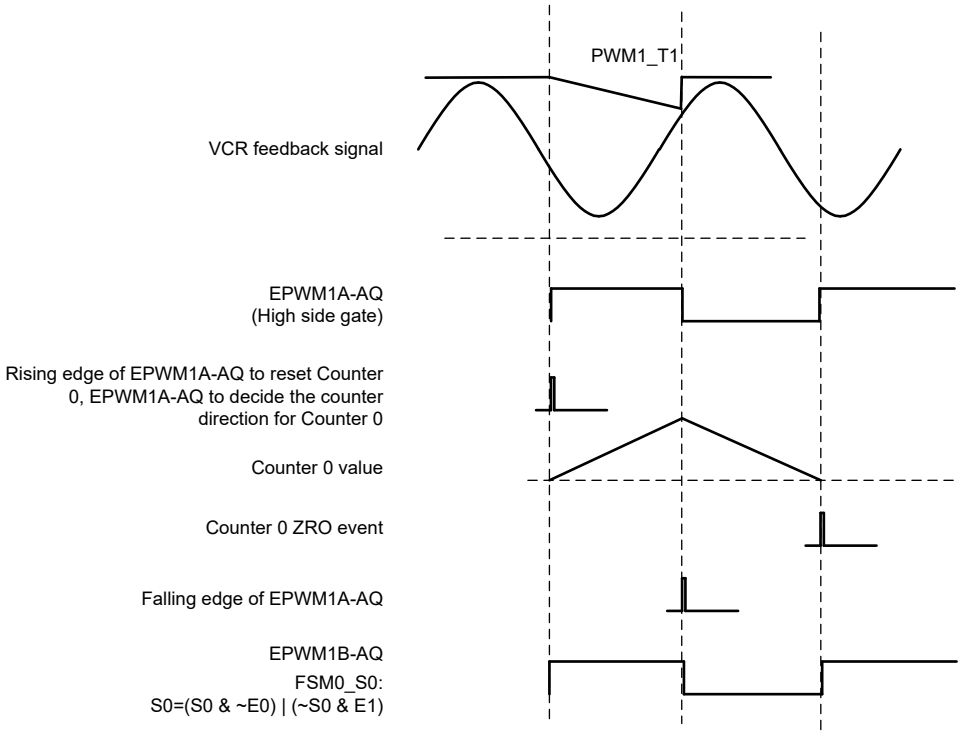

Figure 3-3. CLB Logic for Primary Side PWM

As indicated in Table 3-1, it is possible to use FSM0_S0 to override the AQ module output of EPWM1B, by assigning FSM0_S0 to Output 5 of the CLB1 module, directly with the CLB multiplexer output enable register CLB_OUT_EN.

Table 3-1. CLB Output Signal Multiplexer

CLB Output	CLB OUTLUT	CLB1Destination	CLB2Destination	CLB3Destination	CLB4Destination
0	OUTLUT0	EPWM1A	EPWM2A	EPWM3A	EPWM4A
1	OUTLUT1	EPWM1A_OE	EPWM2A_OE	EPWM3A_OE	EPWM4A_OE
2	OUTLUT2	EPWM1B	EPWM2B	EPWM3B	EPWM4B
3	OUTLUT3	EPWM1B_OE	EPWM2B_OE	EPWM3B_OE	EPWM4B_OE
4	OUTLUT4	EPWM1A_AQ	EPWM2A_AQ	EPWM3A_AQ	EPWM4A_AQ
5	OUTLUT5	EPWM1B_AQ	EPWM2B_AQ	EPWM3B_AQ	EPWM4B_AQ
6	OUTLUT6	EPWM1A_DB	EPWM2A_DB	EPWM3A_DB	EPWM4A_DB
7	OUTLUT7	EPWM1B_DB	EPWM2B_DB	EPWM3B_DB	EPWM4B_DB

Note that to add the rising edge delay to the EPWM1B final output signal, the FSM output generated by CLB is inverted first, then the falling edge delay can be enabled within the DB module.

In addition, the requirement is to generate the synchronization event for EPWM1 module at the falling edge of EPWM1B, which can be achieved by routing FSM_S0 output to the CLB output (Output 4), and then through EPWM X-BAR to configure the synchronization scheme.

A completed CLB configuration block diagram is shown in Figure 3-4.

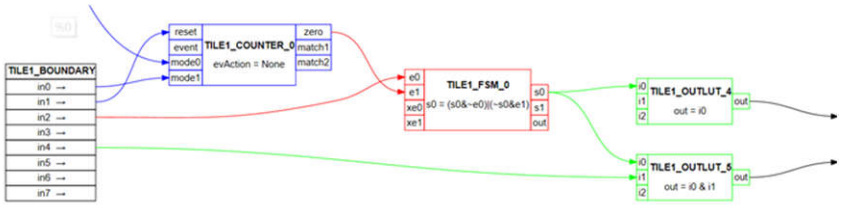

Figure 3-4. CLB Configuration Diagram

4 System Control Method

Since the HHC LLC control does not directly control the switching frequency, it requires different ways for the system control, especially for soft start, burst mode and frequency clamping.

4.1 Soft Start

Soft start process is aimed to build up the output voltage with controlled slew rate, which can avoid current inrush on both primary side and output side for LLC. Figure 4-1 summarizes the soft start flow.

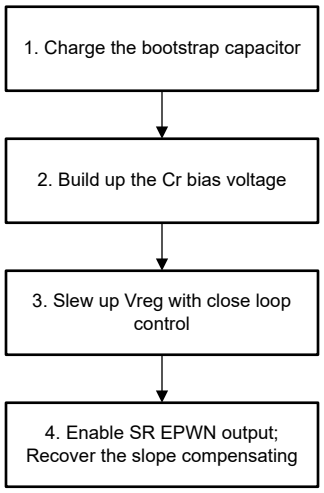

Figure 4-1. Soft Start Process

In the first stage of soft start, it requires to turn on the low side FET to charge the bootstrap capacitor, since the half bridge uses bootstrap power supply for the high side gate driver. This charging pulse can be much longer than driver's turn on delay, and make sure the bootstrap capacitor is completely charged.

As discussed in the Section 3.3, since the low side PWM (EPWM1B) is generated by the high side PWM (EPWM1A), EPWM1B can't be set to high independently. To generate the bootstrap pulse to EPWM1B, but keeping EPWM1A low, the CLB for PWML included another input to handle the bootstrap logic. As shown in Figure 3-4, the CLB input with GPREG bit (Input 4) is leveraged to create the AND logic with FSM0_S0 for EPWM1B, so that changing GPREG bit to logic "0" can set high for EPWM1B regardless of EPWM1A status. Users can define the timing for the on-time of EPWM1B based on system requirements, while keeping EPWM1A low with a large rising edge delay in the DB module configured.

In the second stage, the resonant capacitor voltage needs to be biased to the half of the input voltage, since for half bridge LLC, the offset of VCR is excluded in the HHC control algorithm. This bias voltage can be built up by several symmetry pulses of both the high side and the low side switches. The symmetrical pulses can be generated by a large compensating slope, which turns the HHC into traditional frequency adjusting as voltage mode control.

Then, in the third stage, the output voltage is built up with close loop control and gradually increase the voltage reference from 0V to 12V. When the reference is slewed up to the targeted setting voltage, the soft start process completes. The control scheme during this stage is explained in detail in the later section.

The fourth stage is the beginning of the normal operation. Note that SR PWM output is disabled to avoid any unexpected reverse current during the soft start process, and the initial slope compensation is enlarged to maintain stability control. In this stage, the SR PWM output can be slowly turned on by gradually reducing the deadtime of EPWM to the minimum setting value. In addition, both the slope and the minimum frequency clamping values are gradually recovered in this stage.

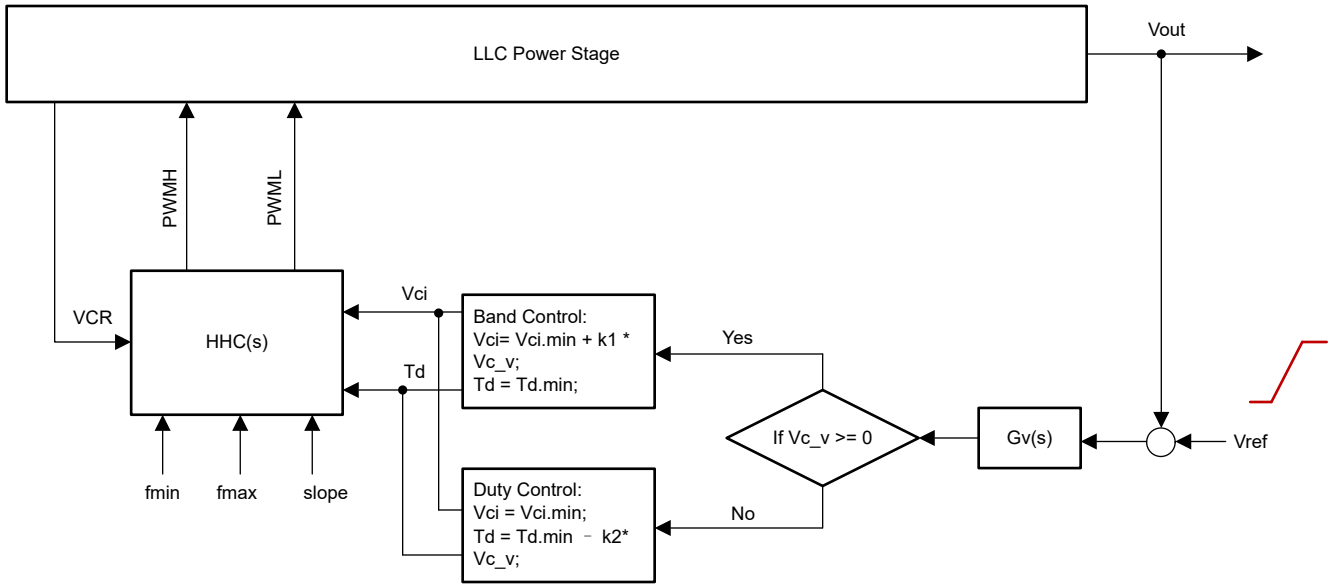

Figure 4-2. Control Algorithm During the Soft Start

There are five control parameters can be adjusted in the HHC control algorithm, shown in Figure 4-2.

1. Control band, Vci
2. Deadtime of primary EPWM, Td
3. Compensating slope, slope
4. Minimum frequency clamping, fmin
5. Maximum frequency clamping, fmax

During the soft start process, deadtime adjustment is included to reduce the inrush current when the output voltage is not high enough. And the mixed control of deadtime and control band adjustment is shown in Figure 4-2. When the voltage loop's compensator output Vc_v is higher than 0, the deadtime Td is set to the minimum value, and the control band Vci is increased from the minimum boundary. When Vc_v is lower than 0, Vci is set to the minimum value, and Td is increased from the minimum setting. Besides, if actual applications require to clamp the minimum on-time for the PWM pulse, it is possible to set the maximum deadtime limitation to achieve this feature. It means that if the deadtime calculated is larger than the maximum one, PWM output is directly turned off, so as to enter burst mode control naturally.

And during the third stage, the compensating slope is temporarily increased to a larger value to avoid oscillation and keep the control loop stable. The slope is reduced by 1unit once Vci reaches the maximum limitation, and can be gradually reduced to the targeted value after the soft start.

In addition, at the beginning of the soft start, the minimum switching frequency clamping fmin is temporarily increased higher than the resonant frequency, which is used to avoid entering the capacitive region when the output voltage is not high enough. And, the maximum frequency is also temporarily increased, to get lower voltage gain. Both minimum and maximum frequency clamping are gradually reduced to the normal value during or after the soft start process.

4.2 Burst Mode Control

During the normal operation condition after the soft start, the burst mode control is implemented to reduce the control gain during light load or no-load conditions. Different with the control schemes in the soft start, the deadtime value of PWM only uses two fixed values, normal one and larger one, which is used to disable PWM output. Thus, compared to the control algorithm in Figure 4-2, it removes the duty cycle adjustment mode by setting the deadtime to a maximum value when Vc_v is lower than 0, as shown in Figure 4-3.

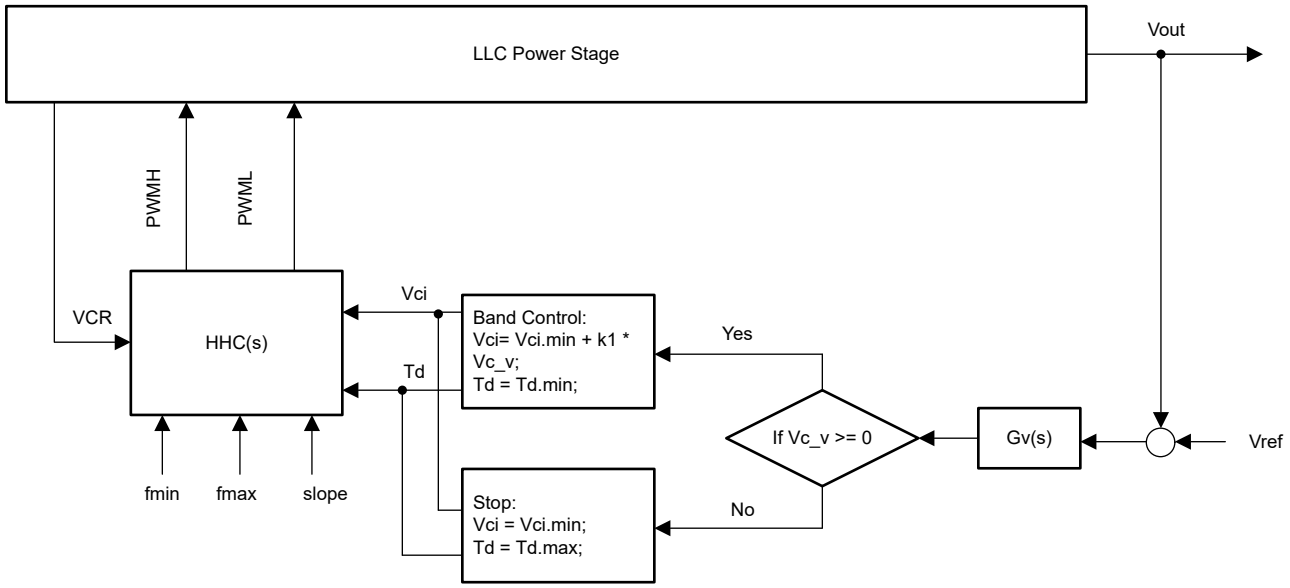

Figure 4-3. Control Algorithm During the Normal Operation

4.3 Minimum and Maximum Frequency Clamping

For LLC converters, to avoid the capacitive region (ZCS region) operation, which might cause MOSFET damaged due to the body diode reverse recovery, it is required to limit the minimum switching frequency according to the power stage parameters. Thus, in addition to the configurations in Chapter 3.2, another AQ module setting is induced, to clear low EPWM1A at the CTR=CMPA event, where CMPA value refers to the maximum switching period/2. In this way, the minimum switching frequency can be automatically clamped if the comparator event has not yet occurred.

In addition, to clamp the maximum switching frequency at the same time, it is possible to enable the blanking window for DCxEVT event (from CMPSS), so that if any comparator events occur within the blanking window, it can only take effect to clear low the PWM signal after the blanking window expires. Thus,

the duration of the blanking window refers to the minimum switching period/2, which starts from CTR= 0 pulse.

5 Resonant Capacitor Voltage Sensing Design

In HHC LLC control, the control object is the voltage variation on the resonant capacitor in a half switching cycle, and since normally the digital controller is placed in the secondary side, the VCR signal is required to be sensed across reinforced isolation. In the reference design PMP41081, it is implemented by a current sense transformer (CST) and an amplifier, as shown in Figure 5-1

The VCR signal is regenerated by integrating the CST current on a capacitor Cs. And, only the AC part of the resonant voltage is obtained, because the resonant current only includes the AC component. In other words, any DC offset or low frequency ripple across the resonant capacitor is ignored.

Besides, the operation amplifier is used to convert the differential voltage into single end with customized gains. The recommendation is to add another current sensing resistor, which is used for the resonant current for the system protection.

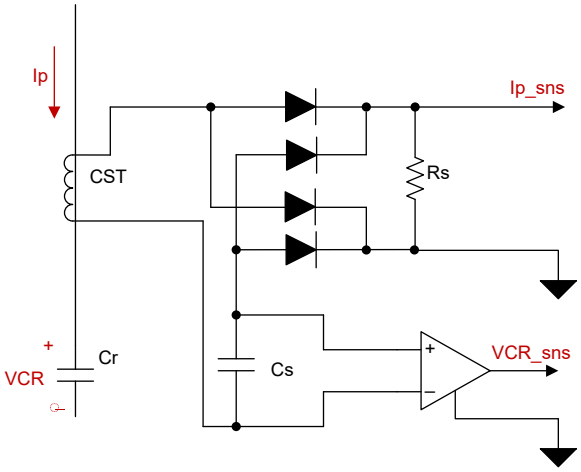

Figure 5-1. Simplified VCR Sensing Circuits

Before designing the VCR sensing circuits parameters, the requirement is to understand the LLC operation condition with the maximum VCR voltage amplitude, which generally refers to the minimum switching frequency with the minimum input voltage and maximum load current. This can be done either by a simulation, or an open loop testing based on the actual power stage.

We then need to select the sensing capacitor, to make sure the CST is operated far to be saturated. Based on the CST turn ratio and volt-time parameters in the data sheet, the limitation for sensing capacitor value is calculated with the following equation.

$$C_s > C_r \times \frac{\Delta VCR_{max}}{N_{ct} \times \frac{1}{5} \times VT_{product} \times 4 \cdot f_{s.min}} \quad (1)$$

- C_s is the sensing capacitor value
- C_r is the resonant capacitor value
- ΔVCR_{max} is the maximum amplitude of the VCR voltage
- N_{ct} is the turn ratio of CST
- $VT_{product}$ is the volt-time product of CST
- $f_{s.min}$ is the lowest operating frequency

After selecting the sensing capacitor, the differential sensing gain for the amplifier K_{OPA} can be decided by matching the maximum VCR sensing voltage to 2.0V in this design, which is limited by the ADC range of controller. Considering the stability of normal amplifiers, the recommendation is to design the differential sensing gain larger than 1.

$$K_{OPA} = \frac{2.0\text{V}}{\Delta VCR_{max}} \times \frac{N_{ct} \cdot C_s}{C_r} \quad (2)$$

In summary, the VCR sensing parameters can be designed with below process:

1. Get the maximum peak-peak VCR voltage by simulation or testing in the worst case;
2. Choose proper CST, and check the turn ratio N:1 and volt-time product;
3. Select a sensing capacitor, make sure CT far to saturate;
4. Adjust the sensing gain ratio and map the to 2.0V, recommend to use K_{OPA} > 1;

6 Summary

To help implement the HHC LLC using digital controller, the application note demonstrates the implementation details regarding the key C2000 peripherals, including the EPWM, CMPSS, and CLB. The document also provides guidance for the system control, and external sensing circuits design.

7 References

1. IEEE Xplore®, *Charge Current Control for LLC Resonant Converter.*
2. IEEE Xplore®, *A Practical Analytical Small Signal Mode Applied for the LLC Converter Based on Hybrid Hysteric Charge Control.*

8 Revision History

Changes from Revision * (June 2024) to Revision A (August 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated equation	11

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