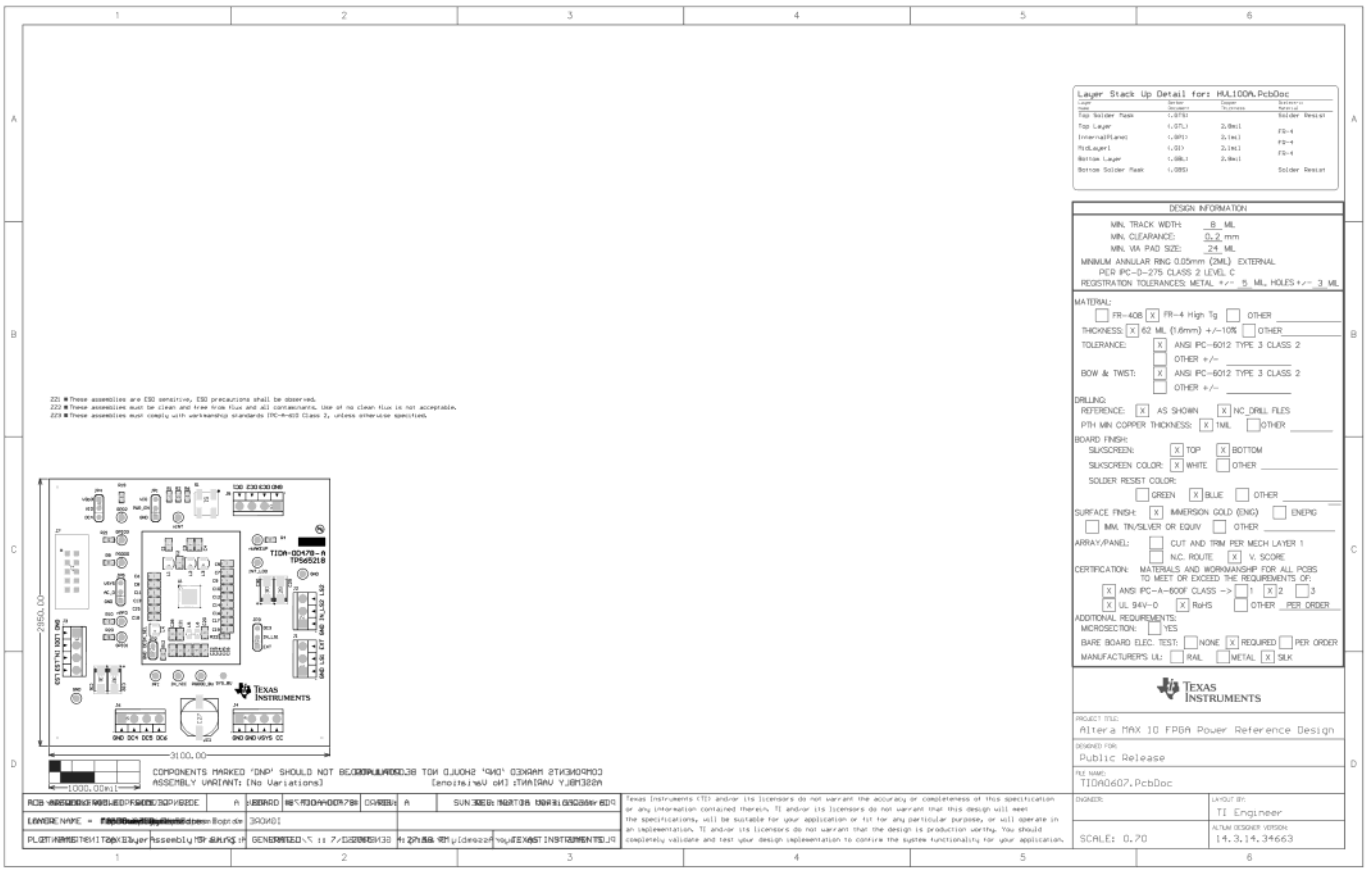
Layer Stack Up Detail for HVL100A.PcbDoc
Top Solder Mask (.07M) Solder Resist
Top Layer (.07L) 2.0mil FR-4
InternalPlane1 (.08P) 2.1mil FR-4
MidLayer1 (.01) 2.1mil FR-4
Bottom Layer (.08L) 2.0mil FR-4
Bottom Solder Mask (.08S) Solder Resist
DESIGN INFORMATION
MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
MATERIAL:
FR-408 X FR-4 High Tg OTHER
THICKNESS: X 62 MIL (1.6mm) +/-10% OTHER
TOLERANCE: X ANSI IPC-6012 TYPE 3 CLASS 2
OTHER +/-
BOW & TWIST: X ANSI IPC-6012 TYPE 3 CLASS 2
OTHER +/-
DRILLING:
REFERENCE: X AS SHOWN X NC_DRILL FILES
PTH MIN COPPER THICKNESS: X 1MIL OTHER
BOARD FINISH:
SILKSCREEN: X TOP X BOTTOM
SILKSCREEN COLOR: X WHITE OTHER
SOLDER RESIST COLOR:
GREEN X BLUE OTHER
SURFACE FINISH: X IMMERSION GOLD (ENIG) ENEPIG
IMM. TIN/SILVER OR EQUIV OTHER
ARRAY/PANEL: CUT AND TRM PER MECH LAYER 1
N.C. ROUTE X V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
X ANSI IPC-A-600F CLASS -> 1 X 2 3
X UL 94V-0 X RoHS OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE X REQUIRED PER ORDER
MANUFACTURERS UL: RAIL METAL X SILK
Texas Instruments
PROJECT TITLE:
Altera MAX 10 FPGA Power Reference Design
DESIGNED FOR:
Public Release
FILE NAME:
TIDA00607.PcbDoc
LAYOUT BY:
TI Engineer
ALTIUM DESIGNER VERSION:
14.3.14.34663
SCALE: 0.70
2950.00
3100.00
1000.00mil
COMPONENTS MARKED 'DNP' SHOULD NOT BE
ASSEMBLY VARIANT: [No Variations]
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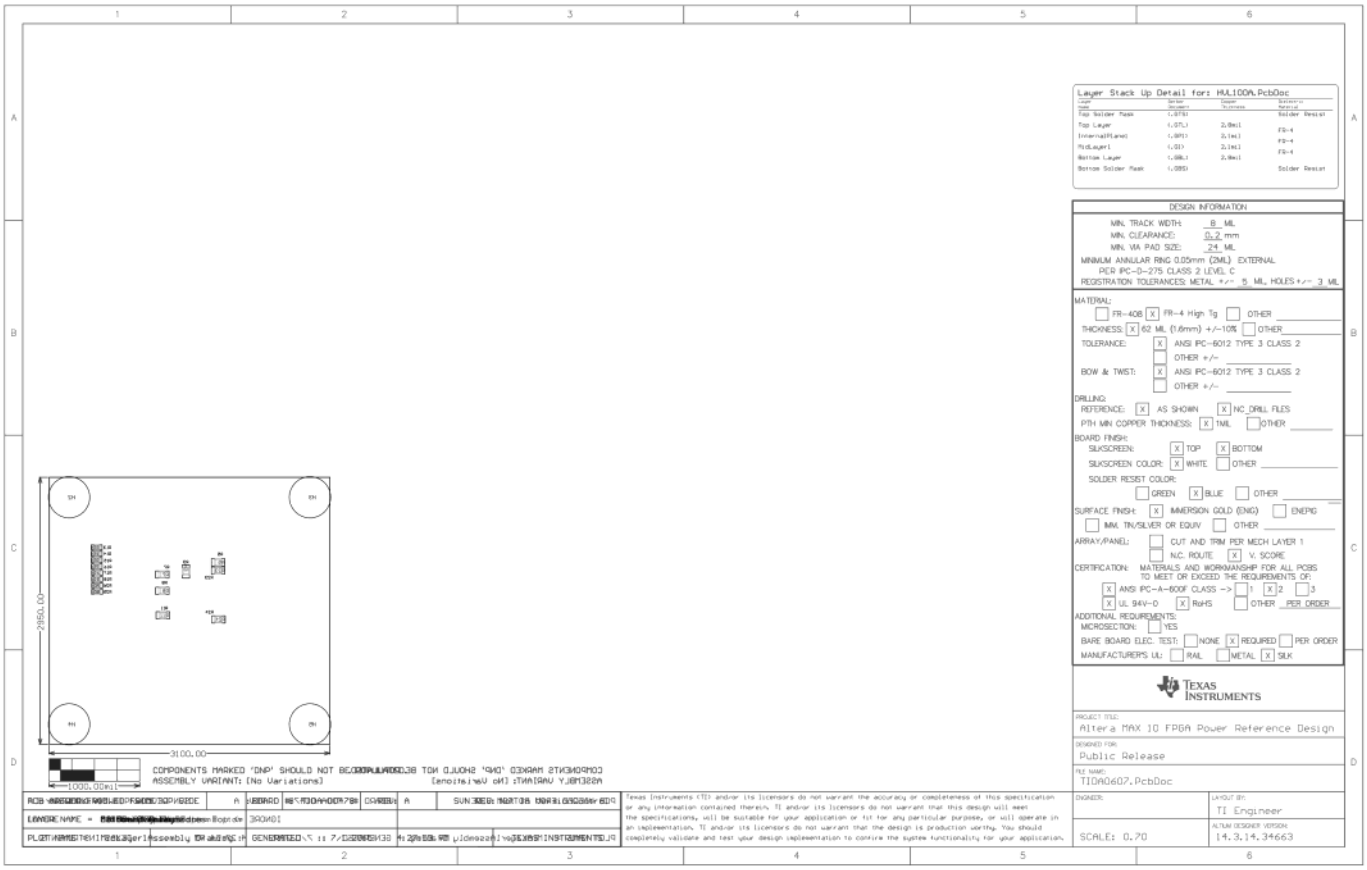
Layer Stack Up Detail for: HUL100A.PcbDoc
DESIGN INFORMATION
MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
MATERIAL:
FR-408 X FR-4 High Tg OTHER
THICKNESS: X 62 MIL (1.6mm) +/-10% OTHER
TOLERANCE: X ANSI IPC-6012 TYPE 3 CLASS 2
OTHER +/-
BOW & TWIST: X ANSI IPC-6012 TYPE 3 CLASS 2
OTHER +/-
DRILLING:
REFERENCE: X AS SHOWN X NC_DRILL FILES
PTH MIN COPPER THICKNESS: X 1MIL OTHER
BOARD FINISH:
SILKSCREEN: X TOP X BOTTOM
SILKSCREEN COLOR: X WHITE OTHER
SOLDER RESIST COLOR:
GREEN X BLUE OTHER
SURFACE FINISH: X IMMERSION GOLD (ENIG) ENEPIG
IMM. TIN/SILVER OR EQUIV OTHER
ARRAY/PANEL: CUT AND TRIM PER MECH LAYER 1
N.C. ROUTE X V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
X ANSI IPC-A-600F CLASS -> 1 X 2 3
X UL 94V-0 X RoHS OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE X REQUIRED PER ORDER
MANUFACTURER'S ID: RAIL METAL X SILK
Texas Instruments
PROJECT TITLE:
Altera MAX 10 FPGA Power Reference Design
DESIGNED FOR:
Public Release
FILE NAME:
TIDA0607.PcbDoc
DRAWN BY:
LAYOUT BY:
TI Engineer
SCALE: 0.70
ALTIUM DESIGNER VERSION:
14.3.14.34663
2950.00
3100.00
1000.00mil
COMPONENTS MARKED 'DNP' SHOULD NOT BE
ASSEMBLY VARIANT: [No Variations]
BOARD
GENERATED
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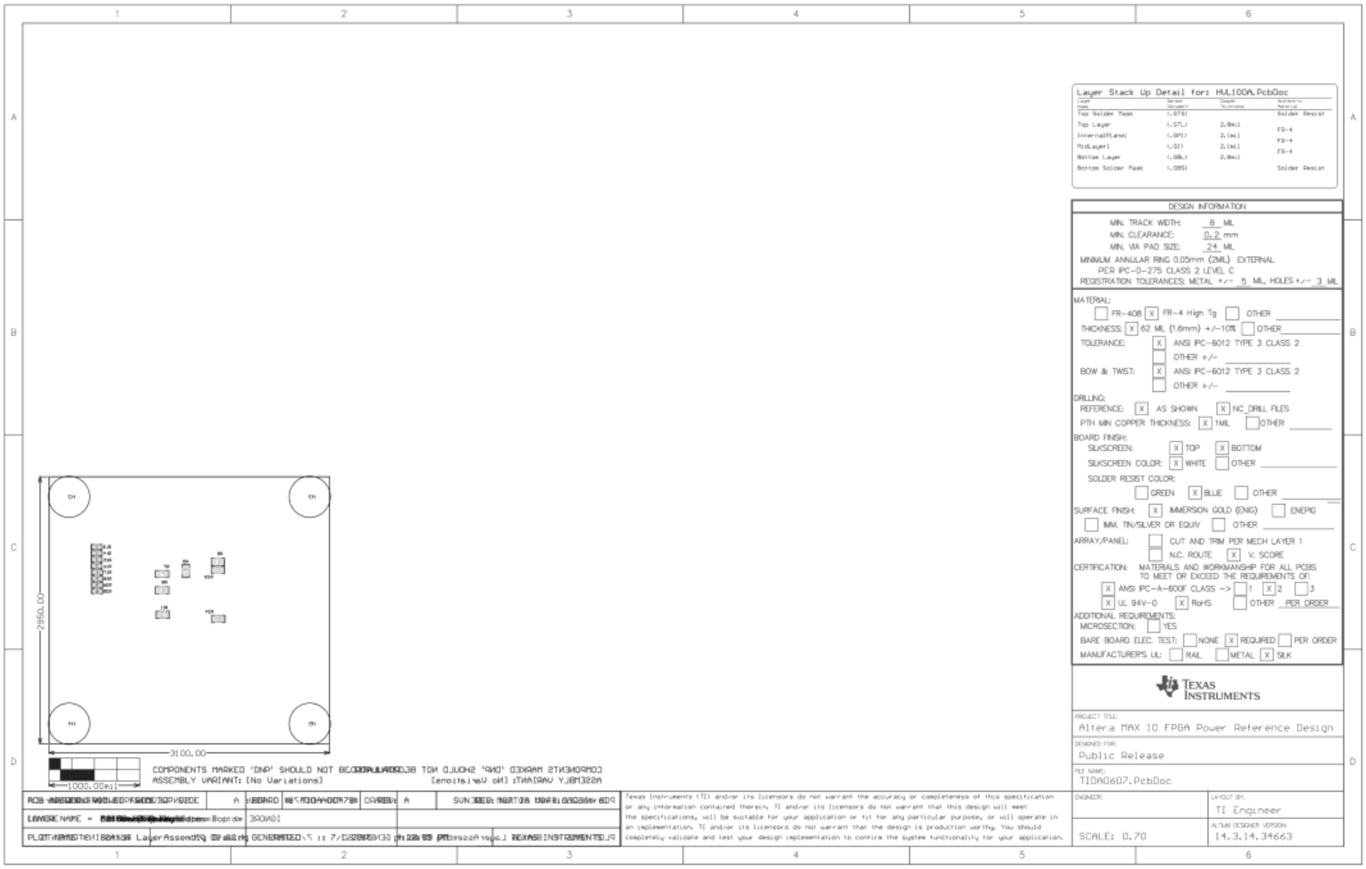
Layer Stack Up Detail for: HVL100A.PcbDoc
Top Solder Mask (.GTS) Solder Resist
Top Layer (.GTL) 2.0mil
InternalPlane1 (.GP1) 2.1mil
MidLayer1 (.G1) 2.1mil
Bottom Layer (.GBL) 2.0mil
Bottom Solder Mask (.GBS) Solder Resist
FR-4
FR-4
FR-4
DESIGN INFORMATION
MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
MATERIAL:
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THICKNESS: X 62 MIL (1.6mm) +/-10% OTHER
TOLERANCE: X ANSI IPC-6012 TYPE 3 CLASS 2
OTHER +/-
BOW & TWIST: X ANSI IPC-6012 TYPE 3 CLASS 2
OTHER +/-
DRILLING:
REFERENCE: X AS SHOWN X NC_DRILL FILES
PTH MIN COPPER THICKNESS: X 1MIL OTHER
BOARD FINISH:
SILKSCREEN: X TOP X BOTTOM
SILKSCREEN COLOR: X WHITE OTHER
SOLDER RESIST COLOR:
GREEN X BLUE OTHER
SURFACE FINISH: X IMMERSION GOLD (ENIG) ENEPIG
IMM. TIN/SILVER OR EQUIV OTHER
ARRAY/PANEL: CUT AND TRIM PER MECH LAYER 1
N.C. ROUTE X V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS
TO MEET OR EXCEED THE REQUIREMENTS OF:
X ANSI IPC-A-600F CLASS -> 1 X 2 3
X UL 94V-0 X RoHS OTHER PER ORDER
ADDITIONAL REQUIREMENTS:
MICROSECTION: YES
BARE BOARD ELEC. TEST: NONE X REQUIRED PER ORDER
MANUFACTURER'S UL: RAIL METAL X SILK
TEXAS INSTRUMENTS
PROJECT TITLE:
Altera MAX 10 FPGA Power Reference Design
DESIGNED FOR:
Public Release
FILE NAME:
TIDA0607.PcbDoc
ENGINEER:
LAYOUT BY:
TI Engineer
SCALE: 0.70
ALTIUM DESIGNER VERSION:
14.3.14.34663
2950.00
3100.00
1000.00mil
COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED
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