PMP8673RevB Test Results

Topology:	Sync. Boost
Device:	LM5121
RC snubber:	OPEN / 4.7Ohm, 330pF

Basic Data:	*Fsw 400kHz, correct to a dot*
ON:	*33.7V*
OFF:	*30.5V*
CS threshold:	*trips at 6.0A input current, corresponding to 3.7A output current*
Total Efficiency:	*>97%*
Output Voltage Ripple:	*150mVpp (<0.5%)*
Transient Response:	*300mVpk @ 500mA<->3A (<1%)*
Load Regulation:	*20mV (<0.05%)*

1 Startup

The startup waveform is shown in the Figure 1. The input voltage was set at 35V, with 3A load at the output. Power supply was switched on, ON at 33.7V input, . startup 16ms:

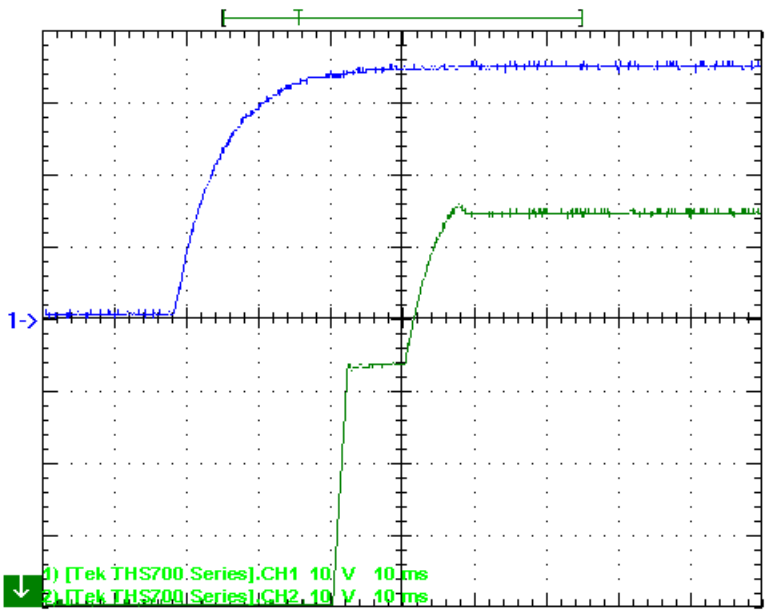


Figure 1

Ch1=> input voltage 10V/div

Ch2=> output voltage 10V/div

10ms/div

2 Shutdown

The shutdown waveform is shown in the Figure 2. The input voltage was set at 35V, with 3A load on the output. Power supply was switched off (input shorted):

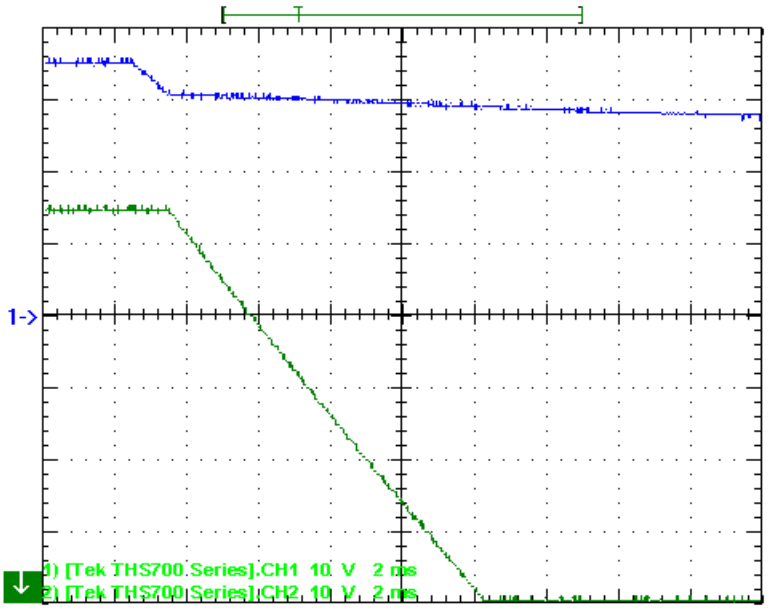


Figure 2

Ch1=> input voltage 10V/div

Ch2=> output voltage 10V/div

2ms/div

3 Efficiency

The efficiency is shown in the Figure 3 below. The input voltage was set to 35V:

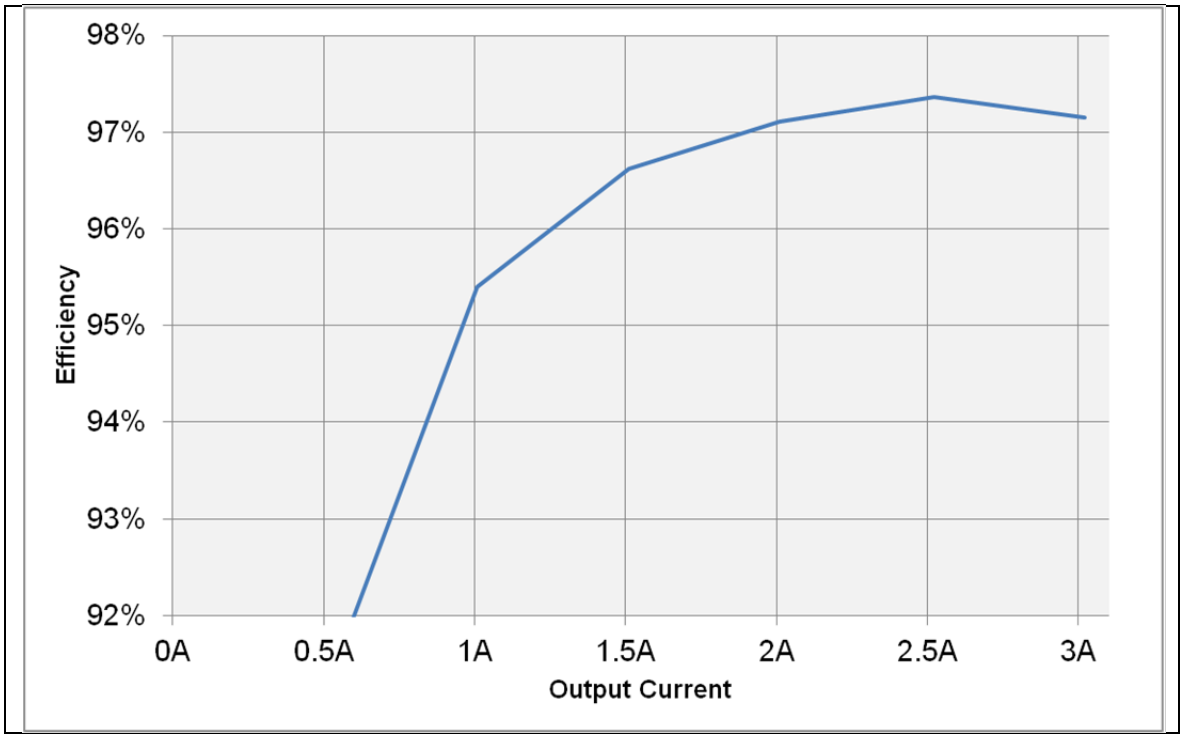


Figure 3

Vin(V)	*Iin(A)*	*Vout*	*Iout*	*Pin(W)*	*Pout*	*Effcy*
35.003	4.926	55.448	3.021	172.42	167.51	**0.9715**
35.005	4.103	55.447	2.522	143.63	139.84	**0.9736**
35.006	3.277	55.449	2.009	114.71	111.4	**0.9711**
35.006	2.477	55.449	1.511	86.71	83.783	0.9663
35.006	1.675	55.451	1.0088	58.635	55.939	0.954
35.007	0.8694	55.453	0.5003	30.435	27.743	0.9116

Effcy >97% in a load range 2A..3A (filter included); power losses 4.91W at full load 3A.

4 Load Regulation

The load regulation of the output is shown in the Figure 4 below. The input voltage was set to 35V. Load regulation 20mV (<0.05%):

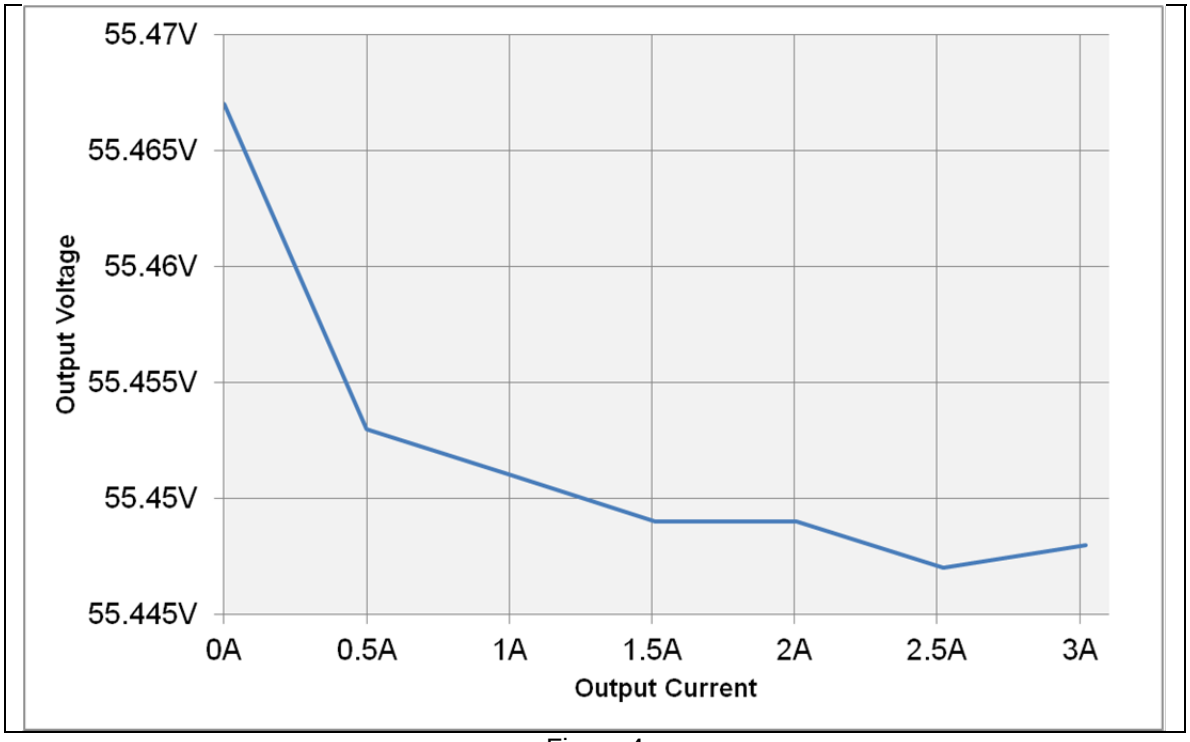


Figure 4

5 Ripple Voltages

The **output** ripple voltage is shown in Figure 5. The image was taken with a 3A load 35V at the input, du = 150mVpp sinewave:

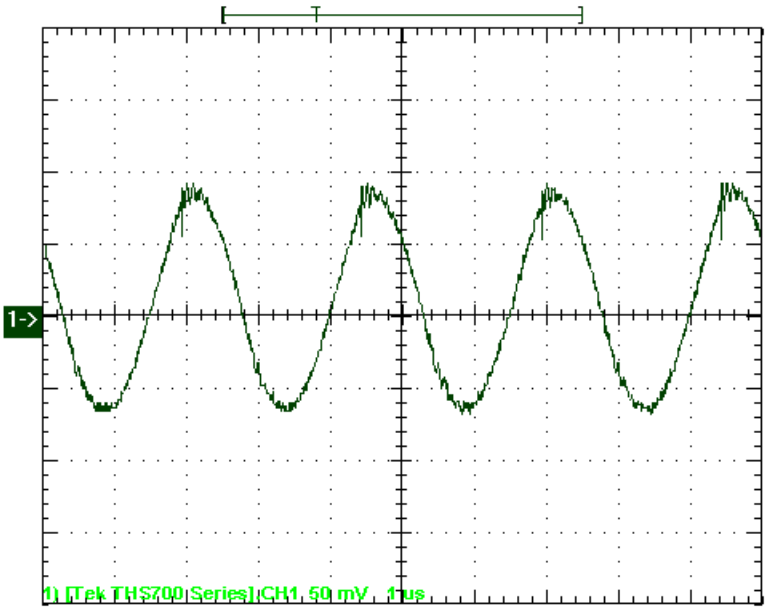


Figure 5

Ch1 => output voltage **50mV**/div

AC coupled

20MHz bandwidth setting

1µs/div

The output ripple voltage before filtering is shown in Figure 6. The image was taken with a 3A load 35V at the input, du 1500mV, filter attenuation 0.1 means -20dB:

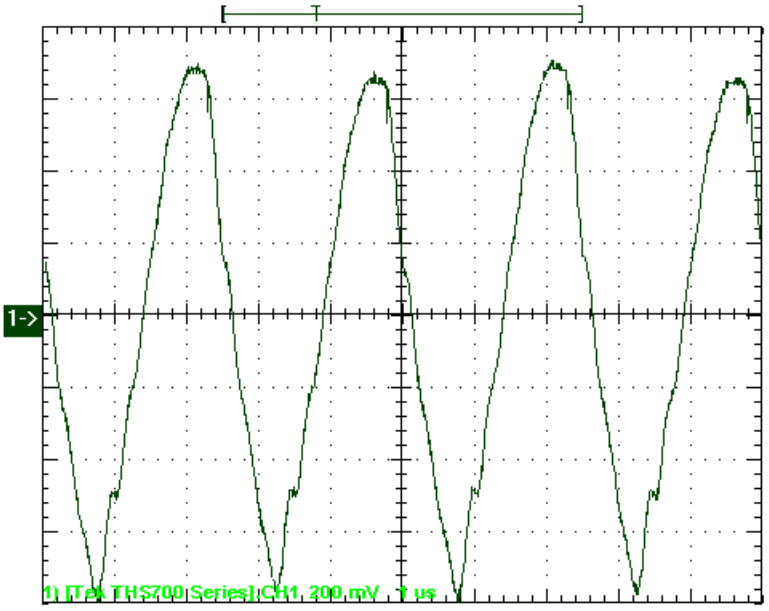


Figure 6

Ch1 => output voltage **200mV**/div

AC coupled

20MHz bandwidth setting

1µs/div

The **input** ripple voltage is shown in Figure 7. The image was taken with a 3A load 35V at the input, 50mVpp sinewave (reflected voltage ripple depends on source impedance):

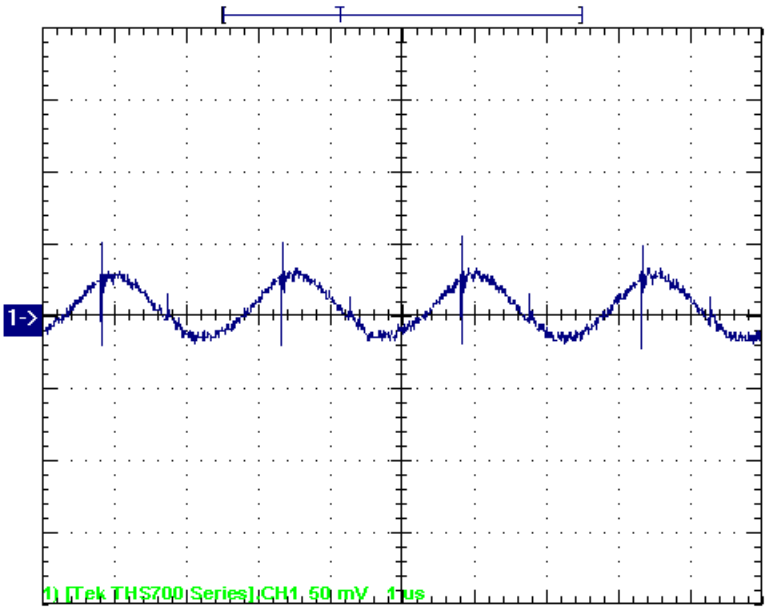


Figure 7

Ch1 => input voltage 50mV/div

20MHz bandwidth setting

1µs/div

6 Control Loop Frequency Response

Figure 8 shows the loop response with 3A load and 35V input.

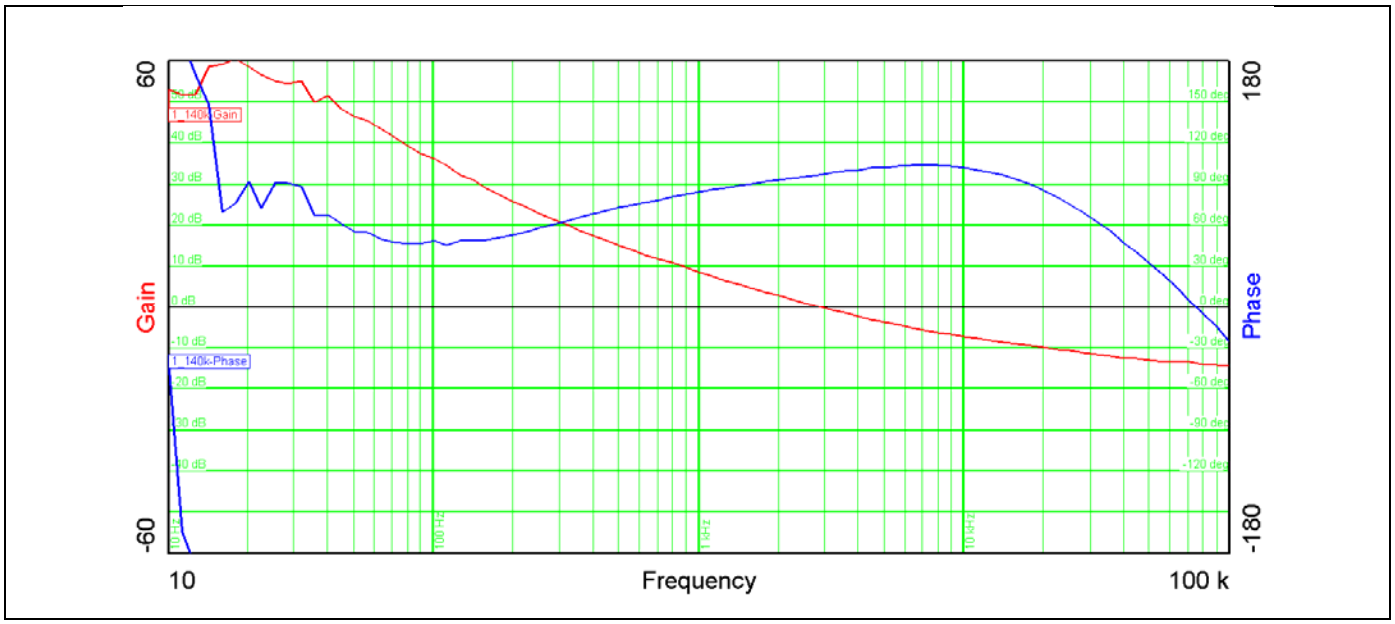


Figure 8

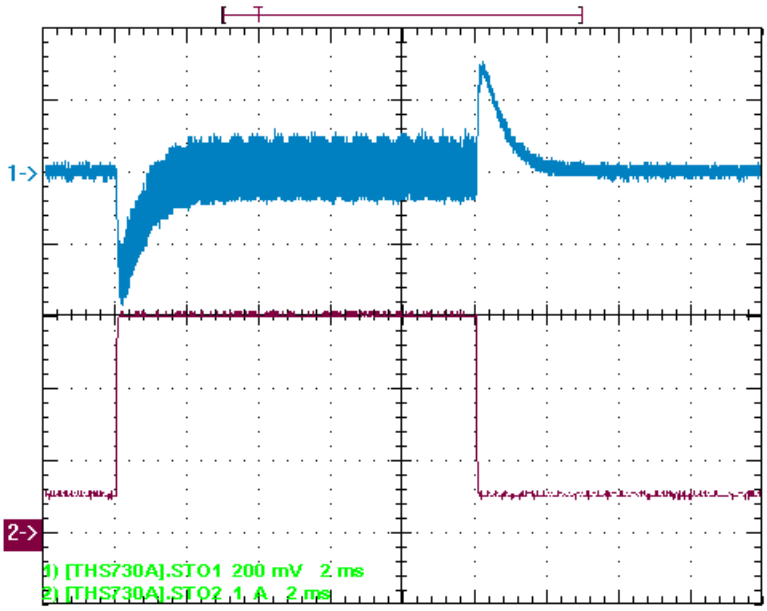
Table 1 summarizes the results from Figure 8

Bandwidth (kHz)	2.88
Phasemargin	97°
slope (20dB/decade)	-0.872
gain margin (dB)	-13.7
slope (20dB/decade)	-0.618
freq (kHz)	75.3

Table 1

7 Load Transients

The Figure 9 shows the response to load transients. The load is switching from 0.5A to 3A. The input voltage was set to 35V, transient response du is 300mVpk, <1%:



Ch1 => output voltage 200mV/div

20MHz bandwidth setting

Ch2 => output current 1A/div

2ms/div

Figure 9

8 Miscellaneous Waveforms

8.1 Switch node (Low Side FET)

With input voltage set to 35V and 3A Iout results in the waveform shown in Figure 10

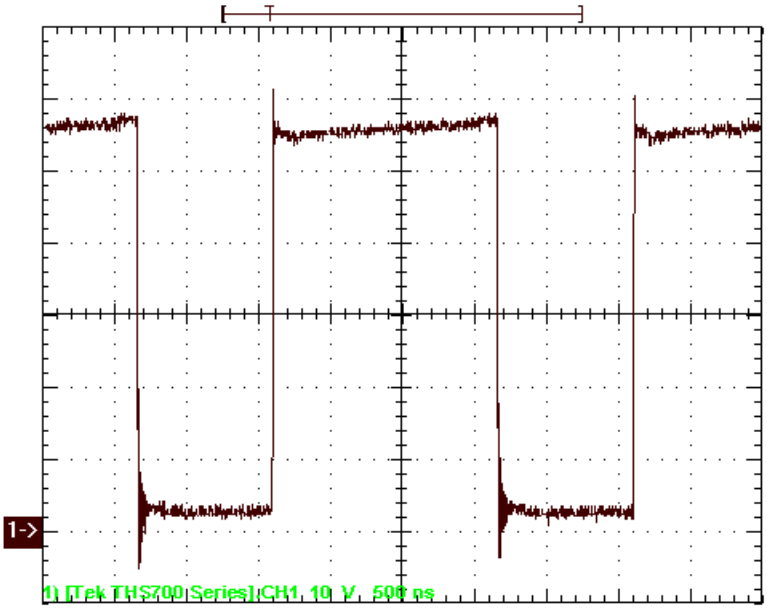
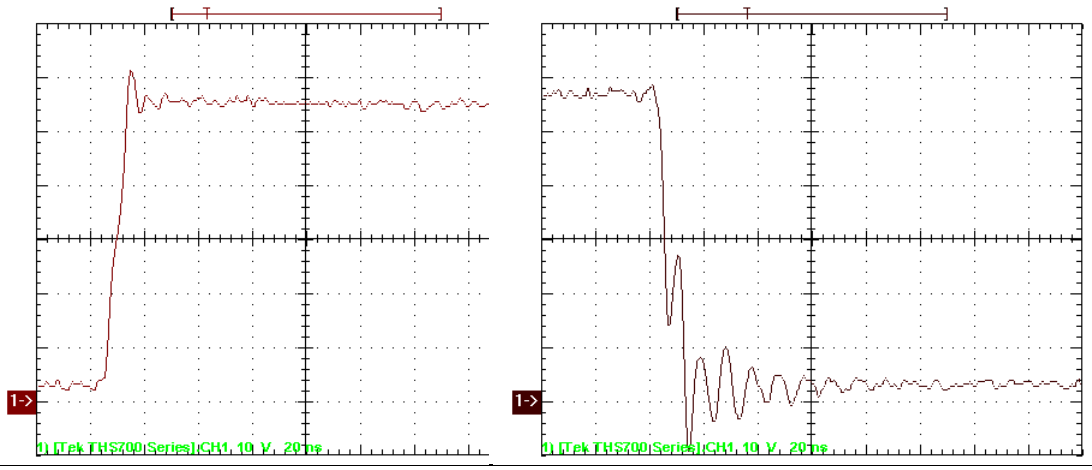
	Ch1 => Vds LS 10V/div 500ns/div full bandwidth
	Ch1 => Vds LS 10V/div 20ns/div

Figure 10

8.2 Gate Control of Low side MOS-FET Q2

Figure 11 shows the gate control Q2; with input voltage set to 35V and 3A Iout results in the waveform shown below:

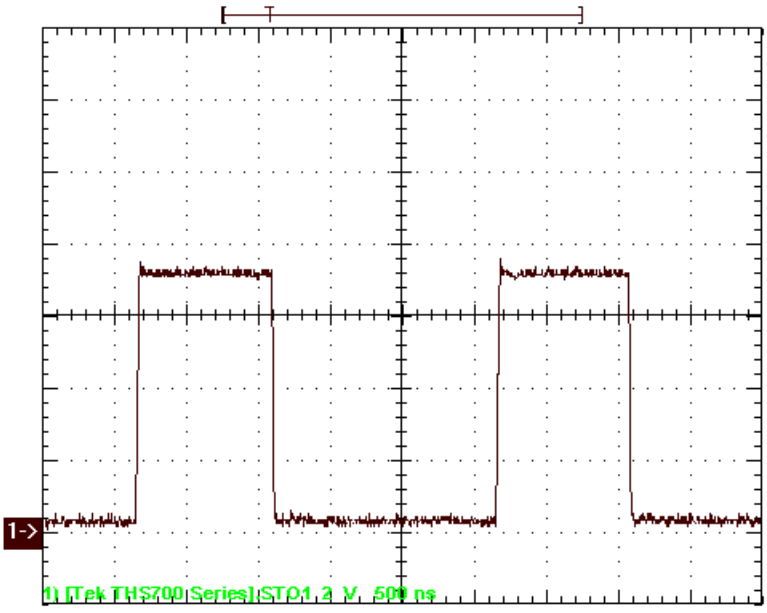
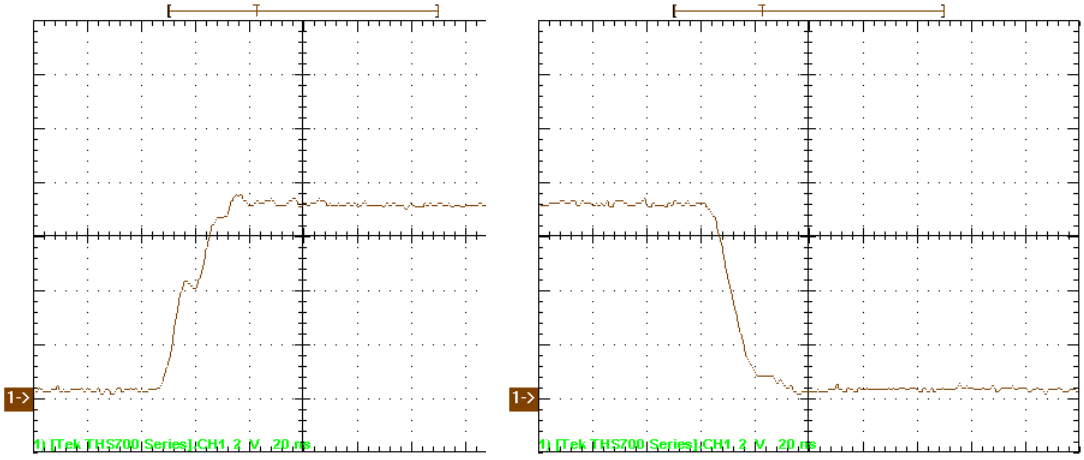
	Ch1 => Vgs LS 2V/div 500ns/div Bw = 20MHz
	Ch1 => Vgs LS 2V/div 20ns/div Bw = 20MHz

Figure 11

8.3 Hi Side MOS FET Q3 w/o RC snubber

The waveform is shown in Figure 12.(the same setup as above), OS 90V/100MHz:

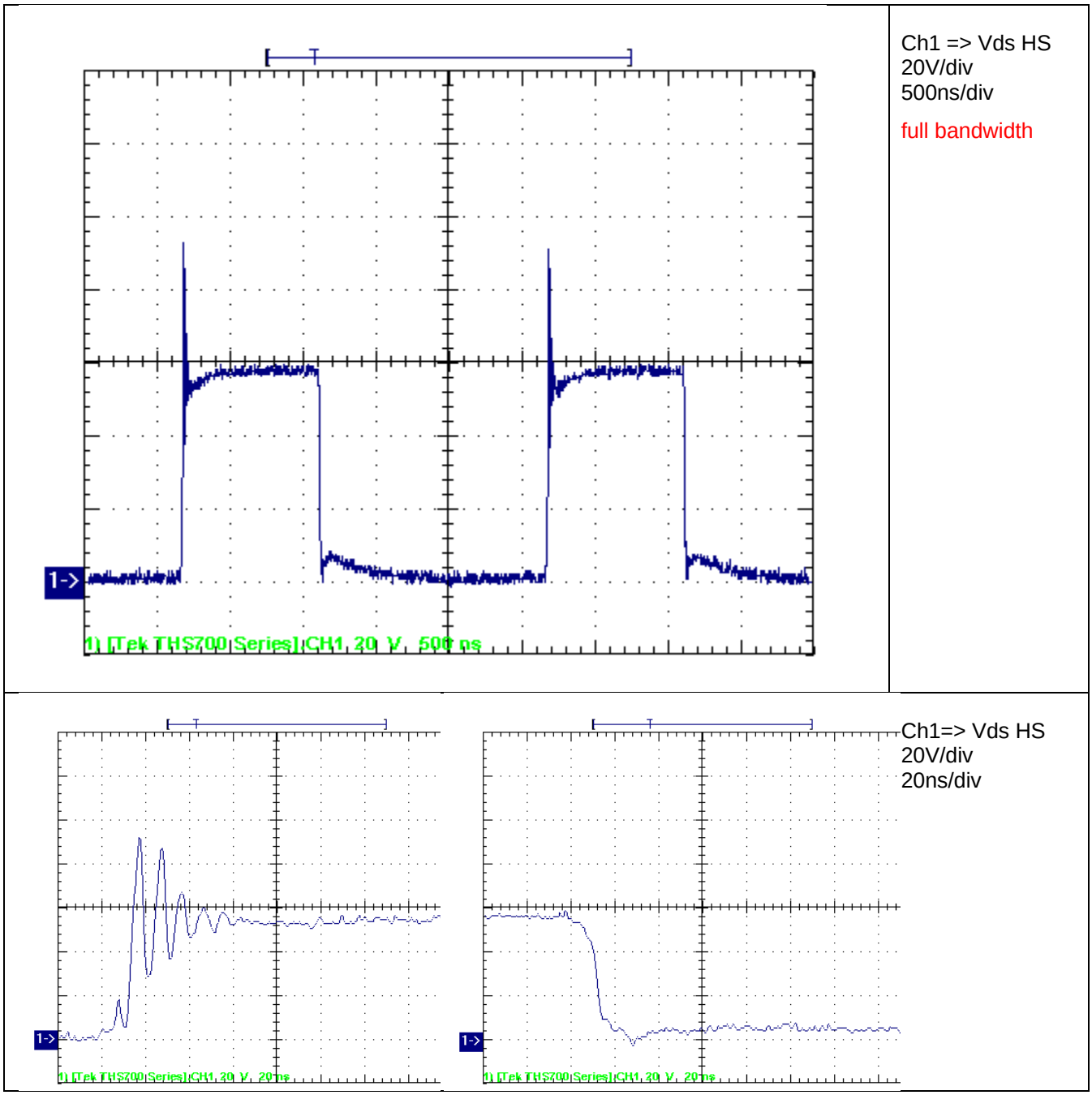


Figure 12

A RC snubber circuit 330pF / 4.7Ohm was implemented to reduce overshoot and RF ringing:

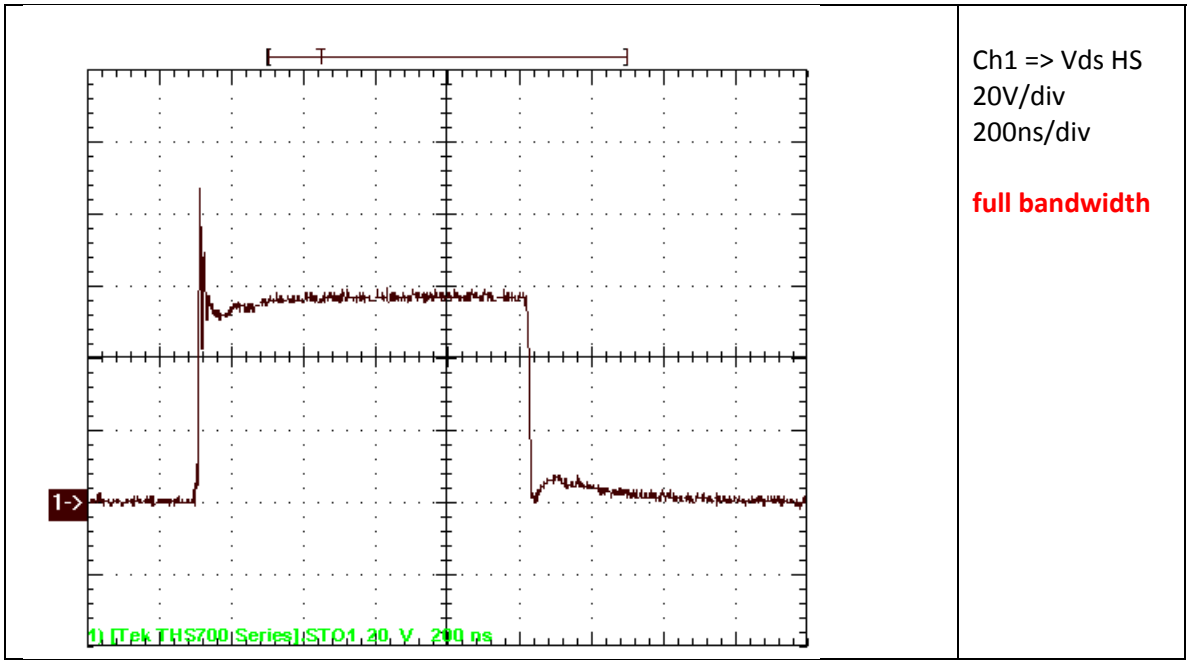


Figure 13

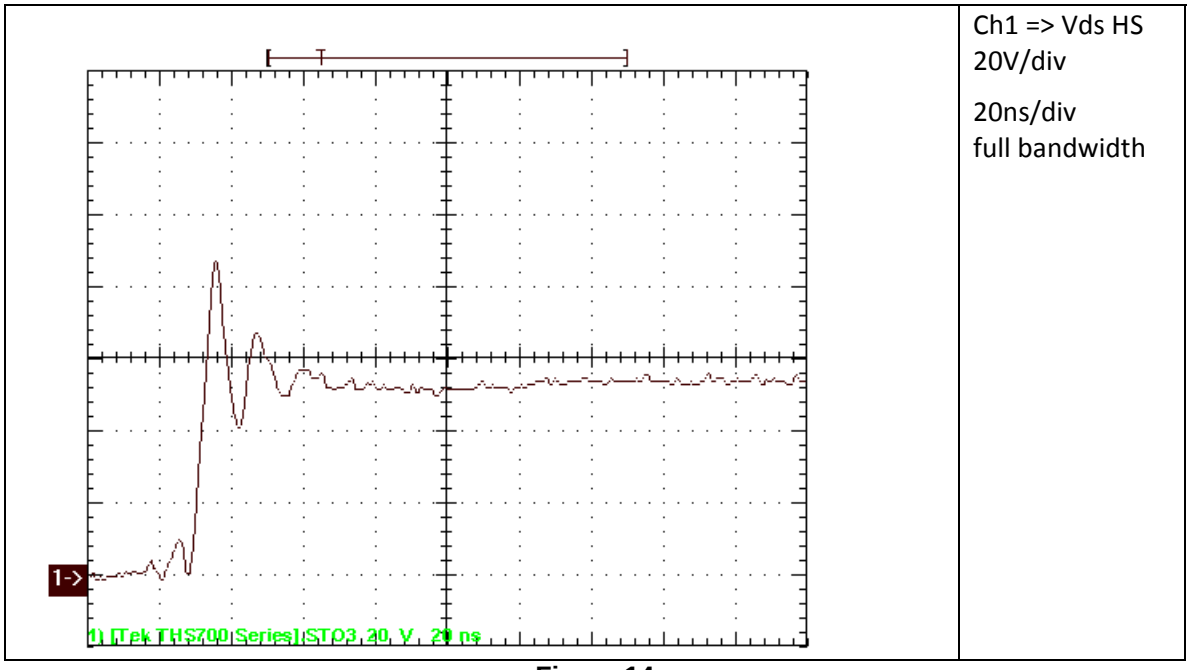


Figure 14

Gate Control of High Side MOS FET Q3

With input voltage set to 35V and 3A Iout results in the waveform shown in Figure 15:

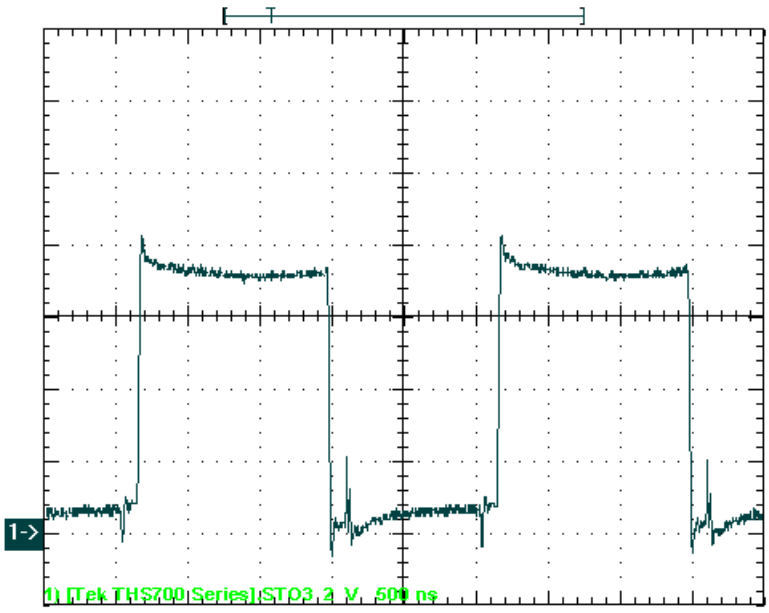
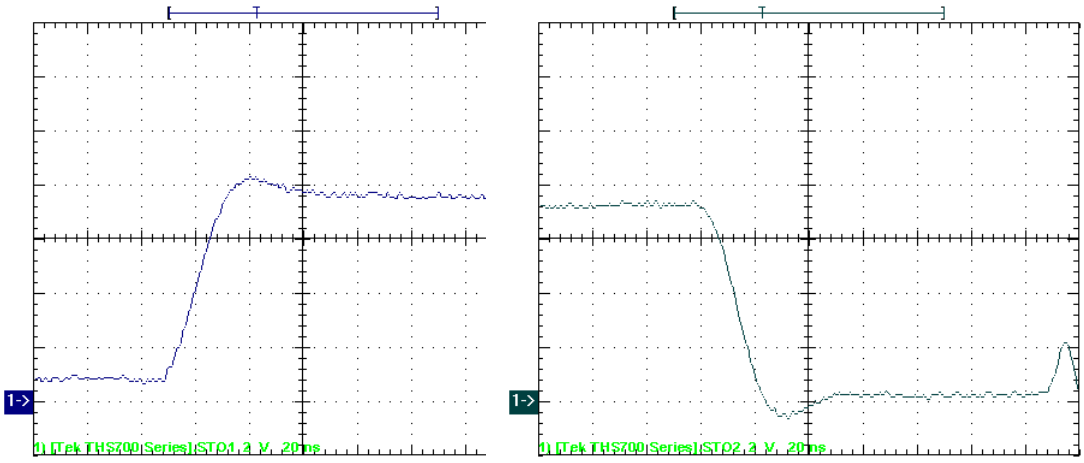
	Ch1 => Vgs HS 2V/div 500ns/div BW 20MHZ
	Ch1 => Vgs HS 2V/div 20ns/div BW 20MHz

Figure 15

9 Thermal Image

Figure 16 shows the thermal image at 35V input and 2A output = 110W output power

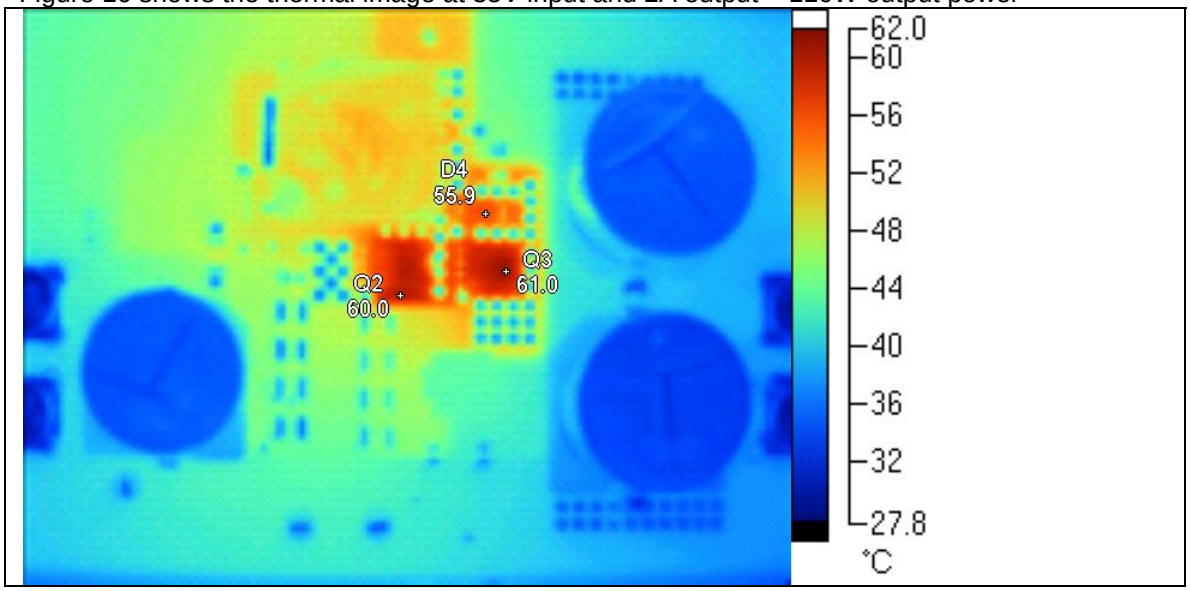


Figure 16

Name	Temperature
Q3	61.0°C
Q2	60.0°C
D4	55.9°C

Table 2

Figure 17 shows the thermal image at 35V input and 3A output = 165W output power

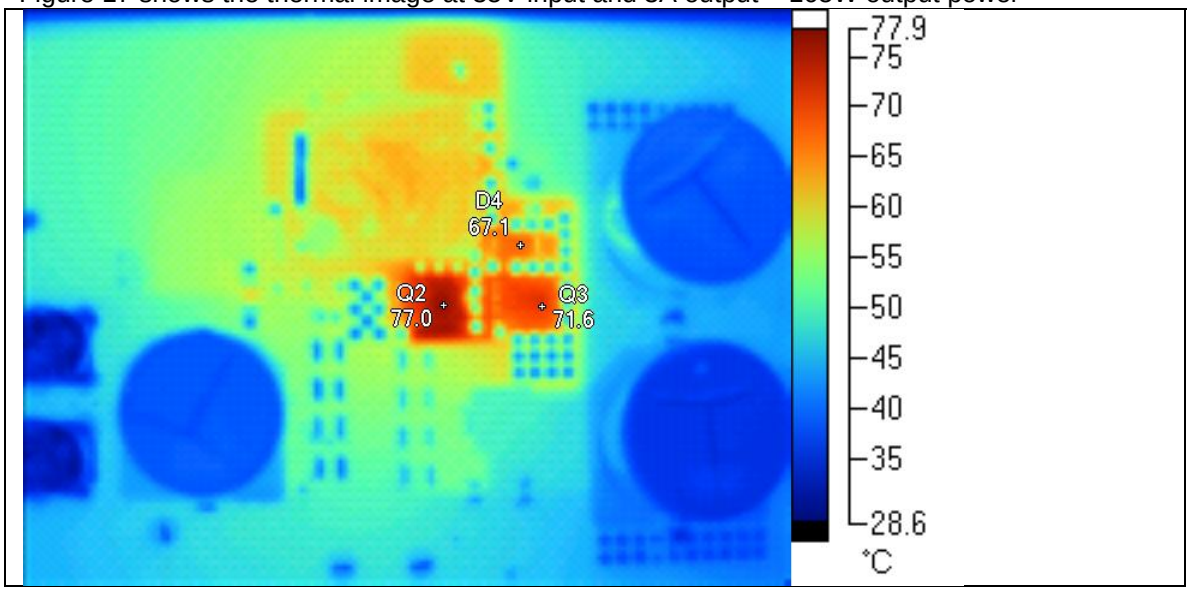


Figure 17

Name	Temperature
Q2	77.0°C
Q3	71.6°C
D4	67.1°C

Table 3

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