bq76200 high-voltage battery pack front-end charge/discharge high-side NFET driver

1 Features

- CHG and DSG high-side NMOS FET drivers for battery protection fast FET turn-on and turn-off times
- Pre-charge PFET driver (for current-limited pre-charge of significantly depleted cell-pack)
- Independent digital enable control for charging and discharging
- Minimal external components needed
- Scalable external capacitor-based charge pump to accommodate a different range of FETs in parallel
- High-voltage tolerant (100-V absolute maximum)
- Internal switch to enable pack-voltage sensing
- Common and separate charge and discharge path configuration support
- Designed to work directly with bq76940, bq76930, and bq76920 battery monitors
- Current consumption:
  - NORMAL mode: 40 µA
  - SHUTDOWN: < 10 µA maximum

2 Applications

- eBikes, eScooters, and eMotorcycles
- Energy storage systems and uninterruptible power supplies (UPS)
- Portable medical systems
- Wireless base-station battery systems
- Lead acid (PbA) replacement batteries
- 12-V to 48-V battery packs

3 Description

The bq76200 device is a low-power, high-side, N-channel system. A high-side protection avoids ground disconnection in the system and also allows continuous communication between the battery pack and host system. The device has additional P-Channel FET control to allow low-current pre-charge to a deeply depleted battery, and a PACK+ voltage monitor control for the host to sense the PACK+ voltage.

The independent enable inputs allow CHG and DSG FETs to be turned on and off separately, offering great implementation flexibility in battery systems.

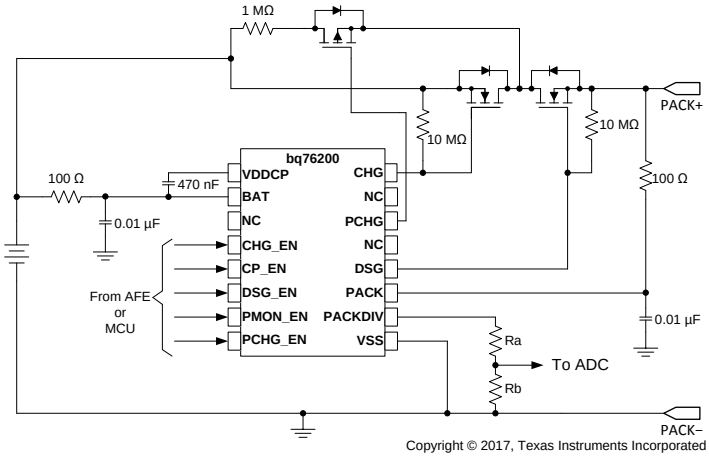
The bq76200 device can be used with a companion analog front end (AFE) device such as the bq76920/30/40 family, a 3-series to 15-series Cell Analog Front End Monitoring, and a host microcontroller or dedicated state-of-charge (SOC) tracking gas gauge device.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq76200	TSSOP (16)	5.00 × 4.40 × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Revision A (September 2018) to Revision B **Page**

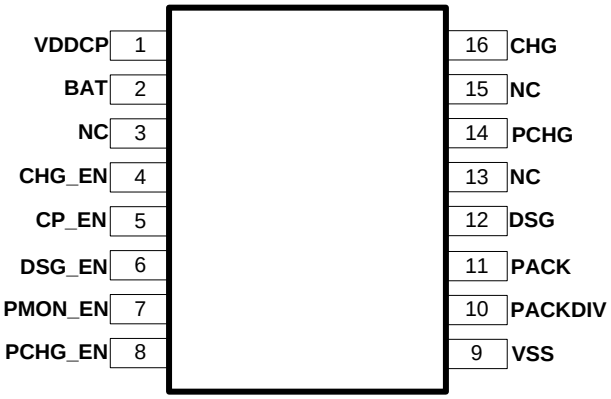
- Added application note references to *Related Documentation*, as well as to sections throughout the data sheet ... 21

Changes from Original (November 2015) to Revision A **Page**

- Changed the predischarge FET symbol in Figure 10 ... 14

5 Pin Configuration and Functions

PW Package
16-pin TSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.	I/O	
BAT	2	P	Top of battery stack
CHG(2)	16	O	Gate drive for charge FET
CHG_EN(3)	4	I	Charge FET enable
CP_EN(3)	5	I	Charge pump enable (internally logic OR'ed with CHG_EN and DSG_EN signals)
DSG(2)	12	O	Gate drive for discharge FET
DSG_EN(3)	6	I	Discharge FET enable
NC	3, 13, 15	—	No connect. Leave the pin floating
PACK	11	P	Analog input from PACK+ terminal
PACKDIV(2)	10	O	PACK voltage after internal switch (Connect to MCU ADC via resistor divider.)
PCHG(2)	14	O	Gate drive for precharge FET
PCHG_EN(3)	8	I	Precharge FET enable
PMON_EN(3)	7	I	Pack monitor enable (allows connection of internal switch between PACK and PACKDIV)
VDDCP	1	O	Charge pump output. Connect a capacitor to BAT pin. Do not load this pin.
VSS	9	P	Ground reference

(1) P = Power Connection, O = Digital Output, AI = Analog Input, I = Digital Input, I/OD = Digital Input/Output
(2) Leave the pin float if the function is not used.
(3) It is recommended to connect the pin to ground if the function is not used.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range, V_{IN}	BAT, PACK (both under charge pump disabled condition)	–0.3	100	V
	CHG_EN, DSG_EN, PCHG_EN, PMON_EN, CP_EN(2)	–0.3	15	V
Output voltage range, V_O	CHG, DSG, PCHG, PACKDIV, VDDCP	–0.3	100	V
T_{FUNC}	Functional Temperature	–40	110	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The enable inputs need to be current limited with the max current not exceeding 5 mA.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Typical values stated where T_A = 25°C and VBAT = 48.8 V, Min/Max values stated where T_A = –40°C to 85°C and BAT = 8 V to 75 V (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{BAT}	Battery cell input supply voltage range		8		75	V
V_{PACK}	Charger/Load voltage range		0		75	V
V_{IN}	Input voltage range	CHG_EN, DSG_EN, PCHG_EN, PMON_EN, CP_EN	0		14	V
C_{VDDCP}	Capacitor Between VDDCP and BAT			470		nF
T_{OPR}	Operating free-range temperature		–40		85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TSSOP (PW) 16 PINS	UNIT
$R_{\theta JA, High K}$	Junction-to-ambient thermal resistance	106.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	41.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Typical values stated at T_A = 25°C and $V_{(BAT)}$ = 48 V. MIN/MAX values stated with T_A = –40°C to 85°C and $V_{(BAT)}$ = 8 to 75 V unless otherwise noted.

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY AND LEAKAGE CURRENT						
$I_{(BAT)}$	NORMAL mode current(1)	$C_{(VDDCP)}$ = 470 nF, $V_{(BAT)}$ = 8V C_L = 10 nF		40	60	µA
		$C_{(VDDCP)}$ = 470 nF, $V_{(BAT)}$ ≥ 48V C_L = 10 nF		40	52	uA
Ishut	Sum of current into BAT and PACK pin	Shutdown Mode, PACK = 0 V, BAT = 8 V		6	9.5	µA
CHARGE PUMP						
$V_{(VDDCP)}$	Charge pump voltage	No Load, CP_EN = hi, $V_{(VDDCP)} – V_{(BAT)}$	9		14	V
t_{CPON}	Charge pump start up time from zero volt	$C_{(VDDCP)}$ = 470 nF, 10% to 90% of $V_{(VDDCP)}$		100		ms
INPUT ENABLE CONTROL SIGNALS						
V_{IL}	Digital low input level for CHG_EN, DSG_EN, PCHG_EN, CP_EN, PMON_EN				0.6	V
V_{IH}	Digital high input level for CHG_EN, DSG_EN, PCHG_EN, CP_EN, PMON_EN		1.2			V
R_{PD}	Internal Pull down	VIN = 5 V	0.6	1	4	MΩ
CHARGE FET DRIVER						
$V_{(CHGFETON)}$	CHG gate drive voltage (on)	C_L = 10 nF, CHG_EN = Hi, $V_{(BAT)}$ = $V_{(PACK)}$, $V_{(CHG)} – V_{(BAT)}$	9	12	14	V
$R_{(CHGFETON)}$	CHG FET driver on resistance	$V_{(VDDCP)} – V_{(BAT)}$ = 12 V, CHG_EN = Hi, $V_{(BAT)}$ = $V_{(PACK)}$		1.1		kΩ
$R_{(CHGFETOFF)}$	CHG FET driver off resistance	$V_{(VDDCP)} – V_{(BAT)}$ = 12 V, CHG_EN = Lo, $V_{(BAT)}$ = $V_{(PACK)}$		0.3		kΩ
DISCHARGE FET DRIVER						
$V_{(DSGFETON)}$	DSG gate drive voltage (on)	C_L = 10 nF, DSG_EN = Hi, $V_{(BAT)}$ = $V_{(PACK)}$, $V_{(DSG)} – V_{(PACK)}$	9	12	14	V
$R_{(DSGFETON)}$	DSG FET driver on resistance	$V_{(VDDCP)} – V_{(BAT)}$ = 12 V, DSG_EN = Hi, $V_{(BAT)}$ = $V_{(PACK)}$		3.5		kΩ
$R_{(DSGFETOFF)}$	DSG FET driver off resistance	$V_{(VDDCP)} – V_{(BAT)}$ = 12 V, DSG_EN = Lo, $V_{(BAT)}$ = $V_{(PACK)}$		1		kΩ
PRECHARGE FET DRIVER						
$V_{(PCHGFETON)}$	PCHG gate drive voltage (on)	$V_{(PACK)}$ > 17 V, $V_{(BAT)}$ < $V_{(PACK)}$, $V_{(PACK)} – V_{(PCHG)}$	5	12	14	V
PACK MONITOR (PACK_DIV)						
$R_{(PMONFET)}$	On resistance of internal FET (R between PACK and PACKDIV)	PMON_EN = hi	1.5	2.5	3.5	kΩ

(1) NORMAL mode is defined as CHG_EN = Hi, DSG_EN = Hi, CP_EN = Hi, PCHG_EN = Lo, PMON_EN = Lo. Current value is averaged out over time.

6.6 Timing Requirements

Parameter	Description	TEST CONDITION	MIN	TYP	MAX	UNIT
$t_{CHGFETON}$	CHG on rise time + propagation delay	C_L = 10 nF, (20% of CHG_EN from Lo to Hi) to (80% of $V_{(CHGFETON)}$), CP_EN = Hi, (CP is already on)		27	45	µs
$t_{CHGFETOFF}$	CHG off fall time + propagation delay	C_L= 10 nF, (80% of CHG_EN from Hi to Lo) to (20% of $V_{(CHGFETON)}$) , CHG_EN = Hi to Lo		7	20	µs
$t_{PROP\ \_CHG}$	CHG EN to CHG output	C_L= 10 nF, CP_EN = Hi, (CP is already on), see timing diagram		0.5		µs
$t_{DSGFETON}$	DSG on rise time + propagation delay	C_L = 10 nF, (20% of DSG_EN from Lo to Hi) to (80% of $V_{(DSGFETON)}$), CP_EN = Hi, (CP is already on)		24	50	µs
$t_{DSGFETOFF}$	DSG off fall time + propagation delay	C_L = 10 nF, (80% of DSG_EN from Hi to Lo) to (20% of $V_{(DSGFETON)}$)		7	20	µs
t_{PROP_DSG}	DSG EN to DSG output propagation delay	C_L= 10 nF, CP_EN = Hi, (CP already on), see timing Diagram		0.5		µs
$t_{PCHGOFF}$	PCHG turn off time + propagation delay	C_L = 1 nF, (20% of PCHG_EN from Hi to Lo) to (80% of $V_{PCHGFETON}$)		30	60	µs
t_{PCHGON}	PCHG turn on time + propagation delay	C_L = 1 nF, (80% of PCHG_EN from Lo to Hi) to (20% of $V_{(PCHGFETON)}$)		34	55	µs
t_{PROP_PCHG}	PCH_EN to PCHG propagation delay	C_L = 1 nF		0.5		µs
t_{PROP_PMON}	PMON_EN and PACKDIV = PACK propagation delay			0.5		µs

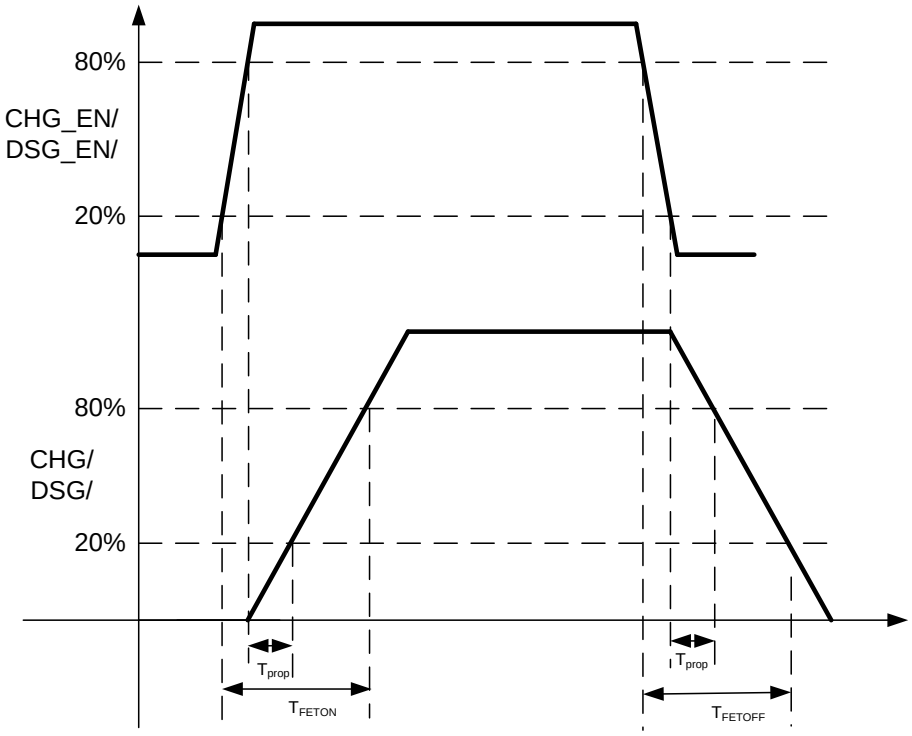


Figure 1. Timing Characteristics - (CP assumed to be already On)

6.7 Typical Characteristics

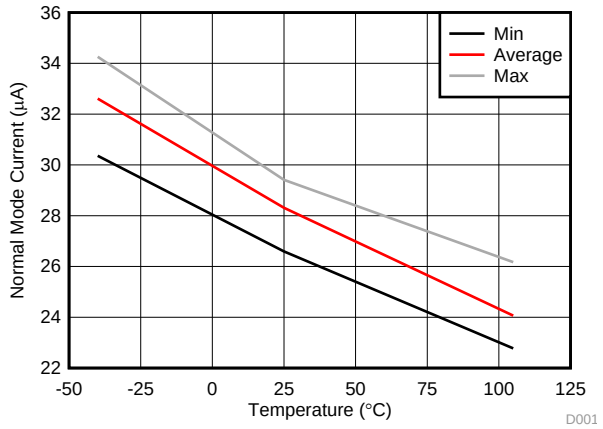


Figure 2. Normal Mode Current Vs Battery

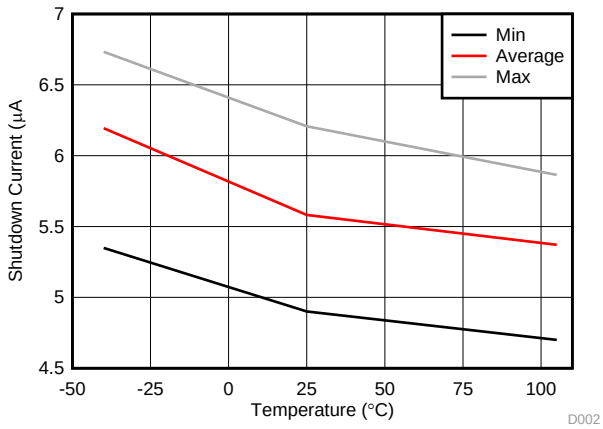


Figure 3. Shutdown Mode Current vs Battery

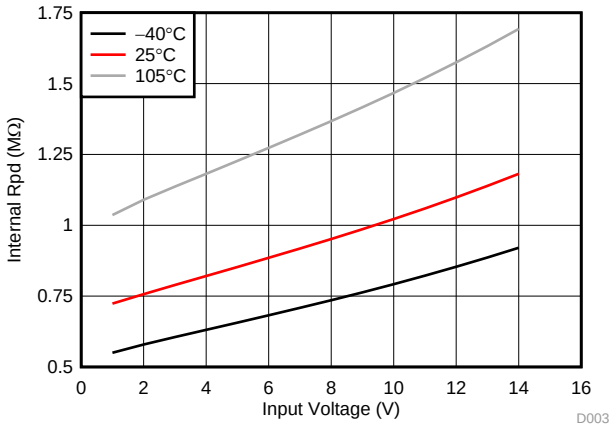


Figure 4. Input Pin Voltage for Internal Pull-Down Resistance (Rpd)

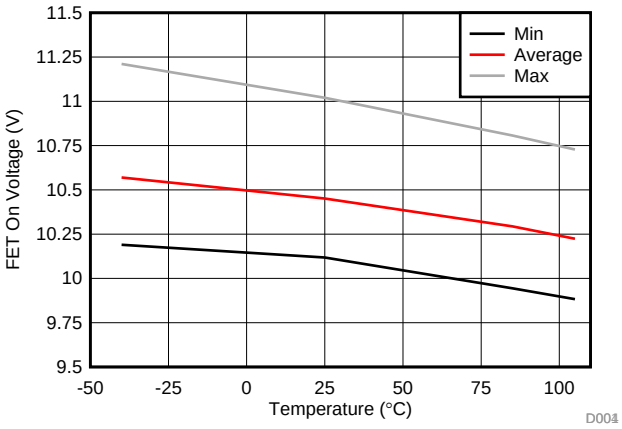


Figure 5. CHG/DSG FET On Voltage vs Temperature

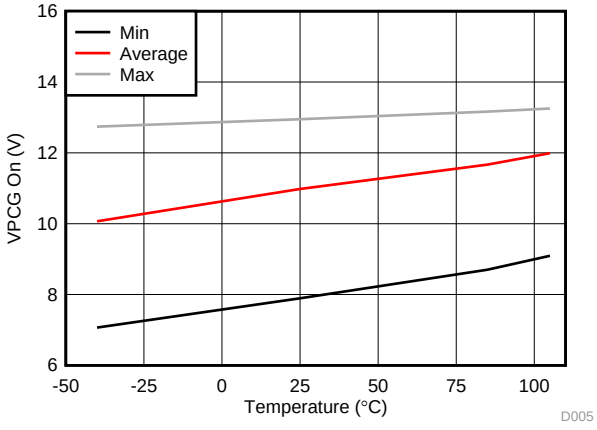


Figure 6. PCHG On Voltage vs Temperature

7 Detailed Description

7.1 Overview

The bq76200 device is a low-power, high-side, N-Channel MOSFET driver for battery-pack protection systems, allowing a low-side battery-protection system to be implemented into a high-side protection system.

High-side charge/discharge FETs offer a huge advantage versus their low-side counterparts; with high-side implementation, a system-side processor can always communicate with the monitor or micro-controller (MCU) within the battery pack, regardless of whether the FETs are on or off — this is not easily supported in a low-side switching architecture due to the lack of a shared ground reference. One key benefit of an ever-present communication link is the ability to read out critical pack parameters despite safety faults, thereby enabling the system to assess pack conditions before determining if normal operation may resume.

The device allows independent control on charging and discharge via the digital enable pins. The device has integrated charge pump which is enabled by the CP_EN pin. The enable inputs, CHG_EN, DSG_EN, and PCHG_EN control the CHG, DSG, and PCHG FET gate drivers, respectively. The enable inputs can be connected to low-side FET driver outputs of an Analog Front End (AFE) such as Texas Instruments bq769x0 series, a general purpose microcontroller, or dedicated battery pack controller such as the bq783xx series.

In normal mode, the AFE or MCU enables the CHG_EN and DSG_EN, turning on the CHG and DSG FET drivers to connect the battery power to the PACK+ terminal. When a fault is detected by the AFE or the microcontroller, it can disable the CHG_EN and/or DSG_EN to open the charge or discharge path for protection. Note that when either the CHG_EN or DSG_EN is enabled, the charge pump will be automatically enabled even if the CP_EN is in the disable state. It is recommended to enable the charge pump via CP_EN pin during system start-up to avoid adding the t_{CPON} time into the FET switching time during normal operation.

A lower charging current is usually applied to a deeply depleted battery pack. The bq76200 PCHG_EN input provides an option to implement a P-Channel MOSFET precharge path (current-limited path) in the battery pack.

An AFE usually provides individual cell voltages and/or battery stack voltage measurements, but it is not necessary to have PACK+ voltage measurement. The bq76200 PMON_EN pin, when enabled, will connect the PACK+ voltage onto the PACKDIV pin, which is connected to an external resistor divider to scale down the PACK+ voltage. This scaled down PACK+ voltage can be connected to a microcontroller's ADC input for voltage measurement. The system can use this information for charger detection or to implement advanced charging control.

For safety purposes, all the enable inputs are internally pulled down. If the AFE or microcontroller is turned off, or if the PCB trace is damaged, the internal pull down of the enable inputs will keep CHG, DSG, PCHG in an off state and the PACK+ voltage does not switch onto the PACKDIV pin.

7.2 Functional Block Diagram

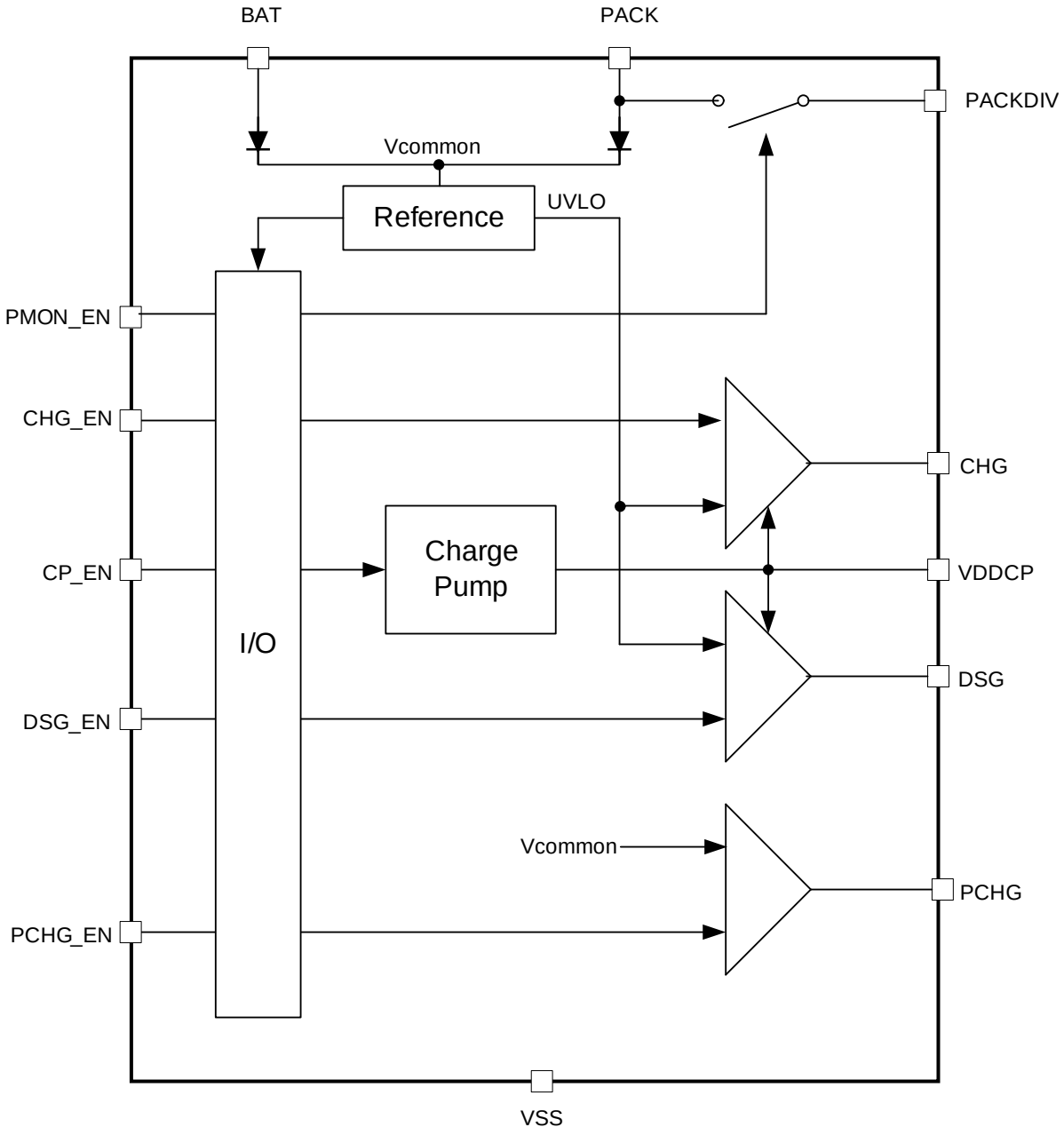


Figure 7. Functional Block Diagram

7.3 Feature Description

7.3.1 Charge Pump Control

The bq76200 device has an integrated charge pump. A minimum of 470-nF capacitor is required on the $V_{(VDDCP)}$ pin to the BAT pin to ensure proper function of the charge pump. If the $V_{(VDDCP)}$ capacitor is disconnected, a residual voltage could reside at the CHG and/or DSG output if CHG_EN and/or DSG_EN are enabled. Such a fault condition can put the external FETs in high Rdson state and result in FET damage.

Feature Description (continued)

The $V_{(VDDCP)}$ capacitor can be scaled up to support more FETs in parallel (such as high-total FET-gate capacitance) than the value specified in the electrical characteristics table. A higher VDDCP capacitance results in longer t_{CPON} time. See the *Application Information* section for more information. Note that probing the VDDCP pin may increase the loading on the charge pump and result in lower measurement value than the $V_{(VDDCP)}$ specification. Using higher impedance probe can reduce such effect on the measurement.

The charge pump is controlled by CP_EN and also OR'ed with the CHG_EN and DSG_EN inputs. This means by enabling CHG_EN or DSG_EN alone, the charge pump will automatically turn on even if the CP_EN pin is disabled. The PCHG_EN controls the PCHG pin, which is a P-channel FET driver and does not require the function of the charge pump. The charge pump is turned off by default. When CP_EN is high, the charge pump turns on regardless of the status of the CHG_EN and DSG_EN inputs.

When CP_EN is enabled, the charge pump voltage starts to ramp up. Once the voltage is above an internal UVLO level, about 9-V typical above V_{BAT}, the charge pump is considered on. The charge pump voltage should continuously ramp to the $V_{(VDDCP)}$ level. If the CHG_EN and/or DSG_EN is enabled, the CHG and/or DSG voltage will starts to turn on after the charge pump voltage is above the UVLO level, and ramp up along the charge pump voltage to the $V_{(VDDCP)}$ level. Otherwise, the CHG and DSG do not turn on if the charge pump voltage fails to ramp up above UVLO. For example, if the $C_{(VDDCP)}$ is not scaled properly to support the number of FETs in parallel, the heavy loading would prevent the charge pump to ramp up above UVLO. CHG and DSG would not be turned on in this case.

When CHG_EN and/or DSG_EN is enabled after the charge pump is fully turned on, the CHG_EN-enable to CHG-on delay (or DSG_EN-enable to DSG-on delay) is simply the sum of (tprop + FET rise time). A system configuration example for this scenario will be connecting the CP_EN to the host MCU, enable CP_EN at system start-up and keep the CP_EN enabled during normal operation. This is the recommended configuration, because the charge pump ramp-up time, t_{CPON}, becomes part of the system start-up time and does not add onto the FET switch delay during normal operation.

If CP_EN is not used (it is highly recommended to connect the CP_EN to ground), the charge pump on- and off-state is controlled by CHG_EN or DSG_EN. The CHG or DSG output will only be on after the charge-pump voltage is ramped up above UVLO. This means the CHG_EN-enable to CHG-on delay (or DSG_EN-enable to DSG-on delay) will be (t_{CPON} + tprop + FET rise time).

The charge pump is turned off when CP_EN AND CHG_EN AND DSG_EN signals are all low. The charge pump is not actively driven low and the voltage on the $V_{(VDDCP)}$ capacitor bleeds off passively. If any of the CP_EN, CHG_EN, or DSG_EN signals is switched high again while the $V_{(VDDCP)}$ capacitor is still bleeding off its charge, the charge pump start up time, t_{CPON}, will be shorter.

7.3.2 Pin Enable Controls

The bq76200 has four digital enable inputs that control the state of associated output signals as defined in the following table. The V_{IH} and VIL levels of these enable pins are low enough to work with most MCUs. At the same times, the pins have high enough tolerant to allow direct control from an AFE FET driver. This gives system maker a flexible option to architect the battery pack configuration.

INPUT PIN	ASSOCIATED OUTPUT PIN	DESCRIPTION
CHG_EN	CHG	Charge FET control
DSG_EN	DSG	Discharge FET control
PCHG_EN	PCHG	Precharge FET control
PMON_EN	PACKDIV	Pack monitor control

7.3.2.1 External Control of CHG and DSG Output Drivers

The CHG_EN and DSG_EN pins provide direct control of the CHG and DSG FET driver. Table 1 summarizes the CHG and DSG statute with respect to the CP_EN, CHG_EN and DSG_EN inputs.

Table 1. CHG and DSG with Respect to CP_EN, CHG_EN, and DSG_EN

CP_EN	CHG_EN	DSG_EN	CHARGE PUMP	CHG	DSG
Lo (default)	Lo (default)	Lo (default)	OFF (default)	OFF (default)	OFF (default)
Lo	Lo	Hi	ON	OFF	ON
Lo	Hi	Lo	ON	ON	OFF
Lo	Hi	Hi	ON	ON	ON
Hi	Lo	Lo	ON	OFF	OFF
Hi	Lo	Hi	ON	OFF	ON
Hi	Hi	Lo	ON	ON	OFF
Hi	Hi	Hi	ON	ON	ON

7.3.2.2 External Control of PCHG Output Driver

The PCHG output driver is designed to drive a P-channel FET and is controlled by the PCHG_EN pin. The PCHG driver provides an option to implement a separate charging path with a P-channel FET to charge the battery when the cells are deeply depleted. A resistor should be added in series to the P-channel precharge FET to limit the charging current. A precharge current is usually at or less than 1/20 of the normal charge current if the charger does not support lower current precharge. Refer to the battery cell specification from the cell manufacturer charging for the appropriate current limit.

PCHG_EN	PCHG
Lo (default)	OFF (default)
Hi	ON

7.3.2.3 Pack Monitor Enable

The bq76200 device provides an internal-switch control to post the PACK+ voltage on to the PACKDIV pin. A resistor divider can be connected to the PACKDIV pin externally to divide down the PACK+ voltage into a measurable range of an MCU. The PMON_EN controls the internal switch between PACK pin and PACKDIV pin. The internal switch has an on resistance of $R_{(PMONFET)}$. The external resistor divider for PACKDIV pin should be selected to avoid exceeding the absolute maximum of the PACKDIV pin and should also keep the loading current < 500 µA. If this function is not used, the PACKDIV pin should leave floating. To reduce power consumption, the PMON_EN should be enabled only when PACK+ voltage measurement is needed.

PMON_EN	PACKDIV
Lo (default)	DISABLED (default)
Hi	ENABLED

7.4 Device Functional Modes

- In NORMAL mode, the bq76200 charge pump is turned on by enabling either CP_EN, CHG_EN, or DSG_EN. In this mode, typically the CHG and DSG outputs are driven to $V_{(BAT)} + V_{(VDDCP)}$.
- In SHUTDOWN mode, the bq76200 is completely powered down. When CHG_EN, DSG_EN, and CP_EN are driven low, the device enters SHUTDOWN mode, and the outputs are driven low.

DEVICE MODES	CONDITION
NORMAL	CHG_EN = Hi, DSG_EN = Hi, CP_EN = Hi, PCHG_EN = don't care, PMON_EN = don't care
SHUTDOWN	CHG_EN = Lo, DSG_EN = Lo, CP_EN = Lo, PCHG_EN = Lo, PMON_EN = Lo

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq76200 device is a high-side NMOS FET driver with integrated charge pump. The device can convert a low-side battery protection system into a high-side protection system, allowing the battery monitor device or battery MCU to always maintain communication to the host system regardless if the protection FETs are on or off. The device provides independent enables to control charge and discharge of a battery pack.

The following section highlights several recommended implementations when using this device. See the *FET Configurations for the bq76200 High-Side N-Channel FET Driver Application Note* (SLVA729).

8.1.1 Recommended System Implementation

8.1.1.1 bq76200 Slave Device

The bq76200 is a FET driver. It controls the output pins (CHG, DSG, PCHG, and PACKDIV) according to the input pin (CHG_EN, DSG_EN, PCHG_EN, CP_EN, and PMON_EN) status. The device does not validate if the inputs should or should not be turned on or off. For example, if both CHG_EN and PCHG_EN are enabled, bq76200 will turn on both CHG and PCHG simultaneously, enabling two charging paths to the system. The system designer should avoid undesirable enable combinations via the schematic, AFE, or host MCU implementation.

8.1.1.2 Flexible Control via AFE or via MCU

The bq76200 device has simple-logic input pins (CHG_EN, DSG_EN, PCHG_EN, CP_EN, and PMON_EN) that can accept a control signal from any MCU I/O. At the same time, the input pins are designed to tolerate high voltage signal such as the FET driver output from an AFE. This flexibility allows a mix of control input driving from AFE and/or MCU to optimize the system design.

For example, it is recommended to control the CP_EN pin via MCU which the system can turn on the charge pump at system start-up, excluding the extra FET delay due to charge pump voltage ramping. On the other hand, the CHG_EN and DSG_EN can be driven by the AFE FET driver output, especially if the AFE has hardware protection features (such as the bq76920/30/40 family), to optimize the FET reaction time.

All the input pins have internal pull-down resistor. The outputs are default to be off if any of the input pins are at high-Z state.

8.1.1.3 Scalable VDDCP Capacitor to Support Multiple FETs in Parallel

The bq76200 requires a minimum 470-nF capacitor to be connected between the VDDCP pin and BAT pin in order to turn on the integrated charge pump. The Electrical Characteristics Specification of this document specified the device performance based on 10 nF loading with 470-nF VDDCP capacitor. The loading capacitance varies with FET choices, number of FETs in use, and in parallel and simultaneous switching versus sequential switching of CHG and DSG FET.

The more FETs that are in parallel, the higher the loading capacitance. Similarly, simultaneously switching of the CHG and DSG FET loads down the charge pump more than sequentially switching both FETs. Eventually, the loading capacitance can exceed the supported range of a 470-nF VDDCP capacitor. A > 470-nF VDDCP capacitor can be used to support higher-loading capacitance.

Application Information (continued)

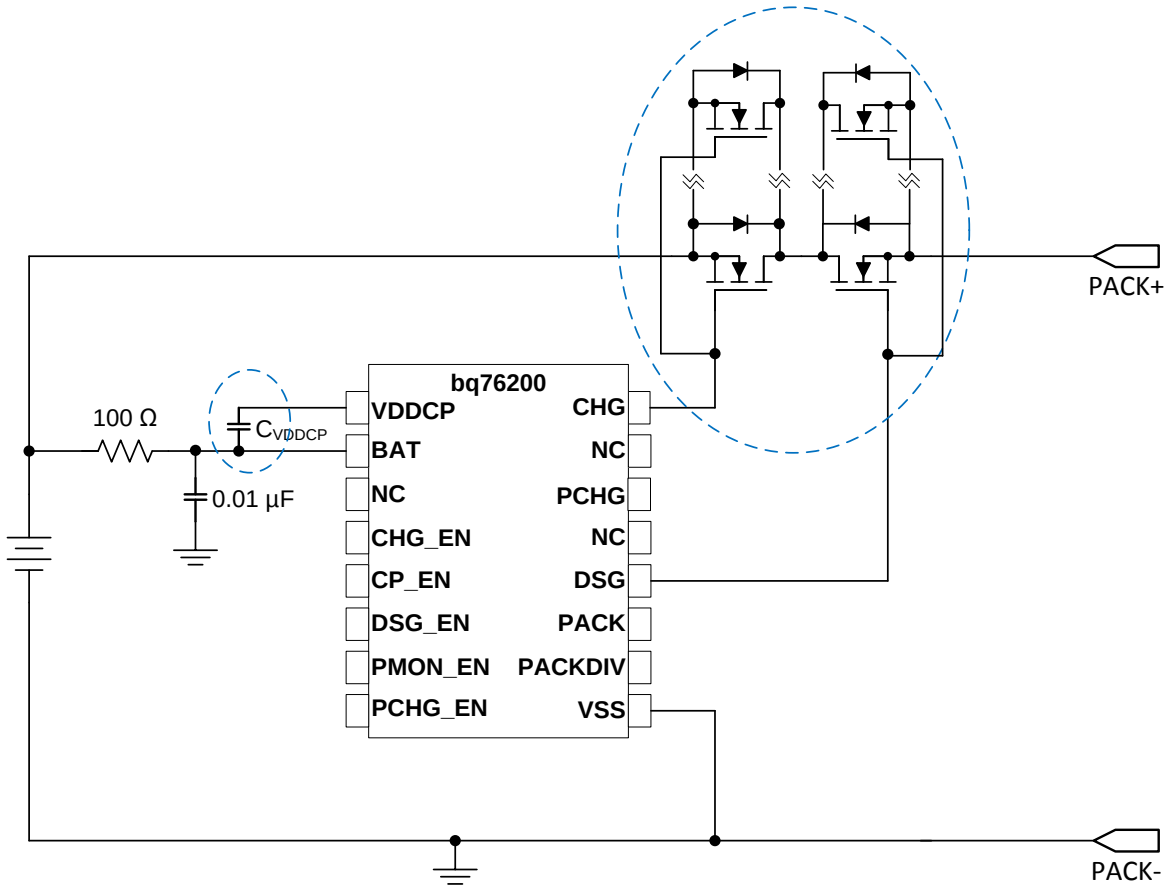


Figure 8. Scale C_{VDDCP} to Support Multiple FETs in Parallel (Partial Schematic Shown)

Based on test results, 470-nF VDDCP capacitor can support up to approximately 30-nF loading capacitance. Using a 470-nF/20-nF ratio (to include some design margin), a 2.1-µF VCCDP capacitor can support up to ~90-nF loading capacitance. Note that a larger VDDCP capacitor increases the charge pump start up time; a higher loading capacitance increases the FET on and off time. System designers should test across the operation range to ensure the design margin and system performance. Refer to the *FET Configurations for the bq76200 High-Side N-Channel FET Driver Application Note* (SLVA729) for more test results.

Also notice that any damage or disconnection of the VDDCP capacitor during operation can leave a residual voltage on the FET driver output if the inputs are enabled. This can result in putting the external FETs in a high-Rdson state and cause FET damage.

8.1.1.4 Precharge and Predischarge Support

For a deeply depleted battery pack, a much lower charging current, for example, a C/10 rate, is usually used to precharge the battery cells. This allows the passivating layer of the cell to be recovered slowly (the passivating layer might be dissolved in the deep discharge state).

The bq76200 has a PCHG output to drive an external P-channel FET to support battery precharge. In this scenario, the external P-channel FET is placed in parallel with the CHG FET and a power resistor can be connected in series of the P-channel FET to limit the charging current during the precharge state. The MCU can be used to control the PCHG_EN pin to determine the entry and exit of the precharge mode.

Application Information (continued)

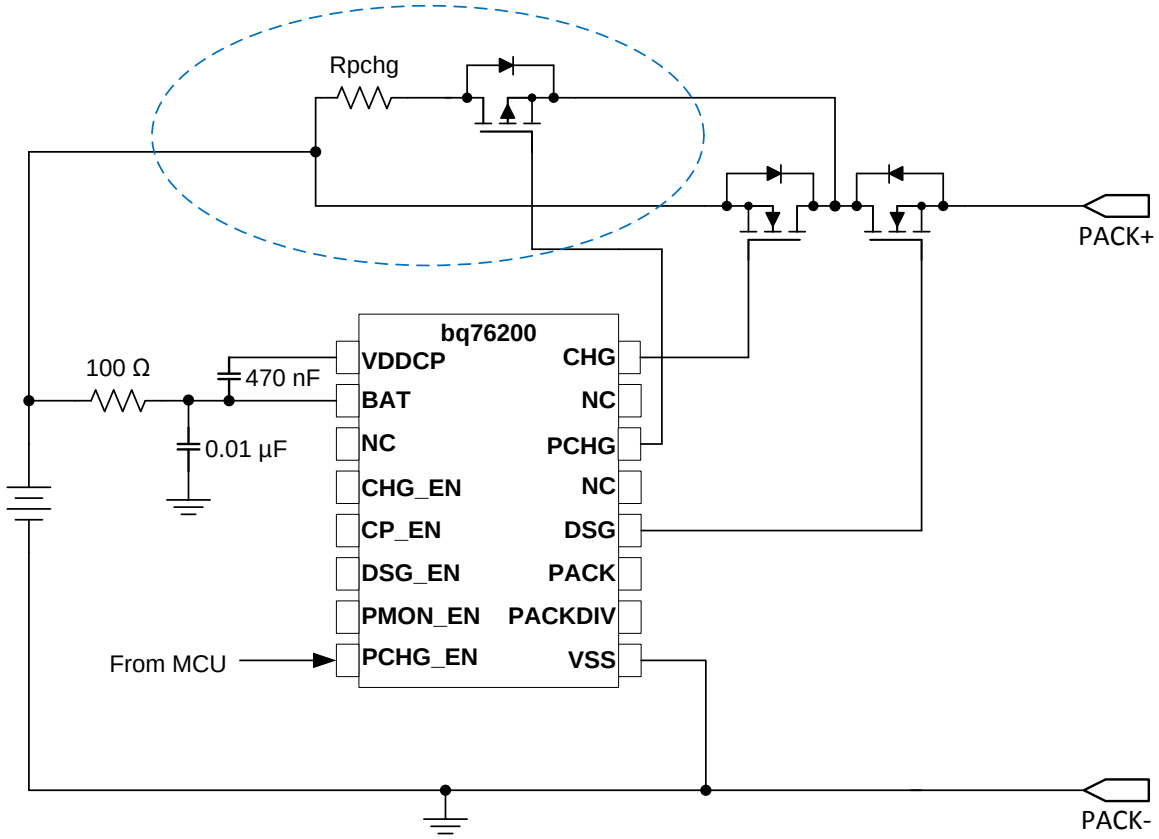


Figure 9. P-Channel FET in Parallel with CHG FET for Precharging (Partial Schematic Shown)

Alternatively, the CHG pin can also be used to precharge a battery pack given if the charging current is controlled by the system (that is, does not require external component to limit the charging current such as a smart charger) and the battery stack voltage is higher than minimum operation voltage of the bq76200 (that is, the charge pump can start to turn on the CHG FET). PCHG should leave floating if it is not used in the application.

The PCHG output can be used to predischarge a high-capacitive system. For example, a load removal can be one of the recovery requirements after a discharge related fault has been detected. In a high-capacitive system, the residual voltage at the system side can take a significant time to bleed off. This results in an additional delay in fault recovery. The PCHG output can be used to control an external P-channel FET placed in parallel with the DSG FET to predischarge the residual voltage in order to speed up the fault recovery process.

Application Information (continued)

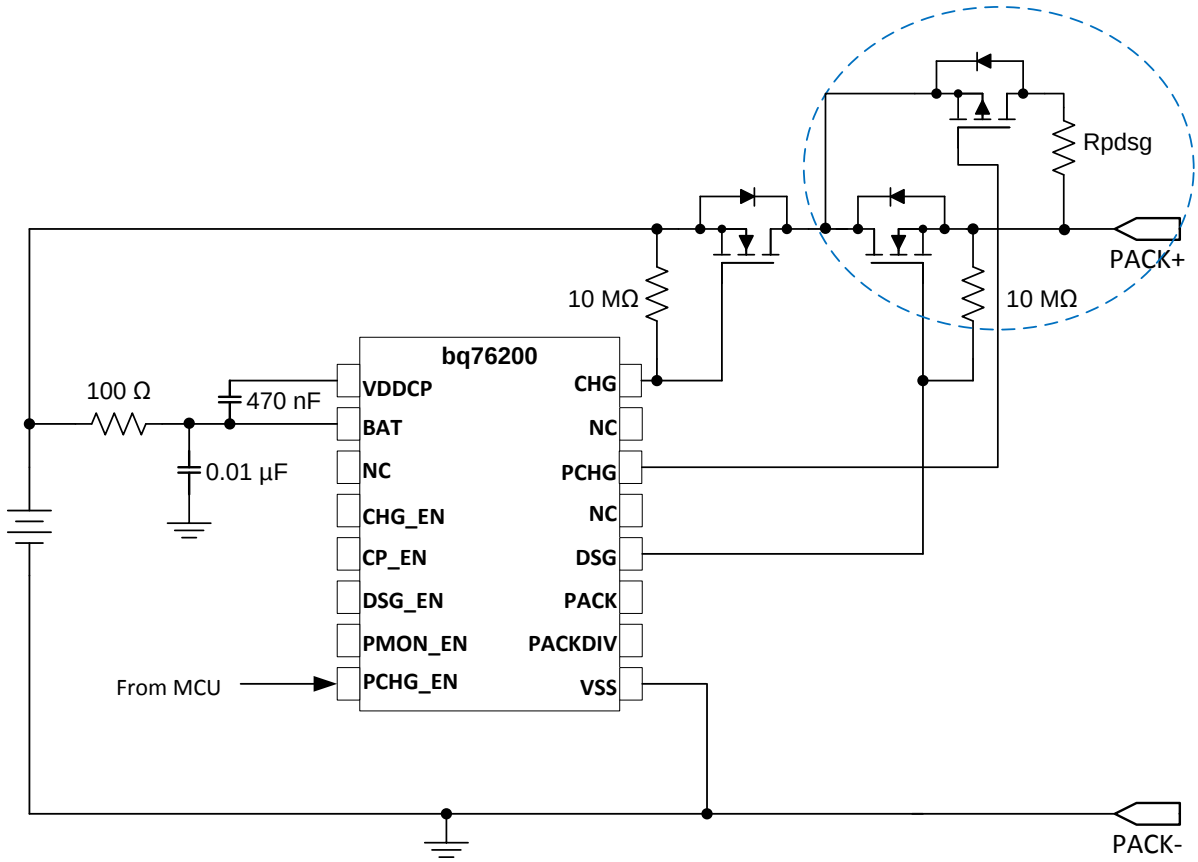


Figure 10. P-Channel FET in Parallel with DSG FET for Predischarging (Partial Schematic Shown)

8.1.1.5 Optional External Gate Resistor

The CHG and DSG have certain internal on and off resistance. However, an optional external gate resistor can be added to CHG and/or DSG FET to slow down the FET on and off timing.

8.1.1.6 Separate Charge and Discharge paths

In some systems, the charging current might be significantly lower than the discharge current. In such systems, the system designer may prefer to implement a separate charge and discharge paths in which the number of FET in parallel for charge and discharge can be different to reduce to BOM cost.

Application Information (continued)

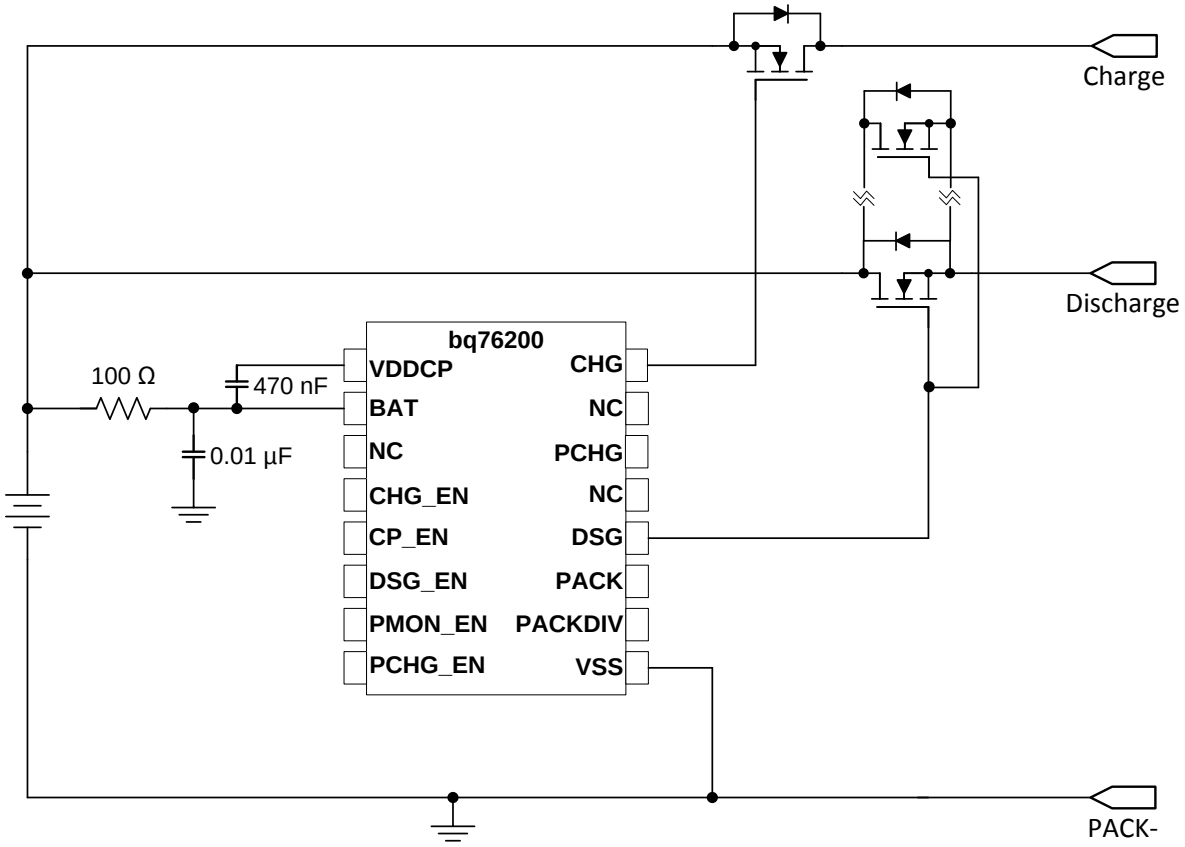
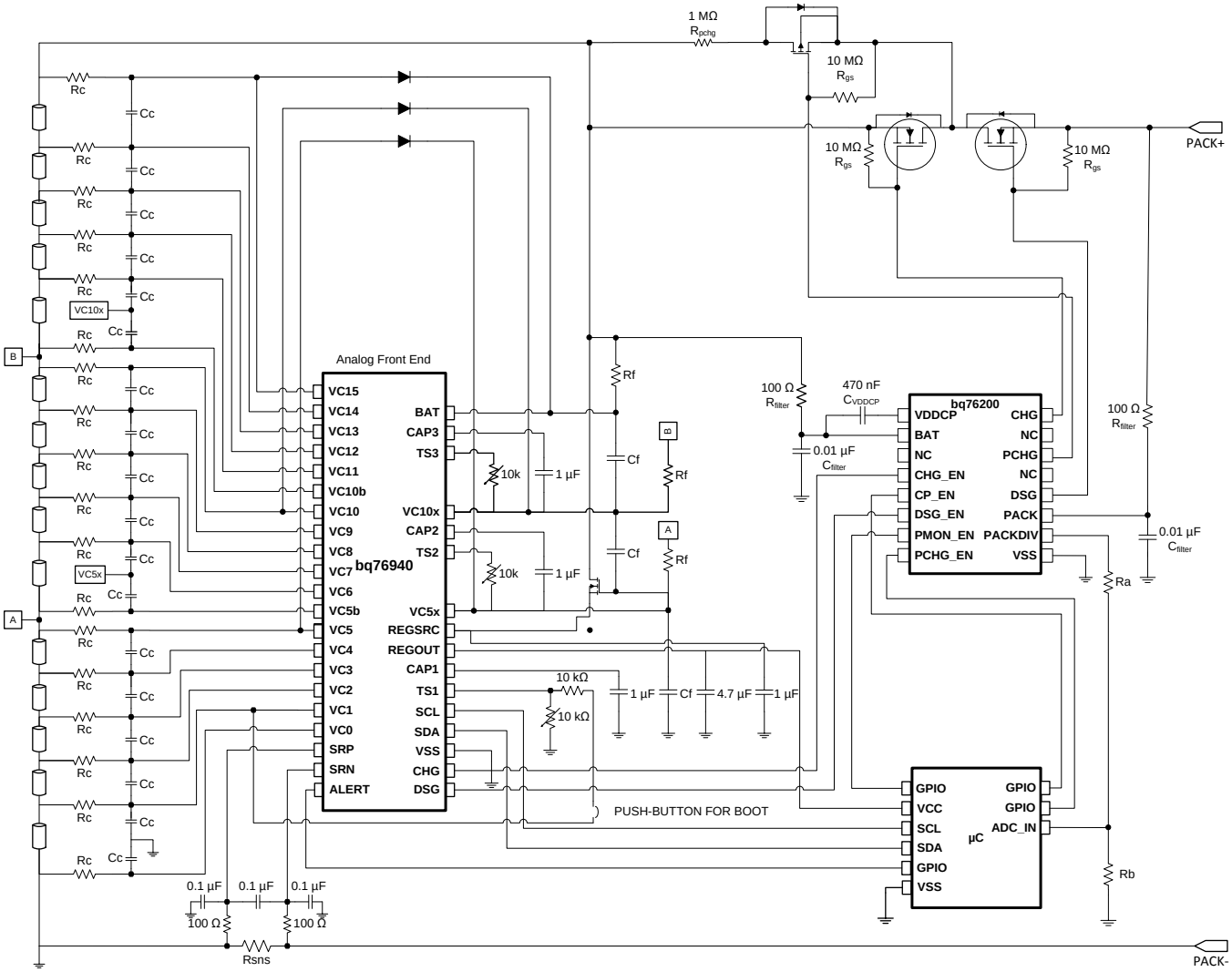


Figure 11. Separate Charge and Discharge Paths (Partial Schematic Shown)

8.2 Typical Applications



8.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

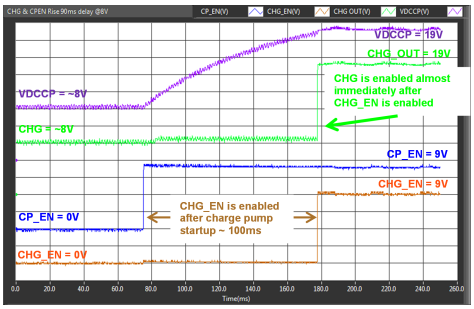
Table 2. Design Parameters

PARAMETER	EXTERNAL COMPONENT	NOTE
BAT and PACK Filters	Rfilter and Cfilter	Recommended to use 100 Ω and 0.01 µF
VDDCP capacitor	C_{VDDCP}	A minimum of 470 µF is required. A higher value can be used to support higher-loading capacitance. See the Recommended Implementation and the *FET Configurations for the bq76200 High-Side N-Channel FET Driver Application Note* (SLVA729).
PACKDIV resistor divider	Ra and Rb	Based on the max PACK voltage of the application, calculate the total value of (Ra + Rb) that can keep the PACKDIV current below 500 µA.
CHG, DSG, PCHG gate-source resistor	Rgs	Recommended to use 10 MΩ. A different Rgs value may change the loading level of the charge pump. System designer should perform thorough system testing if a different Rgs is used.

8.2.2 Detailed Design Procedure

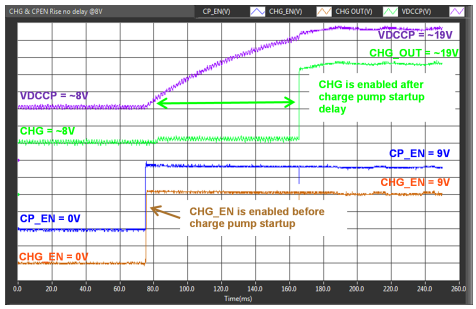
1. Determine if CP_EN pin will be driven by MCU. It is highly recommended to use CP_EN to turn on the charge pump at system start-up. However, it is not a must to operate the bq76200 to switch on CHG and DSG pins. System designer should ensure the FET's turn on time is acceptable during normal operation if CP_EN is not enabled at system startup.
2. Select the correct VDDCP capacitance. Scaling up the VDDCP capacitance allows support for a higher number of FETs in parallel. This test result of various parallel FETs versus VDDCP capacitance in the bq76200 application is for general reference only. System designer should always validate their design tolerant across operation temperature range.
3. If the PMON_EN is used, the PACKDIV resistor divider, Ra and Rb, must be selected to satisfy (Ra+Rb) < 500 µA, AND [Rb/(Ra + Rb)] < (max ADC input range)/(max PACK+ voltage). For example, In a 48V system, if the max charger voltage is 50.4 V and a MCU's max ADC input is 3 V. To meet both (Ra + Rb) < 500 µA, AND [Rb/(Ra + Rb)] < (3 V/50.4 V) requirements, the Ra value might be 100 kΩ or less and Rb value might be 6 KΩ or less.
4. Follow the application schematic (see *Typical Applications*) to connect the device.

8.2.3 Application Curves



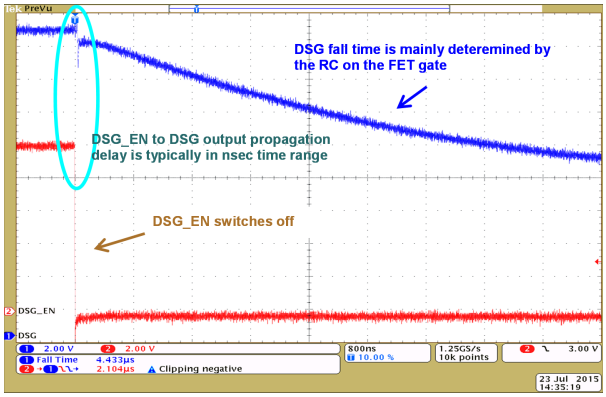
CHG output reacts to the CHG_EN signal immediately. Similar behavior applies to the DSG pin.

Figure 12. CHG_EN Switched On After Charger Pump Turns On and Is Stable



CHG output reacts to the CHG_EN signal after charge pump startup delay. Similar behavior applies to the DSG pin.

Figure 13. CHG_EN Enabled Before Charge Pump is Turned On



With 10-nF loading and no Rgs on DSG output. Note the time scale was 800 ns/div; thus, the DSG waveform above is basically the DSG FET fall time.

Figure 14. DSG_EN to DSG Output Propagation Delay

9 Power Supply Recommendations

The maximum recommended operation voltage on the BAT and PACK pins is 75 V. The charge pump, when it turns on, will add 14 V maximum voltage on top of the BAT or PACK voltage to the device, pushing the total device voltage to approximately 89 V.

The bq76200 has high voltage (100 V) tolerant pins, but system designer should take into account the worse-case transient voltage and the maximum charge pump on voltage to determine the maximum voltage applying to BAT and PACK pins.

10 Layout

10.1 Layout Guidelines

For the following procedure, see Figure 15 and Figure 16.

1. Place C_{VDDCP} capacitor close to the device.
2. Place BAT and PACK RC filters close to the device.
3. Generally, a typical system using an AFE, MCU, and bq76200 usually have a high-current ground trace/plane and low-current ground plane in the PCB layout. If so, the bq76200 ground should be connected to the low-current ground plane of the PCB layout to remove noise affecting the ENABLE signals.

10.2 Layout Example

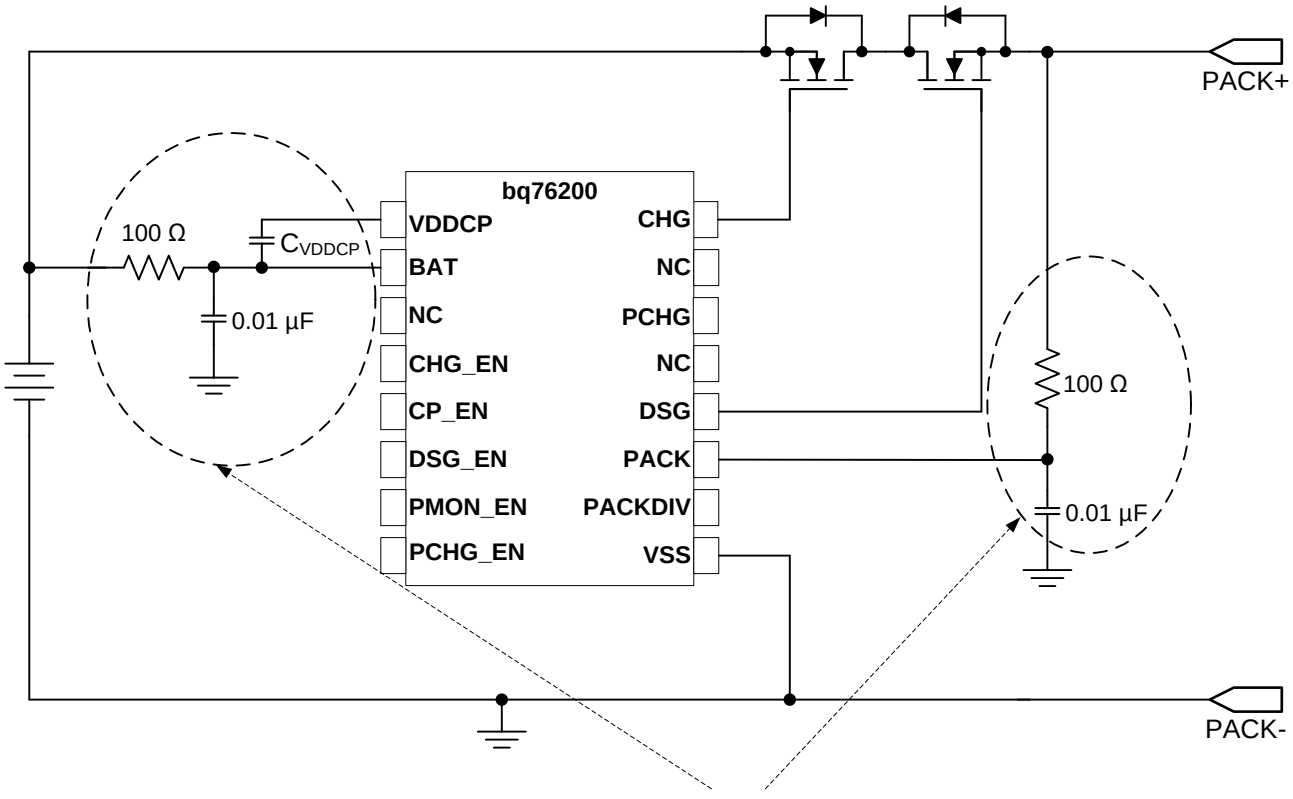


Figure 15. Place C_{VDDCP} and Filter Components Close to Device

Layout Example (continued)

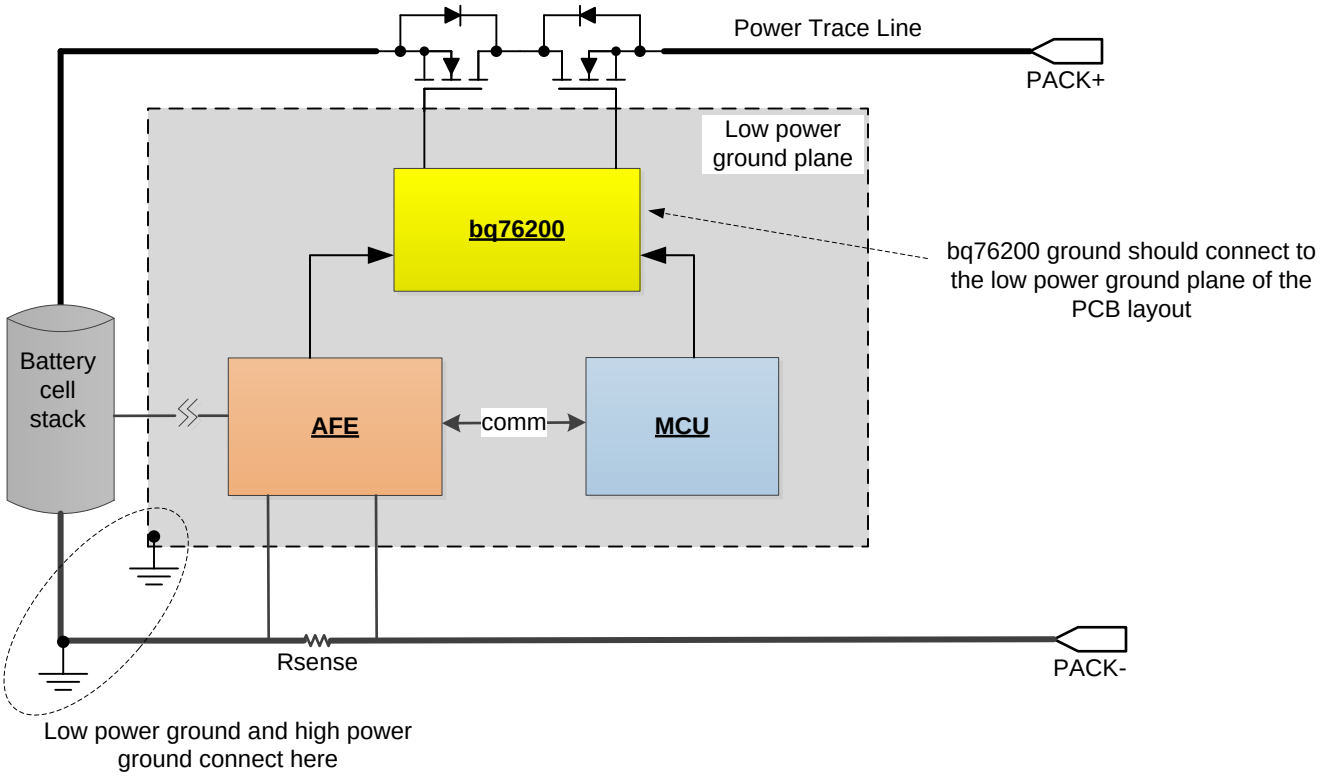


Figure 16. Connect bq76200 to Low Power Ground Plane on PCB Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *bq76200 Reverse Voltage Considerations Application Note* (SLUA796).
- *FET Configurations for the bq76200 High-Side N-Channel FET Driver Application Note* (SLVA729)
- *Minimizing Shutdown Current of the bq76200 Application Note* (SLUA795)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ76200PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7620B	Samples
BQ76200PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BQ7620B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

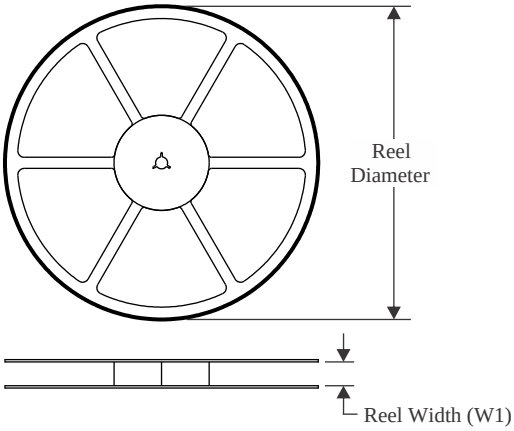
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

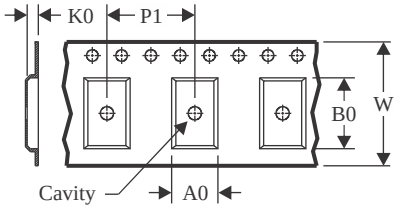
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

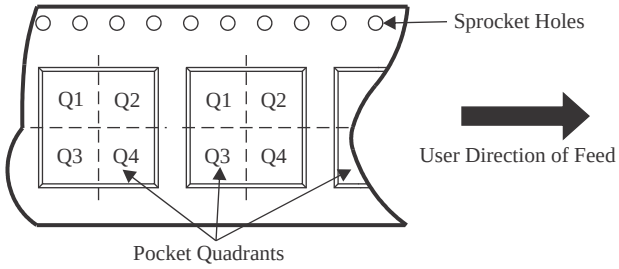


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

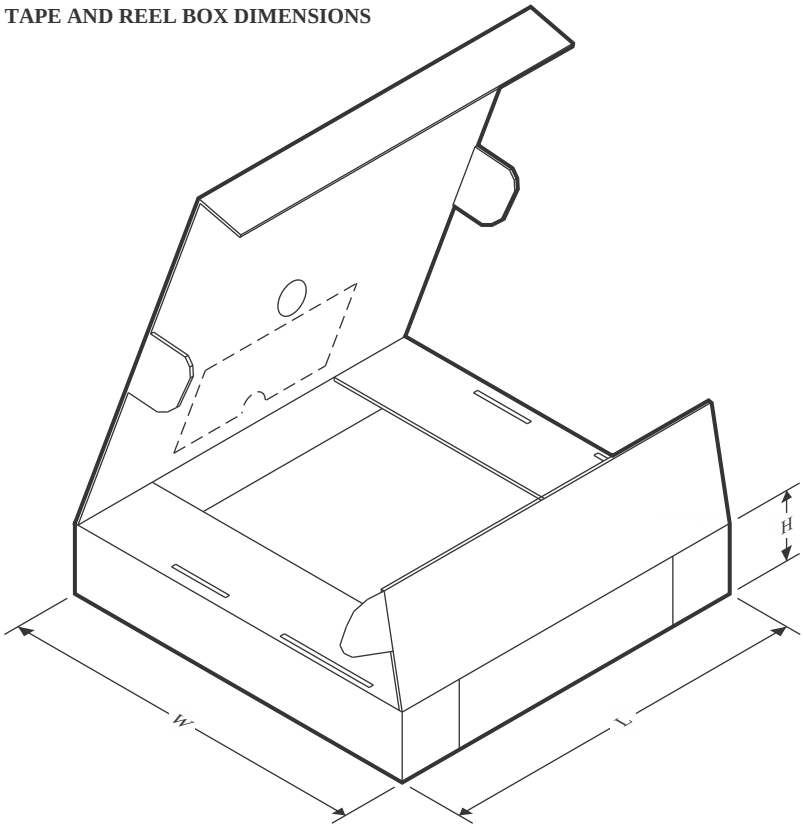
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ76200PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

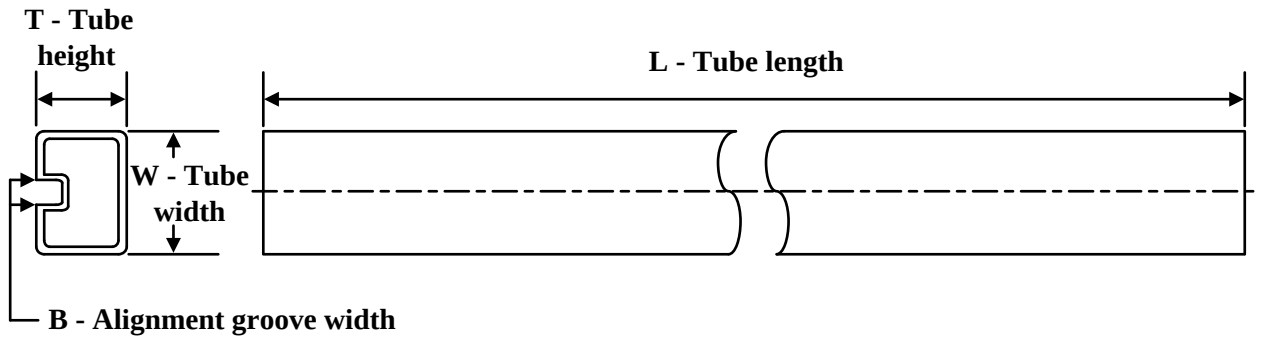
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ76200PWR	TSSOP	PW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

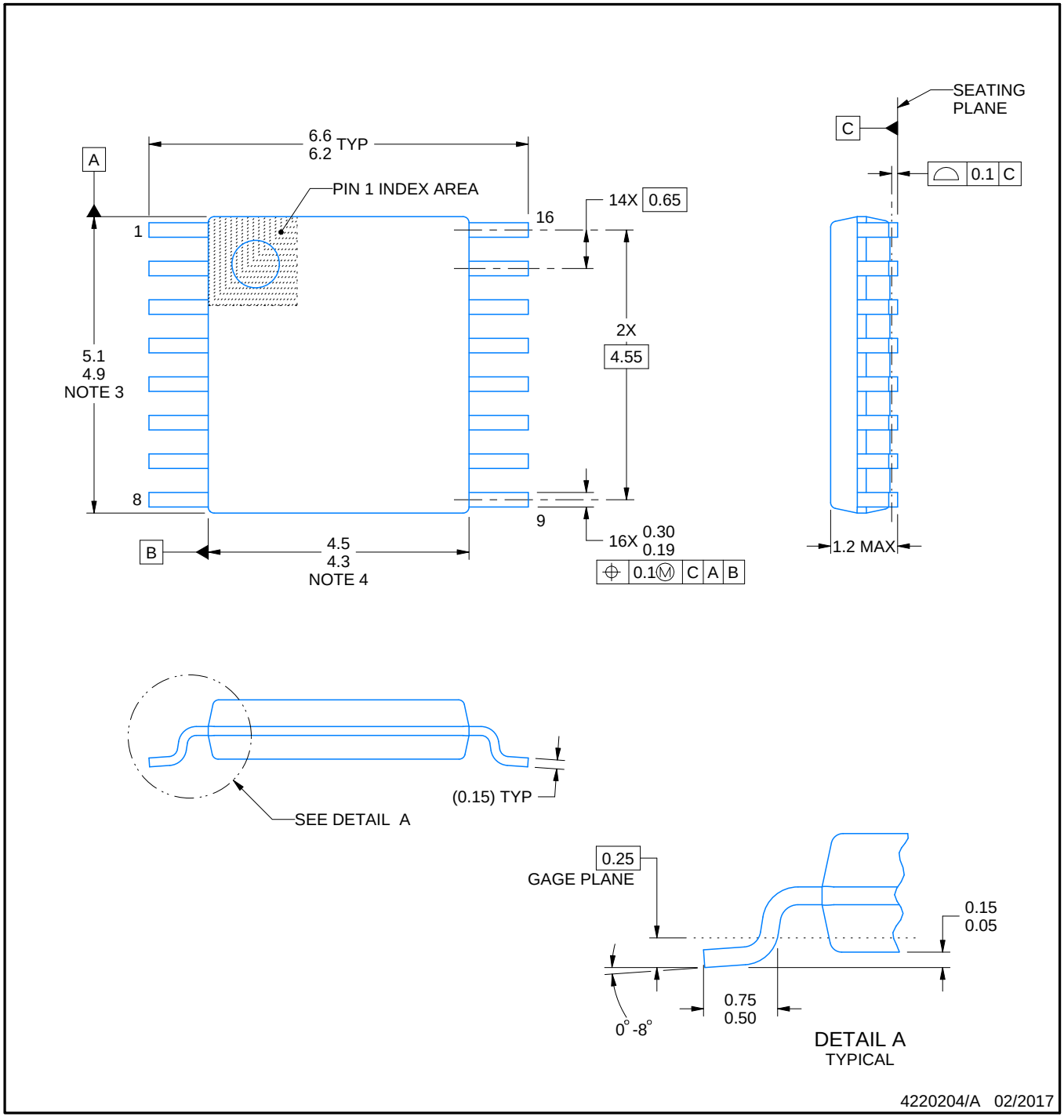
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
BQ76200PW	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

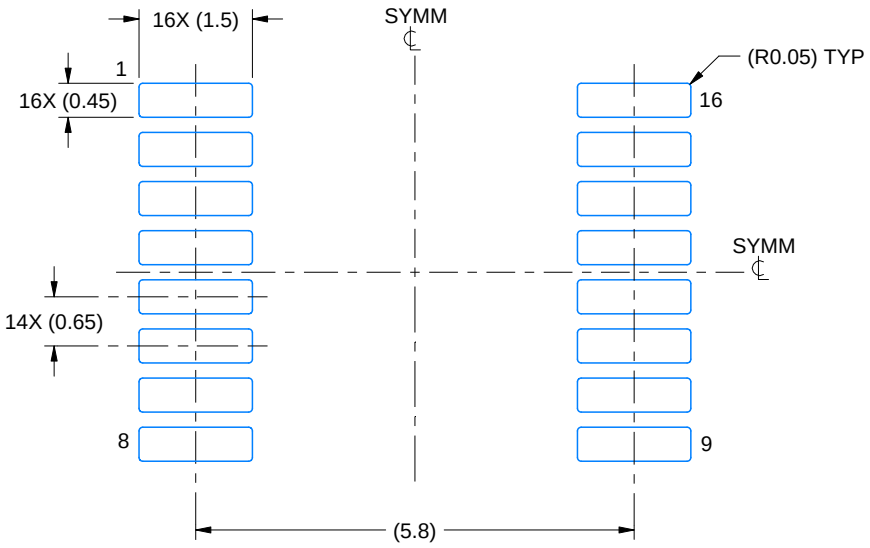
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

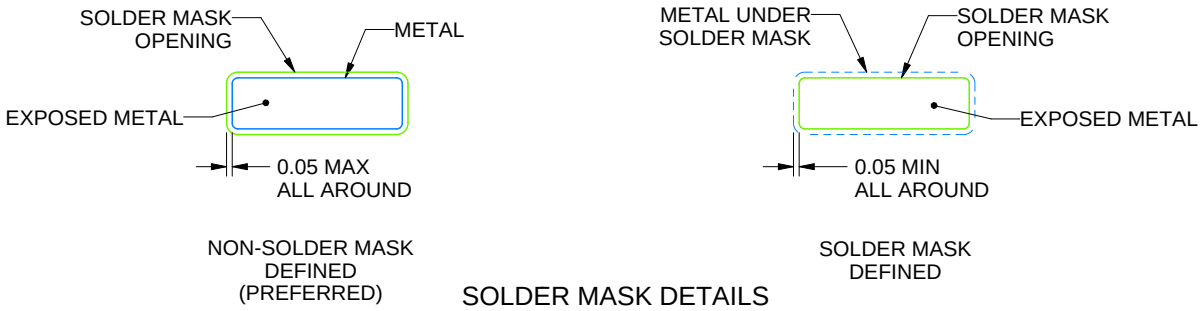


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

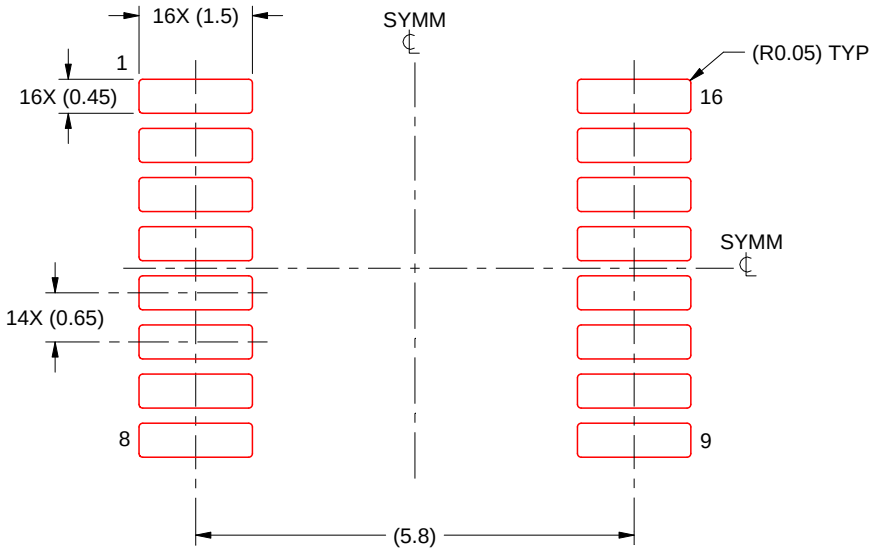


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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