**Ordering & quality**

**Technical documentation**

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**Support & training**

CD54AC240, CD54AC244, CD54ACT240, CD54ACT241, CD54ACT244, CD74AC240, CD74AC244, CD74ACT240, CD74ACT241, CD74ACT244

SCHS287C – DECEMBER 2023 – REVISED MAY 2024

# CDx4AC24x, CDx4ACT24x Octal Buffer/Line Drivers, 3-State

## 1 Features

- SCR-Latch-up-resistant CMOS process and circuit design
- Speed of bipolar FAST /AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5V to 5.5V operation and balanced noise immunity at 30% of the supply
- ±24mA output drive current
  - Fanout to 15 FAST* ICs
  - Drives 50ohm transmission lines

## 2 Description

The RCA CD54/74AC240, CD54/74AC241, and CD54/74AC244 and the CD54/74ACT240, CD54/74ACT241, and CD54/74ACT244 3-state octal buffer/line drivers use the RCA ADVANCED CMOS technology.

### Device Information

| PART NUMBER | PACKAGE[1] | PACKAGE SIZE[2] | BODY SIZE[3] |
|---|---|---|---|
| CDx4AC/ACT24x | DW (SOIC, 20) | 12.8mm x 10.3mm | 12.8mm x 7.5mm |
| | N (PDIP, 20) | 24.33mm x 9.4mm | 24.33mm x 6.35mm |

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) The body size (length × width) is a nominal value and does not include pins.



**Simplified Schematic**

*FAST is a Registered Trademark of Fairchild Semiconductor Corp.*

## Table of Contents

Product Folder Links: *CD54AC240 CD54AC244 CD54ACT240 CD54ACT241 CD54ACT244 CD74AC240 CD74AC244 CD74ACT240 CD74ACT241 CD74ACT244*

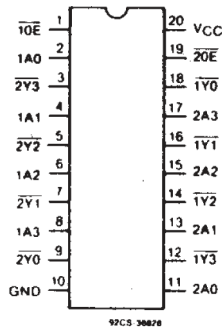## 3 Pin Configuration and Functions



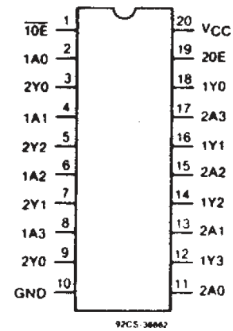**Figure 3-1. CD54/74AC, ACT240 Types Terminal Assignment**
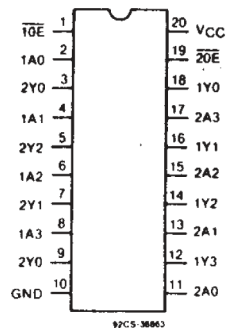


**Figure 3-2. CD54/74AC, ACT241 Types Terminal Assignment**



**Figure 3-3. CD54/74AC, ACT244 Types Terminal Assignment**

**Table 3-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| $1\overline{OE}$ | 1 | I | Bank 1, output enable, active low |
| 1A0 | 2 | I | Bank 1, channel 1 input |
| 2Y3 | 3 | O | Bank 2, channel 4 output |
| 1A1 | 4 | I | Bank 1, channel 2 input |
| 2Y2 | 5 | O | Bank 2, channel 3 output |
| 1A2 | 6 | I | Bank 1, channel 3 input |
| 2Y1 | 7 | O | Bank 2, channel 2 output |
| 1A3 | 8 | I | Bank 1, channel 4 input |
| 2Y0 | 9 | O | Bank 2, channel 1 output |
| GND | 10 | G | Ground |
| 2A0 | 11 | I | Bank 2, channel 1 input |
| 1Y3 | 12 | O | Bank 1, channel 4 output |
| 2A1 | 13 | I | Bank 2, channel 2 input |
| 1Y2 | 14 | O | Bank 1, channel 3 output |
| 2A2 | 15 | I | Bank 2, channel 3 input |
| 1Y1 | 16 | O | Bank 1, channel 2 output |
| 2A3 | 17 | I | Bank 2, channel 4 input |
| 1Y0 | 18 | O | Bank 1, channel 1 output |
| $2\overline{OE}$ | 19 | I | Bank 2, output enable, active low |
| $V_{CC}$ | 20 | P | Positive supply |
| Thermal pad[2] | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply |

(1)    I = input, O = output, I/O = input or output, G = ground, P = power.

(2)    RKS package only.

Product Folder Links: *CD54AC240 CD54AC244 CD54ACT240 CD54ACT241 CD54ACT244 CD74AC240 CD74AC244 CD74ACT240 CD74ACT241 CD74ACT244*

# 4 Specifications

## 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{cc}$ | Supply voltage | | −0.5 | 6 | V |
| $I_{IK}$ | Input diode current | ($V_I$ < −0.5 V or $V_I$ > $V_{CC}$ + 0.5 V) | | ±20 | mA |
| $I_{OK}$ | Output diode current | ($V_o$ < −0.5 V or $V_O$ > $V_{CC}$ + 0.5 V) | | ±50 | mA |
| $I_O$ | Output source or sink current per output pin | ($V_O$ > −0.5 V or $V_O$ < $V_{CC}$ + 0.5 V) | | ±50 | mA |
| | $V_{CC}$ or ground current, ($I_{CC}$ or $I_{GND}$) | | | ±100 | mA[2] |
| $T_{stg}$ | Storage temperature | | -65 | +150 | °C |

(1)    Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2)    For up to 4 outputs per device: add ± 25 mA for each additional output.

## 4.2 Recommended Operating Conditions

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

| CHARACTERISTIC | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ [1] | Supply voltage | | | | |
| | AC Types | | 1.5 | 5.5 | V |
| | ACT Types | | 4.5 | 5.5 | V |
| $V_I$, $V_O$ | Input or Output Voltage | | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature | CD54 | -55 | +125 | °C |
| | | CD74 | -40 | +85 | |
| dt/dv | Input Rise and Fall Slew Rate | | | | |
| | at 1.5 V to 3 V (AC Types) | | 0 | 50 | ns/V |
| | at 3.6 v to 5.5 V (AC Types) | | 0 | 20 | ns/V |
| | at 4.5 V to 5.5 V (ACT Types) | | 0 | 10 | ns/V |

(1)    Unless otherwise specified, all voltages are referenced to ground.

## 4.3 Thermal Information

| THERMAL METRIC[1] | | CDx4AC/ACT24x | | UNIT |
|---|---|---|---|---|
| | | DW (SOIC) | N (PDIP) | |
| | | 20 PINS | | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance | 101.2 | 40 | °C/W |

(1)    For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 4.4 Static Electrical Characteristics: AC Series

| CHARACTERISTICS | | TEST CONDITIONS | | V_CC (V) | AMBIENT TEMPERATURE (T_A) - °C | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | | V_I (V) | I_O (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| V_IH | High-Level Input Voltage | | | 1.5 | 1.2 | — | 1.2 | — | 1.2 | — | V |
| | | | | 3 | 2.1 | — | 2.1 | — | 2.1 | — | |
| | | | | 5.5 | 3.85 | — | 3.85 | — | 3.85 | — | |
| V_IL | Low-Level Input Voltage | | | 1.5 | — | 0.3 | — | 0.3 | — | 0.3 | V |
| | | | | 3 | — | 0.9 | — | 0.9 | — | 0.9 | |
| | | | | 5.5 | — | 1.65 | — | 1.65 | — | 1.65 | |
| V_OH | High-Level Output Voltage | V_IH or V_IL | -0.05 | 1.5 | 1.4 | — | 1.4 | — | 1.4 | — | V |
| | | | -0.05 | 3 | 2.9 | — | 2.9 | — | 2.9 | — | |
| | | | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | |
| | | | -4 | 3 | 2.58 | — | 2.48 | — | 2.4 | — | |
| | | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | (1) , (2) | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| V_ol | Low-Level Output Voltage | V_IH or V_il | 0.05 | 1.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 0.05 | 3 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | |
| | | | 12 | 3 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | (1) , (2) | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| I_I | Input Leakage Current | V_CC or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | μA |
| I_oz | 3-State Leakage Current | v_IH or V_il V_O = V_CC or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | μA |
| I_CC | Quiescent Supply Current, MSI | V_CC or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | μA |

(1)    Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

(2)    Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Product Folder Links: *CD54AC240 CD54AC244 CD54ACT240 CD54ACT241 CD54ACT244 CD74AC240 CD74AC244 CD74ACT240 CD74ACT241 CD74ACT244*

## 4.5 Electrical Characteristics: ACT Series

| CHARACTERISTICS | | TEST CONDITIONS | | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | +25 | | -40 to +85 | | -55 to +125 | | |
| | | $V_I$ (V) | $I_O$ (mA) | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $V_{IH}$ | High-Level Input Voltage | | | 4.5 to 5.5 | 2 | — | 2 | — | 2 | — | V |
| $V_{IL}$ | Low-Level Input Voltage | | | 4.5 to 5.5 | — | 0.8 | — | 0.8 | — | 0.8 | V |
| $V_{OH}$ | High-Level Output Voltage | $V_{IH}$ or $V_{IL}$ | -0.05 | 4.5 | 4.4 | — | 4.4 | — | 4.4 | — | V |
| | | | -24 | 4.5 | 3.94 | — | 3.8 | — | 3.7 | — | |
| | | (1), (2) | -75 | 5.5 | — | — | 3.85 | — | — | — | |
| | | | -50 | 5.5 | — | — | — | — | 3.85 | — | |
| $V_{OL}$ | Low-Level Output Voltage | $V_{IH}$ or $V_{IL}$ | 0.05 | 4.5 | — | 0.1 | — | 0.1 | — | 0.1 | V |
| | | | 24 | 4.5 | — | 0.36 | — | 0.44 | — | 0.5 | |
| | | (1), (2) | 75 | 5.5 | — | — | — | 1.65 | — | — | |
| | | | 50 | 5.5 | — | — | — | — | — | 1.65 | |
| $I_I$ | Input Leakage Current | $V_{CC}$ or GND | | 5.5 | — | ±0.1 | — | ±1 | — | ±1 | µA |
| $I_{OZ}$ | 3-State Leakage Current | $V_{IH}$ or $V_{IL}$ $V_O$ = $V_{CC}$ or GND | | 5.5 | — | ±0.5 | — | ±5 | — | ±10 | µA |
| $I_{CC}$ | Quiescent Supply Current, MSI | $V_{CC}$ or GND | 0 | 5.5 | — | 8 | — | 80 | — | 160 | µA |
| $\Delta I_{CC}$ | Additional Quiescent Supply Current per Input Pin / TTL Inputs High / 1 Unit Load | $V_{cc}$-2.1 | | 4.5 to 5.5 | — | 2.4 | — | 2.8 | — | 3 | mA |

(1) Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

(2) Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C. 75 ohms at +125°C.

**Table 4-1. Act Input Loading Tables**

| CD54/74ACT240 | |
|---|---|
| INPUT | UNIT LOADS[1] |
| nA0 - A3 | 1.42 |
| $\overline{10E}$ | 0.83 |
| $\overline{20E}$ | 0.83 |

| CD54/74ACT241 | |
|---|---|
| INPUT | UNIT LOADS[1] |
| nA0 - A3 | 0.5 |
| $\overline{10E}$ | 0.83 |
| 20E | 1.67 |

| CD54/74ACT244 | |
|---|---|
| INPUT | UNIT LOADS[1] |
| nA0 - A3 | 0.5 |
| $\overline{10E}$ | 0.83 |
| $\overline{20E}$ | 0.83 |

Product Folder Links: CD54AC240 CD54AC244 CD54ACT240 CD54ACT241 CD54ACT244 CD74AC240 CD74AC244 CD74ACT240 CD74ACT241 CD74ACT244

## 4.6 Switching Characteristics: AC Series

$t_r$, $t_l$ 3 ns, $C_L$ = 50 pF

| PARAMETER | CHARACTERISTICS | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN | MAX | MIN | MAX | |
| Propagation Delays: Data to Outputs | | | | | | | |
| $t_{PLH}$ | AC 240 | 1.5 | — | 82 | — | 90 | ns |
| | | 3.3[1] | 2.6 | 9.2 | 2.5 | 10.1 | |
| $t_{PHL}$ | | 5 | 1.9 | 6.5 | 1.8 | 7.2 | |
| $t_{PLH}$ | AC 241, 244 | 1.5 | — | 93 | — | 103 | ns |
| | | 3.3 | 3 | 10.5 | 2.9 | 11.5 | |
| $t_{PHL}$ | | 5 | 2.2 | 7.5 | 2.1 | 8.2 | |
| $t_{PZL}$ | Output Enable Times | 1.5 | — | 136 | — | — | ns |
| | | 3.3 | 4.6 | 16.4 | 4.5 | 18 | |
| $t_{PZH}$ | | 5 | 3.1 | 10.9 | 3 | 12 | |
| $t_{PLZ}$ | Output Disable Times | 1.5 | — | 136 | — | 150 | ns |
| | | 3.3 | 3.9 | 13.6 | 3.8 | 15 | |
| $t_{PHZ}$ | | 5 | 3.1 | 10.9 | 3 | 12 | |
| Power Dissipation Capacitance | | | | | | | |
| $C_{PD}$§ | AC240 | — | 65 Typ. | | 65 Typ. | | pF |
| | AC241, 244 | — | 71 Typ. | | 71 Typ. | | |
| Min. (Valley) $V_{oh}$ | | | | | | | |
| $V_{OHV}$ | During Switching of Other Outputs (Output Under Test Not Switching) | 5 | 4 Typ @25°C | | | | V |
| Max. (Peak) $V_{OL}$ | | | | | | | |
| $V_{OLP}$ | During Switching of Other Outputs (Output Under Test Not Switching) | 5 | 1 Typ. @ 25°C | | | | V |
| $C_I$ | Input Capacitance | — | — | 10 | — | 10 | pF |
| $C_O$ | 3-State Output Capacitance | — | — | 15 | — | 15 | pF |

## 4.7 Switching Characteristics: ACT Series

$t_r$, $t_l$ = 3 ns, $C_L$ = 50 pF

| PARAMETER | CHARACTERISTICS | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN | MAX | MIN | MAX | |
| Propagation Delays: Data to Outputs | | | | | | | |
| $t_{PLH}$ $t_{PHL}$ | ACT240 | 5[2] | 2.3 | 7.8 | 2.2 | 8.6 | ns |
| $t_{PLH}$ $t_{PHL}$ | ACT241, 244 | 5 | 2.5 | 8.7 | 2.4 | 9.6 | ns |
| $t_{PZL}$ $t_{PZH}$ | Output Enable Times | 5 | 3.5 | 12.2 | 3.4 | 13.4 | ns |
| $t_{PLZ}$ $t_{PHZ}$ | Output Disable Times | 5 | 3.5 | 12.2 | 3.4 | 13.4 | ns |
| Power Dissipation Capacitance | | | | | | | |
| $C_{PD}$§[3] | ACT240 | — | 65 Typ | | 65 Typ | | pF |
| | ACT241, 244 | — | 71 Typ | | 71 Typ | | pF |

Product Folder Links: *CD54AC240 CD54AC244 CD54ACT240 CD54ACT241 CD54ACT244 CD74AC240 CD74AC244 CD74ACT240 CD74ACT241 CD74ACT244*

$t_r$, $t_l$ = 3 ns, $C_L$ = 50 pF

| PARAMETER | CHARACTERISTICS | $V_{CC}$ (V) | AMBIENT TEMPERATURE ($T_A$) - °C | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | -40 to +85 | | -55 to +125 | | |
| | | | MIN | MAX | MIN | MAX | |
| Min. (Valley) $V_{oh}$ $V_{OHV}$ [1] | During Switching of Other Outputs (Output Under Test Not Switching) | 5 | 4 Typ @25°C | | | | V |
| Max. (Peak) $V_{OL}$ $V_{OLP}$ [1] | During Switching of Other Outputs (Output Under Test Not Switching) | 5 | 1 Typ. @ 25°C | | | | V |
| $C_I$ | Input Capacitance | — | — | 10 | — | 10 | pF |
| $C_O$ | 3-State Output Capacitance | — | — | 15 | — | 15 | pF |

(1)  3.3 V: min. is @ 3.6 V; max. is @ 3 V
(2)  5 V: min. is @ 5.5 V; max. is @ 4.5 V
(3)  $C_{PD}$ is used to determine the dynamic power consumption, per package.
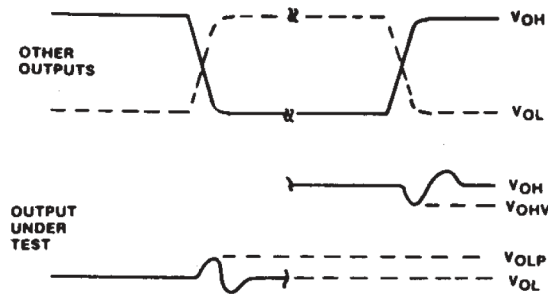
    a.    For AC series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$

    b.    For ACT series: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where $f_i$ = input frequency

        i.    $C_L$ = output load capacitance

        ii.    $V_{CC}$ = supply voltage.

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Product Folder Links: CD54AC240 CD54AC244 CD54ACT240 CD54ACT241 CD54ACT244 CD74AC240 CD74AC244 CD74ACT240 CD74ACT241 CD74ACT244

## 5 Parameter Measurement Information



A.  $V_{OHV}$ AND $V_{OLP}$ ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.

B.  INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS: PRR ≤ 1 MHz, $t_r$ = 3 ns, $t_f$ = 3 ns, SKEW 1 ns.

C.  R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1 $\mu$F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

D.  92CS-42406
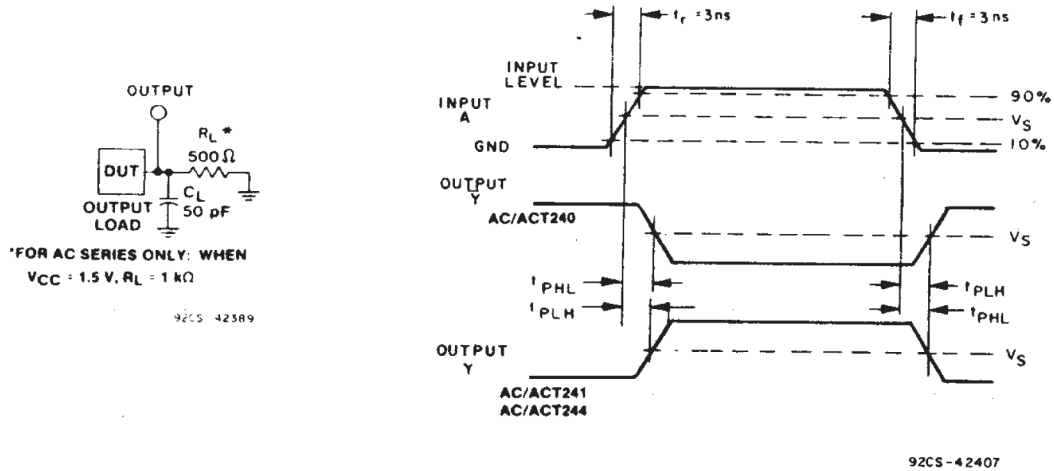
**Figure 5-1. Simultaneous Switching Transient Waveforms.**
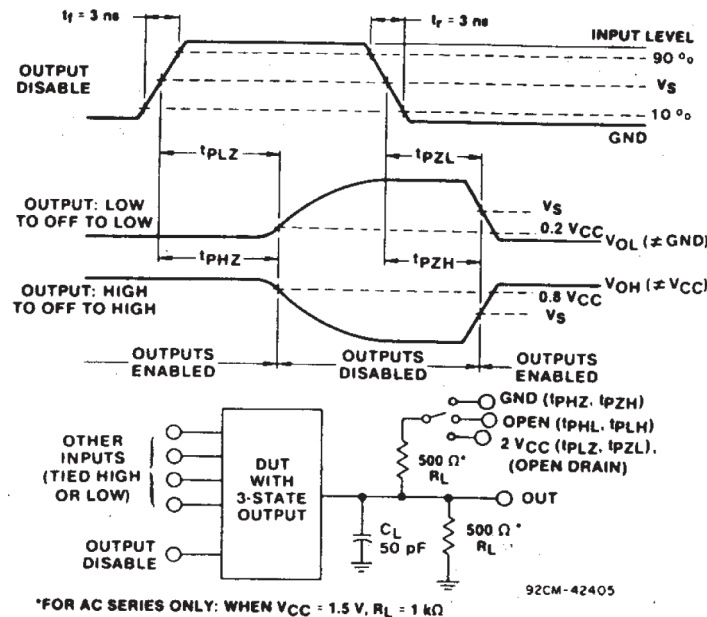


**Figure 5-2. Three-state Propagation Delay Times and Test Circuit.**

Product Folder Links: *CD54AC240 CD54AC244 CD54ACT240 CD54ACT241 CD54ACT244 CD74AC240 CD74AC244 CD74ACT240 CD74ACT241 CD74ACT244*

**Figure 5-3. Propagation Delay Times and Test Circuit.**

|  | CDX4AC | CDX4ACT |
|---|---|---|
| Input Level | $V_{CC}$ | 3 V |
| Input Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 1.5 V |
| Output Switching Voltage, $V_S$ | 0.5 $V_{CC}$ | 0.5 $V_{CC}$ |

# 6 Detailed Description

## 6.1 Overview

The RCA CD54/74AC240, CD54/74AC241, and CD54/74AC244 and the CD54/74ACT240, CD54/74ACT241, and CD54/74ACT244 3-state octal buffer/line drivers use the RCA ADVANCED CMOS technology. The CD54/74AC/ACT240 and CD54/74AC/ACT244 have active-LOW output enables ($\overline{1OE}$, $\overline{2OE}$). The CD54/74AC/ACT241 has one active-LOW ($\overline{1OE}$) and one active-HIGH (2OE) output enable.

The CD74AC240 and CD74ACT240 are supplied in 20-lead dual-in-line plastic packages (E suffix) and 20-lead small-outline packages (M and M96 suffixes). The CD74AC241 is supplied in 20-lead dual-in-line plastic packages (E suffix) and the CD74ACT241 is supplied in 20-lead dual-in-line plastic packages (E suffix) and 20-lead small-outline packages (M96 suffix). The CD74AC244 and CD74ACT244 are supplied in 20-lead dual-in-line plastic packages (E suffix), 20-lead small-outline packages (M and M96 suffixes), and 20-lead shrink small-outline packages (SM96 suffix). These package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (−40 to +85°C); and Extended Industrial/Military (−55 to +125°C).

The CD54AC240 and CD54AC244 and the CD54ACT240, CD54ACT241, and CD54ACT244 are supplied in 20-lead hermetic dual-in-line ceramic packages (F3A suffix) and are operable over the −55 to +125°C temperature range.

## 6.2 Functional Block Diagram
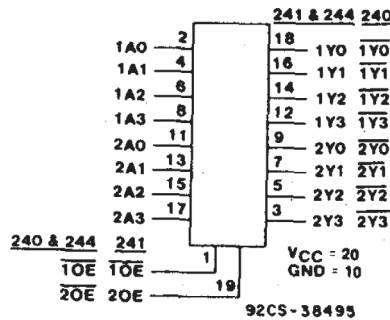


## 6.3 Device Functional Modes

**Table 6-1. Truth Tables**

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{1OE}$, $\overline{2OE}$ | A | Y |
| L | L | H |
| L | H | L |
| H | X | Z |
| (AC/ACT240) | | |

| INPUTS | | OUTPUT |
|---|---|---|
| $\overline{1OE}$, $\overline{2OE}$ | A | Y |
| L | L | L |
| L | H | H |
| H | X | Z |
| (AC/ACT244) | | |

| INPUTS | | OUTPUT | INPUTS | | OUTPUT |
|---|---|---|---|---|---|
| $\overline{10E}$ | 1A | 1Y | 20E | 2A | 2Y |
| L | L | L | L | X | Z |
| L | H | H | H | L | L |
| H | X | Z | H | H | H |
| (AC/ACT241) | | | | | |

## 7 Application and Implementation

---

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

---

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in *Section 4.2*.

Each $V_{CC}$ terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1 µF and if there are multiple $V_{CC}$ terminals, then TI recommends .01 µF or .022 µF for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 µF and 1 µF are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$ whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

# 8 Device and Documentation Support

## 8.1 Documentation Support (Analog)

### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 8-1. Related Links**

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| CD74AC240 | Click here | Click here | Click here | Click here | Click here |
| CD74AC244 | Click here | Click here | Click here | Click here | Click here |
| CD74ACT240 | Click here | Click here | Click here | Click here | Click here |
| CD74ACT241 | Click here | Click here | Click here | Click here | Click here |
| CD74ACT244 | Click here | Click here | Click here | Click here | Click here |

## 8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

## 8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.6 Glossary

TI Glossary     This glossary lists and explains terms, acronyms, and definitions.

# 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Product Folder Links: *CD54AC240 CD54AC244 CD54ACT240 CD54ACT241 CD54ACT244 CD74AC240 CD74AC244 CD74ACT240 CD74ACT241 CD74ACT244*

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD54AC240F3A | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54AC240F3A | Samples |
| CD54AC244F3A | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54AC244F3A | Samples |
| CD54ACT240F3A | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54ACT240F3A | Samples |
| CD54ACT241F3A | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54ACT241F3A | Samples |
| CD54ACT244F3A | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54ACT244F3A | Samples |
| CD74AC240E | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC240E | Samples |
| CD74AC240EE4 | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC240E | Samples |
| CD74AC240M | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -55 to 125 | AC240M | |
| CD74AC240M96 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | AC240M | Samples |
| CD74AC244E | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74AC244E | Samples |
| CD74AC244M | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -55 to 125 | AC244M | |
| CD74AC244M96 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (AC244, AC244M) | Samples |
| CD74ACT240E | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT240E | Samples |
| CD74ACT240M | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -55 to 125 | ACT240M | |
| CD74ACT240M96 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT240M | Samples |
| CD74ACT240M96E4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT240M | Samples |
| CD74ACT241E | ACTIVE | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT241E | Samples |
| CD74ACT241M96 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | ACT241M | Samples |
| CD74ACT244E | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74ACT244E | Samples |
| CD74ACT244M96 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | (ACT244, ACT244M) | Samples |

**(1)** The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54AC240, CD54AC244, CD54ACT240, CD54ACT241, CD54ACT244, CD74AC240, CD74AC244, CD74ACT240, CD74ACT241, CD74ACT244 :**

● Catalog : CD74AC240, CD74AC244, CD74ACT240, CD74ACT241, CD74ACT244

● Military : CD54AC240, CD54AC244, CD54ACT240, CD54ACT241, CD54ACT244

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74AC240M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74AC244M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74AC244M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74ACT240M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74ACT241M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74ACT244M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| CD74ACT244M96 | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74AC240M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74AC244M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74AC244M96 | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| CD74ACT240M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74ACT241M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74ACT244M96 | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| CD74ACT244M96 | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |

![Texas Instruments logo] **PACKAGE MATERIALS INFORMATION**

## TUBE



**T - Tube height**

**L - Tube length**

**W - Tube width**

**B - Alignment groove width**

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CD74AC240E | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC240EE4 | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74AC244E | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT240E | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT241E | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| CD74ACT244E | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |

J (R—GDIP—T**)                    CERAMIC DUAL IN—LINE PACKAGE
14 LEADS SHOWN

| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |

B

14                    8

C

1                    7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
         C.  This package is hermetically sealed with a ceramic lid using glass frit.
         D.  Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E.  Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

**N (R-PDIP-T**)**
16 PINS SHOWN

**PLASTIC DUAL-IN-LINE PACKAGE**

| DIM | PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|---|
| A MAX | | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS-001 VARIATION | | AA | BB | AC | AD |

A

16    9

0.260 (6,60)
0.240 (6,10)

1    8

0.070 (1,78)
0.045 (1,14)  /D\

0.045 (1,14)
0.030 (0,76)  /D\

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.010 (0,25) NOM

0.125 (3,18) MIN

0.100 (2,54)

0.430 (10,92) MAX

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option  /D\

4040049/E  12/2002

NOTES:  A.  All linear dimensions are in inches (millimeters).
        B.  This drawing is subject to change without notice.
    /C\  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
    /D\  The 20 pin end lead shoulder width is a vendor option, either half or full width.

TEXAS
INSTRUMENTS
www.ti.com

10.63 / 9.97 TYP

A

PIN 1 ID AREA

1

20

18X 1.27

13.0 / 12.6 NOTE 3

10

11

2X 11.43

20X 0.51 / 0.31

⊕ 0.25 Ⓜ C A B

B

7.6 / 7.4 NOTE 4

C

SEATING PLANE

◯ 0.1 C

2.65 MAX

0.33 / 0.10 TYP

SEE DETAIL A

0.25 GAGE PLANE

0° - 8°

1.27 / 0.40

0.3 / 0.1

DETAIL A
TYPICAL

4220724/A  05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

## DW0020A

SOIC

20X (2)

SYMM

1

20

20X (0.6)

18X (1.27)

SYMM

(R0.05)
TYP

10

11

(9.3)

**LAND PATTERN EXAMPLE**
SCALE:6X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

4220724/A   05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

20X (2)

1

20X (0.6)

18X (1.27)

SYMM

SYMM

20

10

11

(9.3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A   05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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