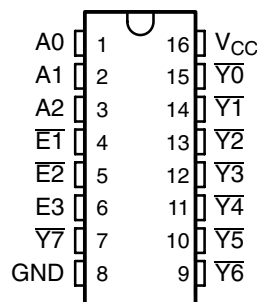


**CD74HC138-Q1**  
**HIGH-SPEED CMOS LOGIC**  
**3- TO 8-LINE INVERTING DECODER/DEMULTIPLEXER**

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- Qualified for Automotive Applications
- Select One of Eight Data Outputs Active Low
- I/O Port or Memory Selector
- Three Enable Inputs to Simplify Cascading
- Typical Propagation Delay of 13 ns at  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (Over Temperature Range)
  - Standard Outputs . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . 15 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- 2-V to 6-V  $V_{CC}$  Operation
- High Noise Immunity;  $N_{IL}$  or  $N_{IH} = 30\%$  of  $V_{CC}$ ,  $V_{CC} = 5\text{ V}$

M PACKAGE  
(TOP VIEW)



**description/ordering information**

The CD74HC138 is a high-speed silicon-gate CMOS decoder well suited to memory address decoding or data routing applications. This circuit features low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low-power Schottky TTL logic. The circuit has three binary select inputs (A0, A1, and A2). If the device is enabled, these inputs determine which one of the eight normally high outputs of the HC138 will go low.

Two active-low and one active-high enables ( $\overline{E1}$ ,  $\overline{E2}$ , and E3) are provided to ease the cascading of decoders. The decoder's eight outputs can drive ten low-power Schottky TTL equivalent loads.

**ORDERING INFORMATION†**

$T_A$	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Reel of 2500	CD74HC138QM96Q1	HC138Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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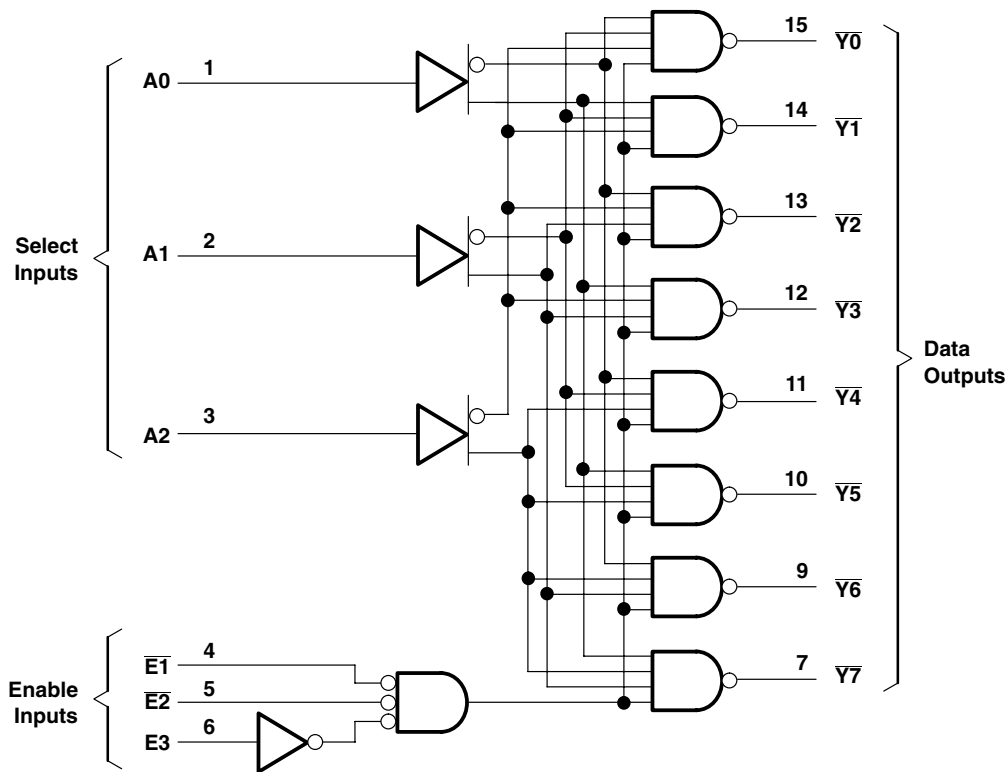
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**FUNCTION TABLE**

ENABLE INPUTS			SELECT INPUTS			OUTPUTS							
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

NOTE: H = High voltage level, L = Low voltage level, X = Don't care

**logic diagram (positive logic)**



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**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†**

Supply voltage range, $V_{CC}$ (see Note 1)	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V)	±20 mA
Source or sink current per output pin, $I_O$ ( $V_O > -0.5$ V or $V_O < V_{CC} + 0.5$ V)	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2)	73°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages referenced to GND unless otherwise specified.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

**recommended operating conditions (see Note 3)**

		MIN	MAX	UNIT	
$V_{CC}$	Supply voltage	2	6	V	
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V	
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V	
		$V_{CC} = 4.5$ V	1.35		
		$V_{CC} = 6$ V	1.8		
$V_I$	Input voltage	0	$V_{CC}$	V	
$V_O$	Output voltage	0	$V_{CC}$	V	
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000	ns
		$V_{CC} = 4.5$ V	0	500	
		$V_{CC} = 6$ V	0	400	
$T_A$	Operating free-air temperature	–40	125	°C	

- NOTES: 3. All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		I <sub>o</sub> (mA)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	-0.02	2 V	1.9			1.9		V
			-0.02	4.5 V	4.4			4.4		
			-0.02	6 V	5.9			5.9		
		TTL loads	-4	4.5 V	3.98			3.7		
			-5.2	6 V	5.48			5.2		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	CMOS loads	0.02	2 V	0.1			0.1		V
			0.02	4.5 V	0.1			0.1		
			0.02	6 V	0.1			0.1		
		TTL loads	4	4.5 V	0.26			0.4		
			5.2	6 V	0.26			0.4		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			6 V	±0.1			±1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		0	6 V	8			160		μA
C <sub>IN</sub>					10			10		pF

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	C <sub>L</sub> = 15 pF	5 V	13					ns
				2 V	150			225		
			C <sub>L</sub> = 50 pF	4.5 V	30			45		
				6 V	26			38		
	E	Y	C <sub>L</sub> = 50 pF	2 V	150			265		
				4.5 V	30			53		
6 V	26			45						
t <sub>t</sub>		Y	C <sub>L</sub> = 50 pF	2 V	75			110		ns
				4.5 V	15			22		
				6 V	13			19		

operating characteristics, V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C, Input t<sub>r</sub>, t<sub>f</sub> = 6 ns, C<sub>L</sub> = 15 pF

PARAMETER	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance (see Note 4)	67	pF

NOTE 4: C<sub>pd</sub> is used to determine the dynamic power consumption, per gate.

$$P_D = V_{CC}^2 f_i (C_{pd} + C_L)$$

f<sub>i</sub> = input frequency

C<sub>L</sub> = output load capacitance

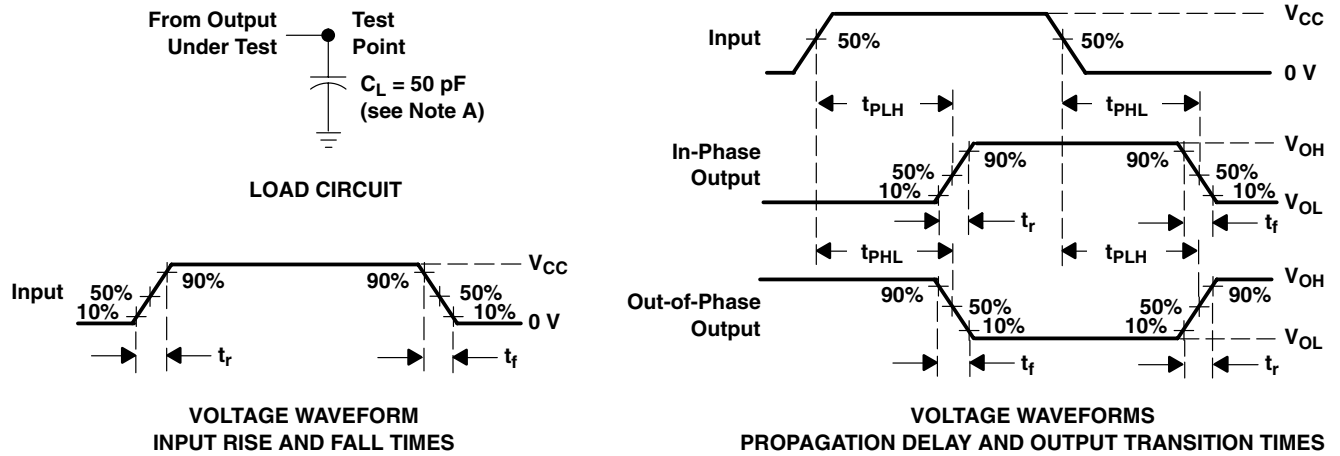
V<sub>CC</sub> = supply voltage



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**PARAMETER MEASUREMENT INFORMATION**



- NOTES:
- $C_L$  includes probe and test-fixture capacitance.
  - Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - The outputs are measured one at a time, with one input transition per measurement.
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC138QM96Q1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC138Q	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD74HC138-Q1 :**

- Catalog: [CD74HC138](#)
- Military: [CD54HC138](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



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