CSD17318Q2 30V N-Channel NexFET™ Power MOSFET

1 Features

- Optimized for 5V gate drive
- Low capacitance and charge
- Low $R_{DS(ON)}$
- Low-thermal resistance
- Lead free
- RoHS compliant
- Halogen free
- SON 2mm × 2mm plastic package

2 Applications

- Storage, tablets, and handheld devices
- Optimized for load switch applications
- DC-DC converters
- Battery and load management applications

3 Description

This 30V, 12.6mΩ, 2mm × 2mm SON NexFET™ power MOSFET is designed to minimize losses in power conversion applications and optimized for 5V gate drive applications. The 2mm × 2mm SON offers excellent thermal performance for the size of the package.

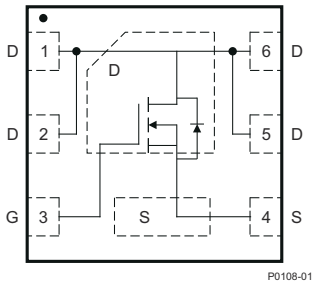
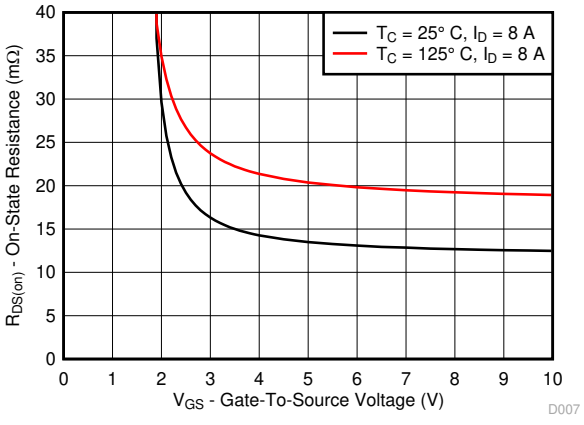


Figure 3-1. Top View



On-State Resistance vs Gate to Source Voltage

Product Summary

T_A = 25°C		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5V)	6.0		nC
Q_{gd}	Gate Charge Gate-to-Drain	1.3		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	V_{GS} = 2.5V	20	mΩ
		V_{GS} = 4.5V	13.9	
		V_{GS} = 8V	12.6	
$V_{GS(th)}$	Threshold Voltage	0.9		V

Device Information(1)

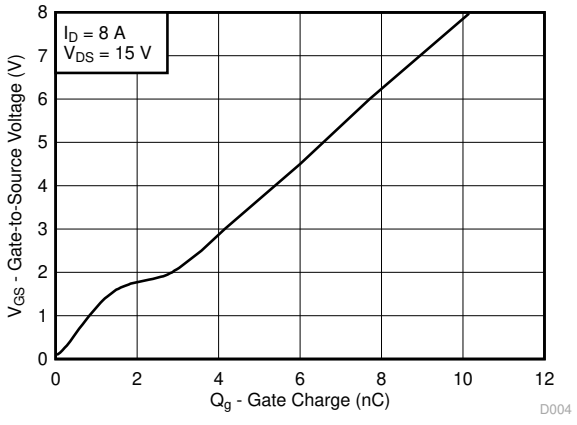
PART NUMBER	QTY	MEDIA	PACKAGE	SHIP
CSD17318Q2	3000	7 Inch Reel	SON 2.00mm × 2.00mm Plastic Package	Tape and Reel
CSD17318Q2T	250			

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

T_A = 25°C		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±10	V
I_D	Continuous Drain Current (Package Limited)	21.5	A
	Continuous Drain Current (Silicon Limited), T_C = 25°C	25	
	Continuous Drain Current(1)	10	
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	68	A
P_D	Power Dissipation(1)	2.5	W
	Power Dissipation, T_C = 25°C	16	
T_J, T_{STG}	Operating Junction, Storage Temperature	–55 to 150	°C
E_{AS}	Avalanche Energy, Single Pulse, I_D = 12.4A, L = 0.1mH, R_G = 25Ω	7.7	mJ

(1) Typical $R_{\theta JA}$ = 55°C/W on a 1in², 2oz Cu pad on a 0.06in thick FR4 PCB.
(2) Max $R_{\theta JC}$ = 7°C/W, pulse duration ≤ 100µs, duty cycle ≤ 1%.



Gate Charge

Table of Contents

1 Features....1
2 Applications....1
3 Description....1
4 Specifications....3
4.1 Electrical Characteristics....3
4.2 Thermal Characteristics....3
4.3 Typical MOSFET Characteristics....4
5 Device and Documentation Support....7
5.1 Receiving Notification of Documentation Updates....7
5.2 Support Resources....7
5.3 Trademarks....7
6 Revision History....7
7 Mechanical, Packaging, and Orderable Information....8

4 Specifications

4.1 Electrical Characteristics

T_A = 25°C (unless otherwise noted)

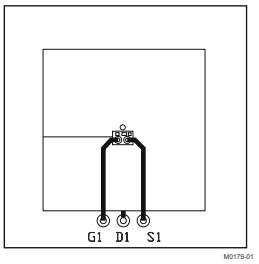
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0V, I_D = 250µA	30			V
I_{DSS}	Drain-to-source leakage	V_{GS} = 0V, V_{DS} = 24V			1	µA
I_{GSS}	Gate-to-source leakage	V_{DS} = 0V, V_{GS} = 10V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	0.6	0.9	1.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 2.5V, I_D = 8A		20	30	mΩ
		V_{GS} = 4.5V, I_D = 8A		13.9	16.9	
		V_{GS} = 8V, I_D = 8A		12.6	15.1	
g_{fs}	Transconductance	V_{DS} = 3V, I_D = 8A		42		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0V, V_{DS} = 15V, f = 1MHz		676	879	pF
C_{oss}	Output capacitance			71	92	pF
C_{rss}	Reverse transfer capacitance			39	51	pF
R_G	Series gate resistance			1.0	2.0	Ω
Q_g	Gate charge total (4.5 V)	V_{DS} = 15V, I_D = 8A		6.0		nC
Q_{gd}	Gate charge gate-to-drain			1.3		nC
Q_{gs}	Gate charge gate-to-source			1.5		nC
$Q_{g(th)}$	Gate charge at Vth			0.7		nC
Q_{oss}	Output charge	V_{DS} = 15V, V_{GS} = 0V		2.7		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 15V, V_{GS} = 4.5V, I_D = 8A, R_G = 2Ω		5		ns
t_r	Rise time			16		ns
$t_{d(off)}$	Turnoff delay time			13		ns
t_f	Fall time			4		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 8A, V_{GS} = 0V		0.8	1.0	V
Q_{rr}	Reverse recovery charge	V_{DD}= 15V, I_F = 8A, di/dt = 300A/µs		2.9		nC
t_{rr}	Reverse recovery time			12		ns

4.2 Thermal Characteristics

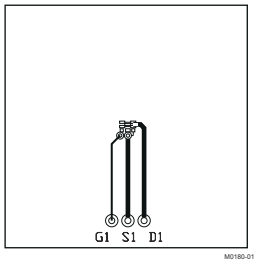
T_A = 25°C (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal resistance junction-to-case(1)			7.9	°C/W
$R_{\theta JA}$	Thermal resistance junction-to-ambient(1) (2)			65	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu pad on a 1.5in × 1.5in (3.81cm × 3.81cm), 0.06in (1.52mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1in^2 (6.45cm^2), 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 65°C/W when mounted on 1in^2 (6.45cm^2) of 2oz (0.071mm) thick Cu.



Max $R_{\theta JA}$ = 250°C/W when mounted on a minimum pad area of 2oz (0.071mm) thick Cu.

4.3 Typical MOSFET Characteristics

T_A = 25°C (unless otherwise noted)

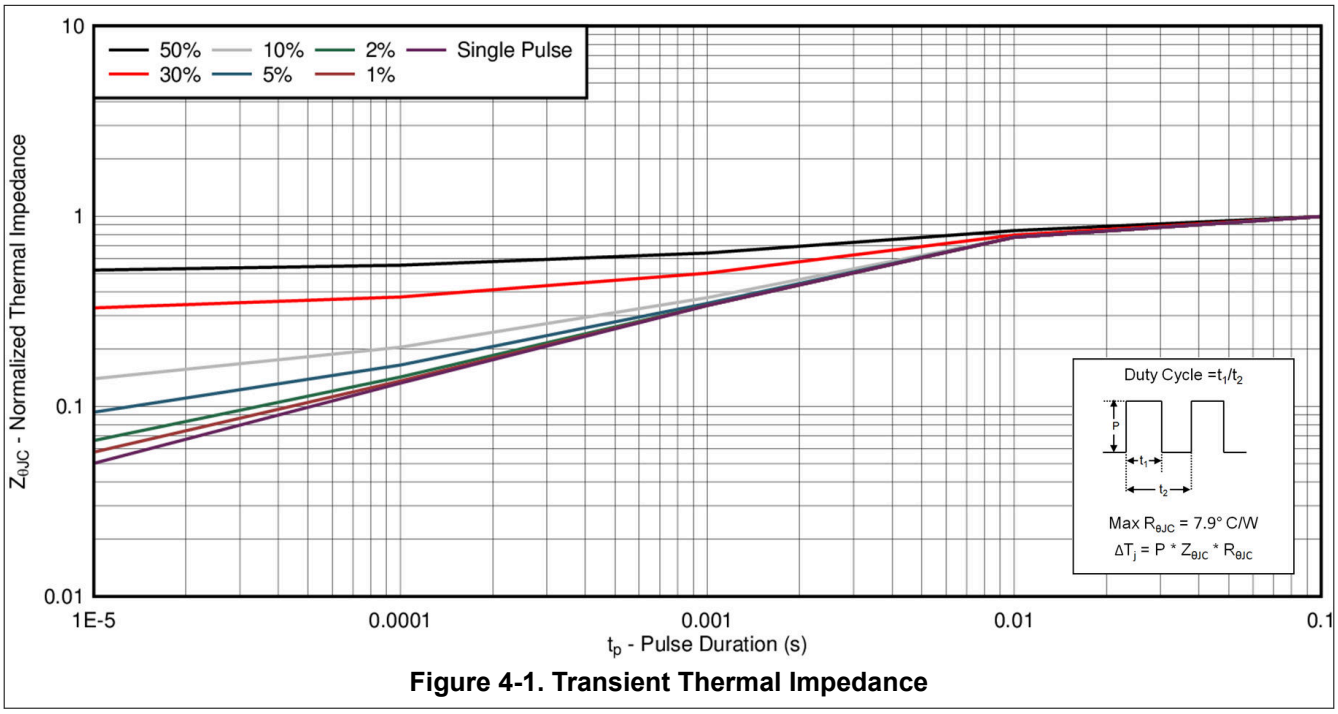


Figure 4-1. Transient Thermal Impedance

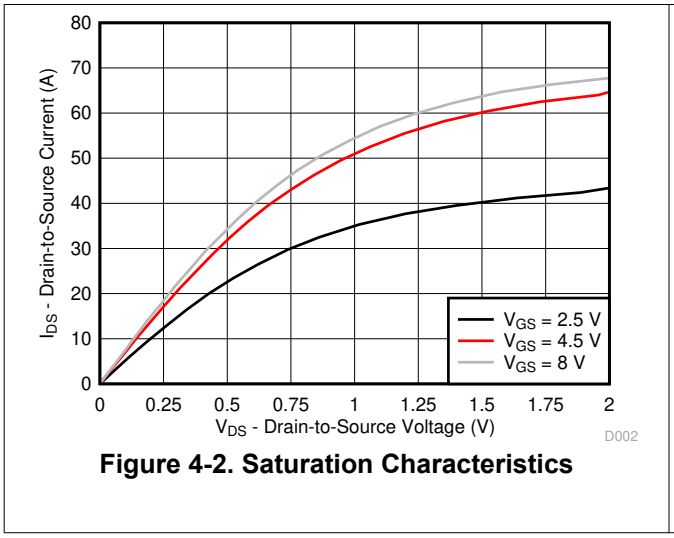
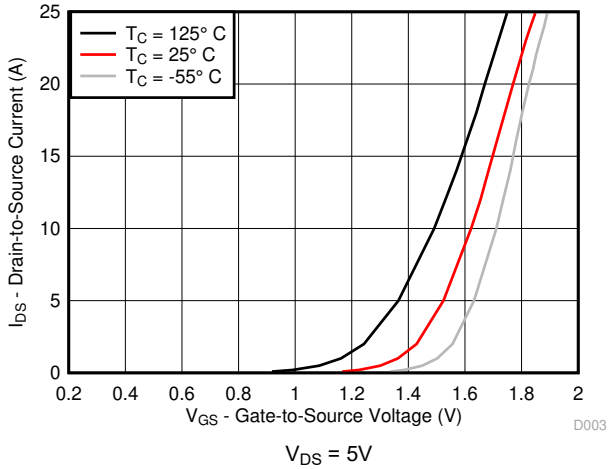
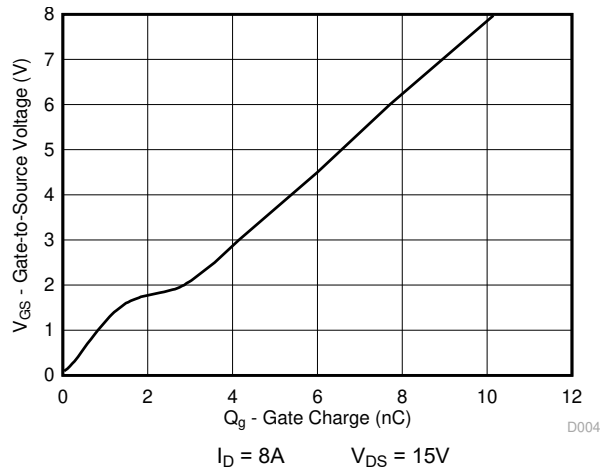


Figure 4-2. Saturation Characteristics



V_{DS} = 5V

Figure 4-3. Transfer Characteristics



I_D = 8A V_{DS} = 15V

Figure 4-4. Gate Charge

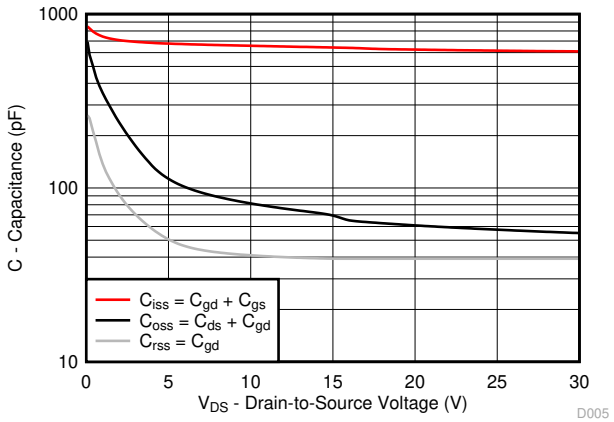
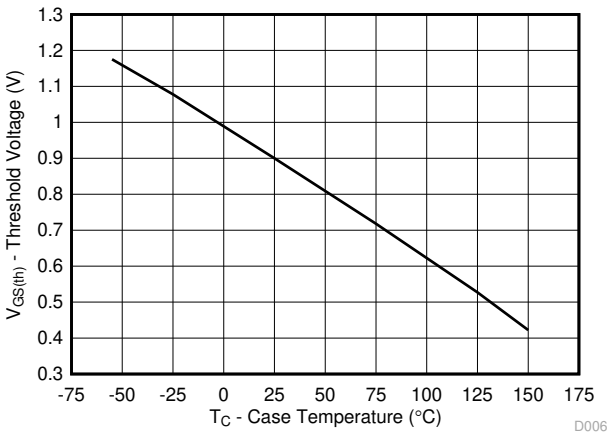
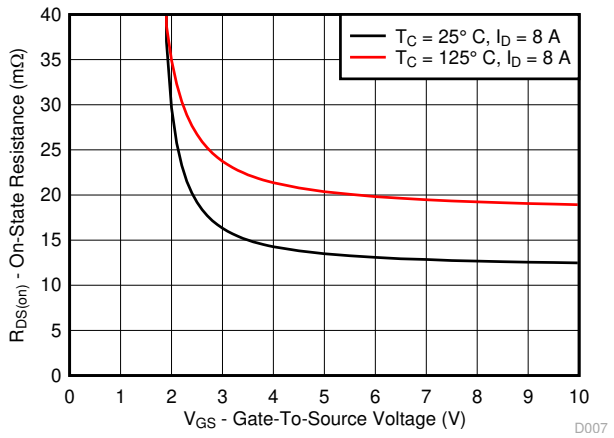


Figure 4-5. Capacitance



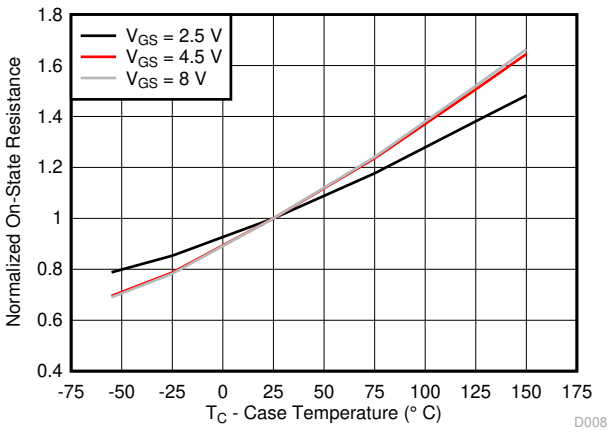
I_D = 250µA

Figure 4-6. Threshold Voltage vs Temperature



I_D = 8A

Figure 4-7. On-State Resistance vs Gate-to-Source Voltage



I_D = 8A

Figure 4-8. Normalized On-State Resistance vs Temperature

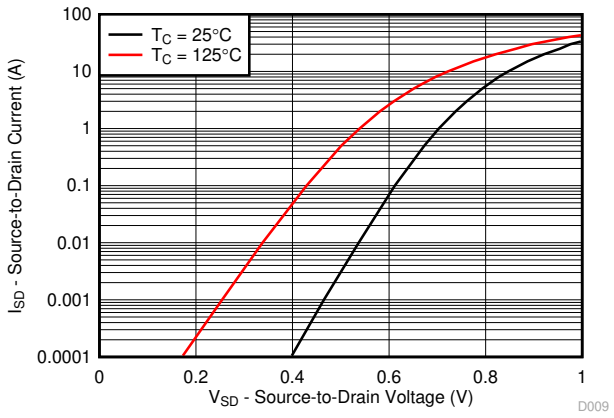
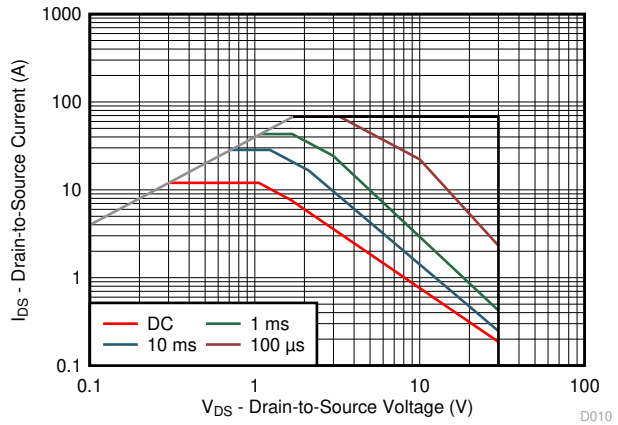


Figure 4-9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 7.9°C/W

Figure 4-10. Maximum Safe Operating Area

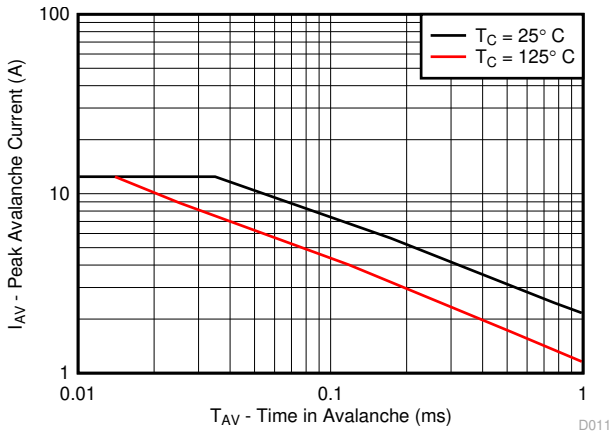


Figure 4-11. Single Pulse Unclamped Inductive Switching

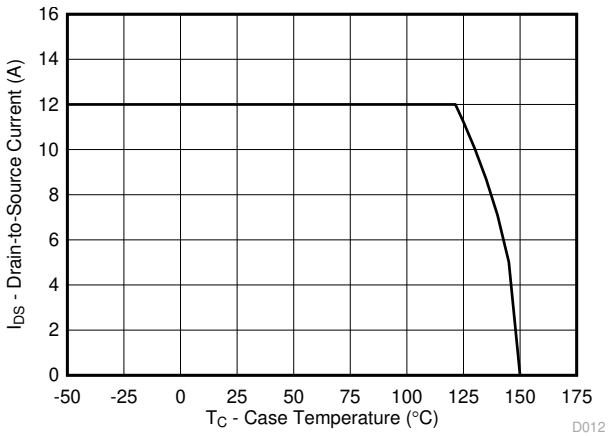


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.3 Trademarks

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All trademarks are the property of their respective owners.

6 Revision History

Changes from Revision A (February 2017) to Revision B (June 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17318Q2	ACTIVE	WSON	DQK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1718	Samples
CSD17318Q2T	ACTIVE	WSON	DQK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	1718	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

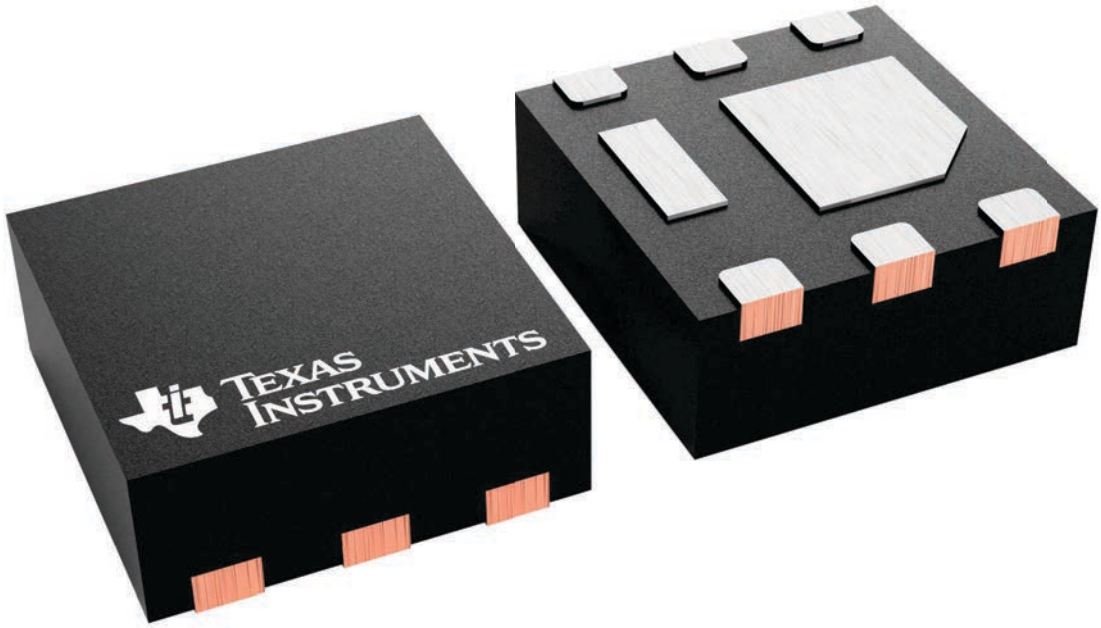
DQK 6

WSON - 0.8 mm max height

2 x 2, 0.65 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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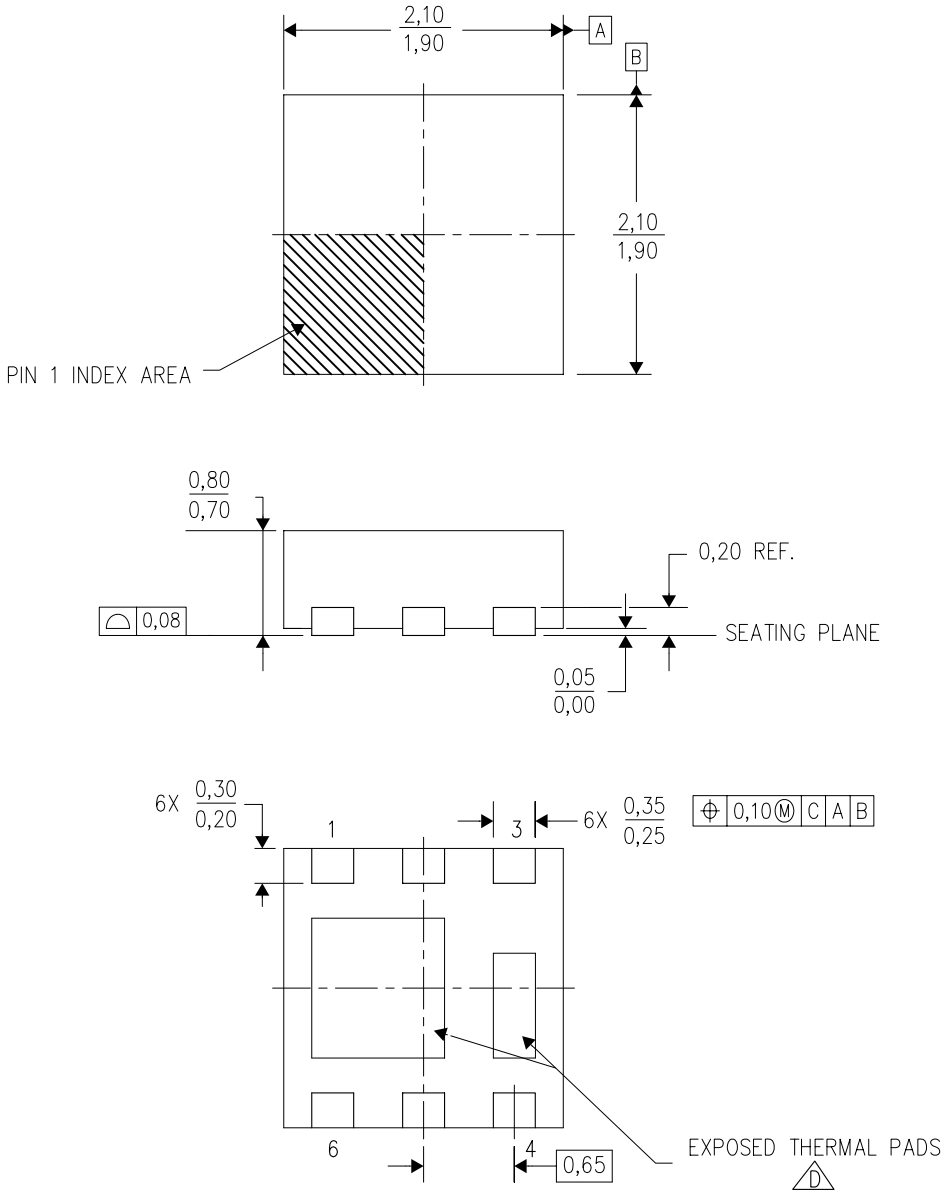
DQK (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pads must be soldered to the board for thermal and mechanical performance.

THERMAL PAD MECHANICAL DATA

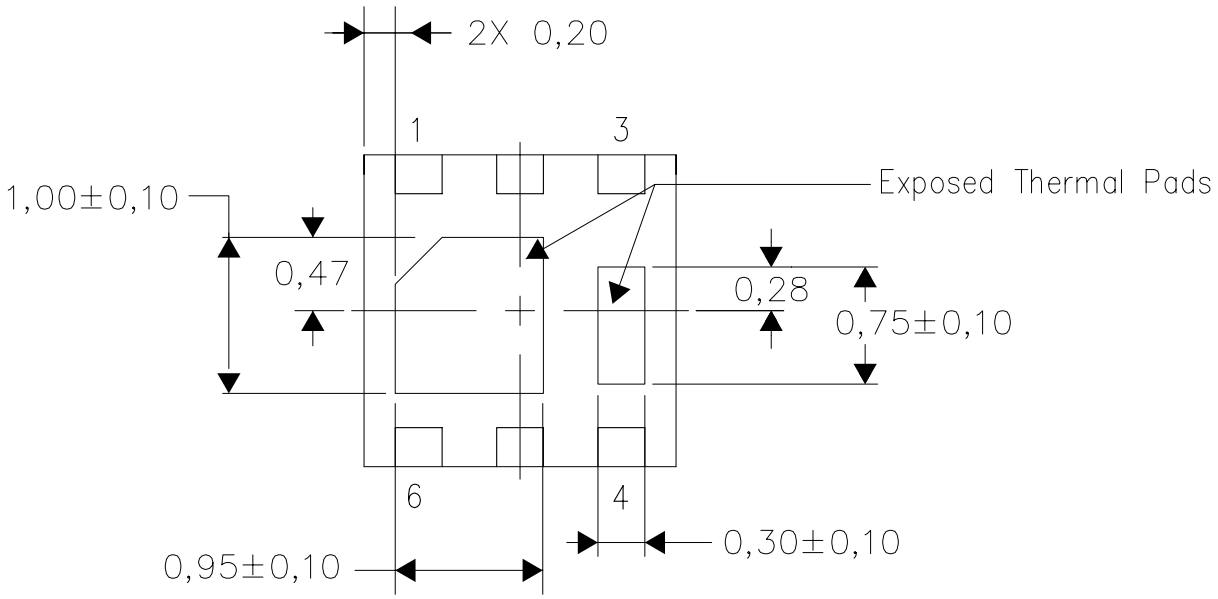
DQK (S–PWSON–N6)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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