INA21x-Q1 Automotive-Grade, Voltage Output, Low-Side or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Wide common-mode range: –0.3 V to 26 V
- Offset voltage: ±100 µV (maximum) (enables shunt drops of 10-mV full-scale)
- Accuracy:
  - Gain error:
    - ±1% (max over temperature, versions A, B)
    - ±0.5% (version C)
  - Offset drift: 0.5-µV/°C (maximum)
  - Gain drift: 10-ppm/°C (maximum)
- Choice of gain:
  - INA210-Q1: 200 V/V
  - INA211-Q1: 500 V/V
  - INA212-Q1: 1000 V/V
  - INA213-Q1: 50 V/V
  - INA214-Q1: 100 V/V
  - INA215-Q1: 75 V/V
- Quiescent current: 100 µA (maximum)
- Package: 6-pin SC70

2 Applications

- Body control module
- Valve control
- Motor control
- Electronic stability control
- Wireless charging transmitters

3 Description

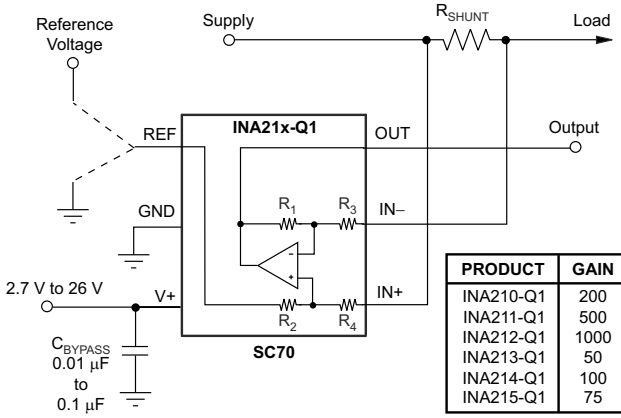
The INA21x-Q1 family of devices is a voltage-output, current-shunt monitor (also called a current-sense amplifier) that can sense drops across shunts at common-mode voltages from –0.3 V to 26 V, independent of the supply voltage. Five fixed gains are available: 50 V/V, 75 V/V, 100 V/V, 200 V/V, 500 V/V, and 1000 V/V. This family of devices is commonly used for overcurrent detection, voltage feedback control loops, or as a power monitor. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale.

The devices operate from a single 2.7-V to 26-V power supply, drawing a maximum of 100 µA of supply current. The devices are specified over the operating temperature range of –40°C to +125°C and are offered in a 6-pin SC70 package.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
INA210-Q1	SC70 (6)	2.00 mm × 1.25 mm
INA211-Q1	SC70 (6)	2.00 mm × 1.25 mm
INA212-Q1	SC70 (6)	2.00 mm × 1.25 mm
INA213-Q1	SC70 (6)	2.00 mm × 1.25 mm
INA214-Q1	SC70 (6)	2.00 mm × 1.25 mm
INA215-Q1	SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.



PRODUCT	GAIN	R_3 and R_4	R_1 and R_2
INA210-Q1	200	5 kΩ	1 MΩ
INA211-Q1	500	2 kΩ	1 MΩ
INA212-Q1	1000	1 kΩ	1 MΩ
INA213-Q1	50	20 kΩ	1 MΩ
INA214-Q1	100	10 kΩ	1 MΩ
INA215-Q1	75	13.3 kΩ	1 MΩ

$V_{OUT} = (I_{LOAD} \times R_{SHUNT})$ Gain + V_{REF}

Simplified Schematic

Table of Contents

4 Pin Configuration and Functions

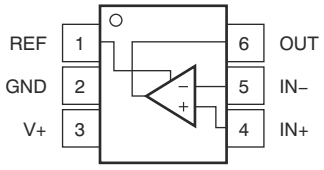


Figure 4-1. DCK Package 6-Pin SC70 Top View

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Ground
IN–	5	I	Connect to load side of shunt resistor.
IN+	4	I	Connect to supply side of shunt resistor
OUT	6	O	Output voltage
REF	1	I	Reference voltage, 0 V to V+
V+	3	—	Power supply, 2.7 V to 26 V

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage, V_S [5] [3]			28	V
Analog inputs, V_{IN+} , $V_{IN–}$ [3] [2]	Differential: $V_{DIF} = (V_{IN+}) – (V_{IN–})$	–28	28	V
	Common-mode (Version A)	GND – 0.3	28	
	Common-mode (Versions B and C)	GND – 0.1	28	V
REF input		GND – 0.3	(V_S) + 0.3	V
Output[4]		GND – 0.3	(V_S) + 0.3	V
Input current into any pin[4]			5	mA
Operating temperature		–40	125	°C
Junction temperature			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) V_{IN+} and $V_{IN–}$ are the voltages at the IN+ and IN– pins, respectively.
(3) Sustained operation between 26 V and 28 V for more than a few minutes may cause permanent damage to the device.
(4) Input voltage at any pin can exceed the voltage shown if the current at that pin is limited to 5 mA.
(5) V_S refers to the voltage at the V+ pin.

5.2 ESD Ratings

			VALUE	UNIT
INA21x-Q1 (VERSION A)				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD classification level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	
INA21x-Q1 (VERSIONS B AND C)				
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002[1] HBM ESD classification level 2	±3500	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage		12		V
V_S	Supply voltage	2.7		26	V
T_J	Junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		INA21x-Q1 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	227.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	79.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

at T_A = 25°C and $V_{SENSE} = V_{IN+} - V_{IN-}$.
INA210-Q1, INA213-Q1, INA214-Q1, and INA215-Q1: V_S = 5 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$, (unless otherwise noted)
INA211-Q1 and INA212-Q1: V_S = 12 V, V_{IN+} = 12 V, and $V_{REF} = V_S / 2$, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT							
V_{CM}	Common-mode input	Version A T_A = –40°C to 125°C		–0.3		26	V
		Versions B and C T_A = –40°C to 125°C		–0.1		26	
CMRR	Common-mode rejection ratio	V_{IN+} = 0 V to 26 V V_{SENSE} = 0 mV T_A = –40°C to 125°C	INA210-Q1 INA211-Q1 INA212-Q1 INA214-Q1 INA215-Q1	105	140		dB
			INA213-Q1	100	120		
V_{OS}	Offset voltage, RTI[1]	V_{SENSE} = 0 mV T_A = 25°C	INA210-Q1 INA211-Q1 INA212-Q1		±0.55	±35	µV
			INA213-Q1		±5	±100	
			INA214-Q1 INA215-Q1		±1	±60	
dV_{OS}/dT	Offset voltage vs temperature[3]	T_A = –40°C to 125°C			0.1	0.5	µV/°C
PSR	Offset voltage vs power supply	V_S = 2.7 V to 18 V V_{IN+} = 18 V V_{SENSE} = 0 mV T_A = 25°C			±0.1	±10	µV/V
I_B	Input bias current	V_{SENSE} = 0 mV T_A = 25°C		15	28	35	µA
I_{OS}	Input offset current	V_{SENSE} = 0 mV T_A = 25°C			±0.02		µA

5.5 Electrical Characteristics (continued)

at T_A = 25°C and V_{SENSE} = V_{IN+} – $V_{IN–}$.
INA210-Q1, INA213-Q1, INA214-Q1, and INA215-Q1: V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, (unless otherwise noted)
INA211-Q1 and INA212-Q1: V_S = 12 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
	Gain	INA210-Q1			200		V/V
		INA211-Q1			500		
		INA212-Q1			1000		
		INA213-Q1			50		
		INA214-Q1			100		
		INA215-Q1			75		
	Gain error	V_{SENSE} = –5 mV to 5 mV (Versions A and B) T_A = –40°C to 125°C			±0.02%	±1%	
		V_{SENSE} = –5 mV to 5 mV (Version C) T_A = –40°C to 125°C			±0.02%	±0.5%	
	Gain error vs temperature(3)	T_A = –40°C to 125°C			3	10	ppm/°C
	Nonlinearity error	T_A = 25°C			±0.01%		
	Maximum capacitive load	No sustained oscillation T_A = 25°C			1		nF
VOLTAGE OUTPUT							
	Output voltage swing to V+ power-supply rail(2)	R_L = 10 kΩ to GND T_A = –40°C to 125°C			(V+) – 0.05	(V+) – 0.2	V
	Output voltage swing to GND	T_A = –40°C to 125°C			(V_{GND}) + 0.005	(V_{GND}) + 0.05	V
FREQUENCY RESPONSE							
BW	Bandwidth	C_{LOAD} = 10 pF INA210-Q1	T_A = 25°C		14		kHz
		C_{LOAD} = 10 pF INA211-Q1			7		
		C_{LOAD} = 10 pF INA212-Q1			4		
		C_{LOAD} = 10 pF INA213-Q1			80		
		C_{LOAD} = 10 pF INA214-Q1			30		
		C_{LOAD} = 10 pF INA215-Q1			40		
SR	Slew rate	T_A = 25°C			0.4		V/µs
NOISE, RTI							
	Voltage noise density	RTI(1) T_A = 25°C			25		nV/√Hz
POWER SUPPLY							
I_Q	Quiescent current	V_{SENSE} = 0 mV	T_A = 25°C		65	100	µA
			T_A = –40°C to 125°C			115	

(1) RTI = referred to input.
(2) See Figure 5-10 in the *Section 5.6* section.
(3) Not production tested.

5.6 Typical Characteristics

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, (unless otherwise noted)

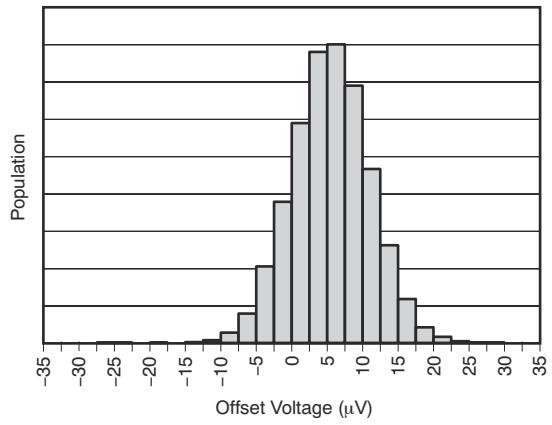


Figure 5-1. Input Offset Voltage Production Distribution

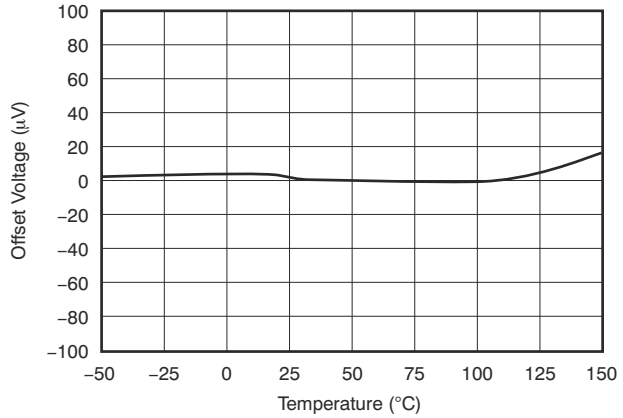


Figure 5-2. Offset Voltage vs Temperature

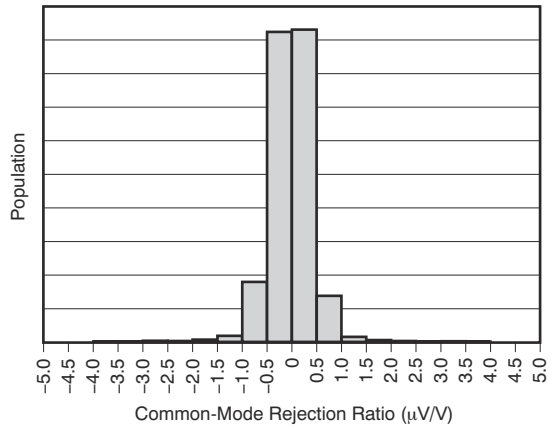


Figure 5-3. Common-Mode Rejection Production Distribution

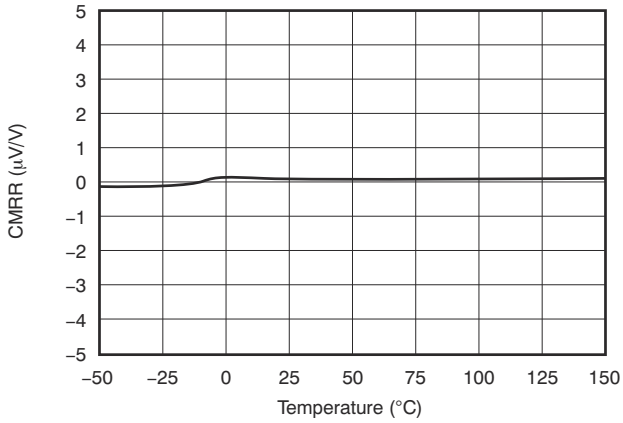


Figure 5-4. Common-Mode Rejection Ratio vs Temperature

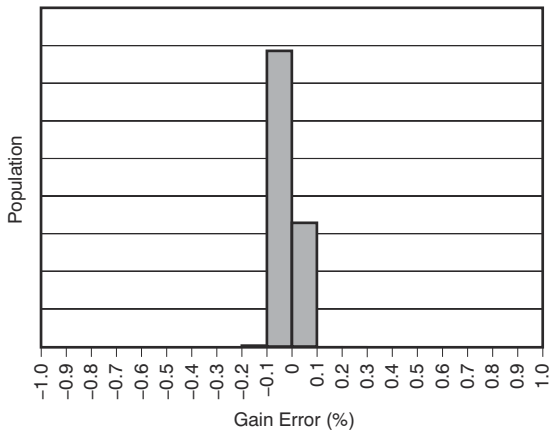
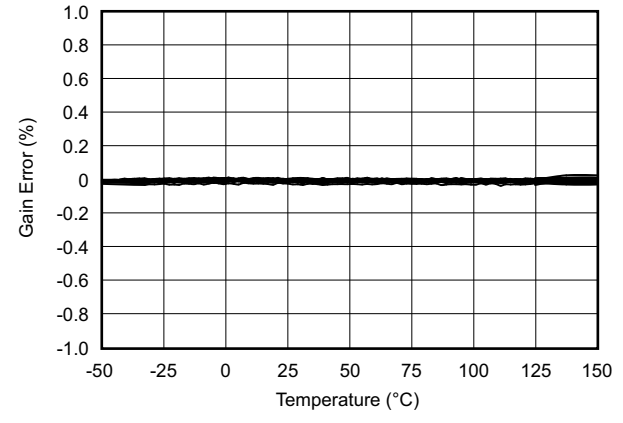


Figure 5-5. Gain Error Production Distribution

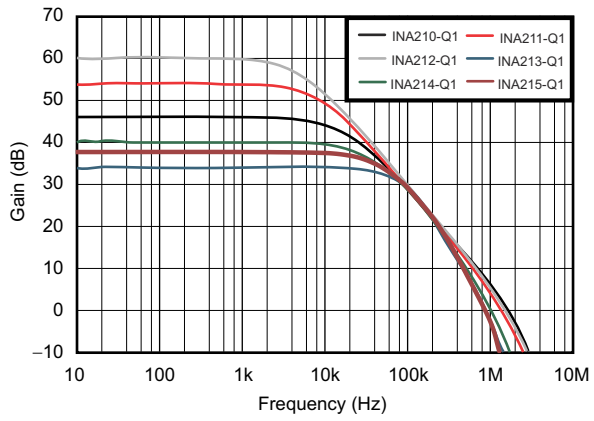


20 typical units shown

Figure 5-6. Gain Error vs Temperature

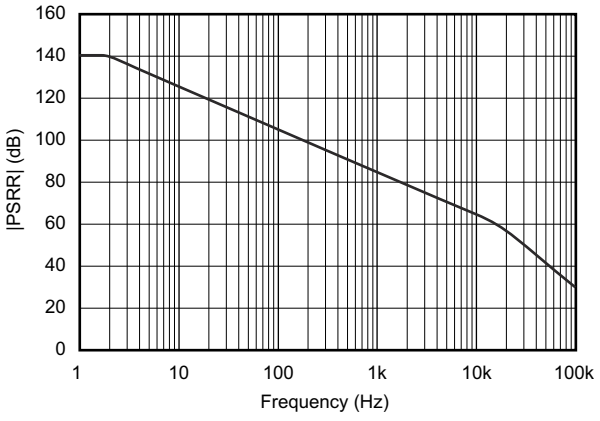
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, (unless otherwise noted)



V_{CM} = 0 V V_{DIF} = 15-mV_{PP} sine

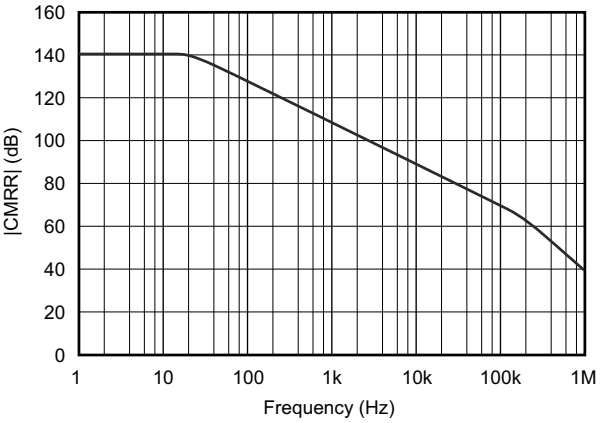
Figure 5-7. Gain vs Frequency



V_S = 5 V + 250-mV sine disturbance

V_{CM} = 0 V V_{REF} = 2.5 V V_{DIF} = shorted

Figure 5-8. Power-Supply Rejection Ratio vs Frequency



V_S = 5 V V_{CM} = 1 V sine V_{DIF} = shorted

V_{REF} = 2.5 V

Figure 5-9. Common-Mode Rejection Ratio vs Frequency

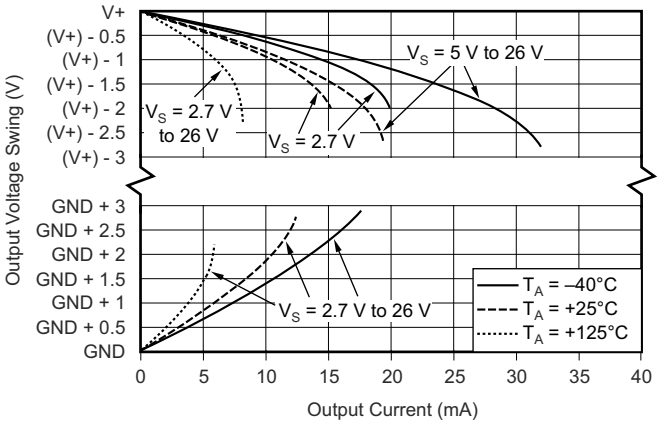


Figure 5-10. Output Voltage Swing vs Output Current

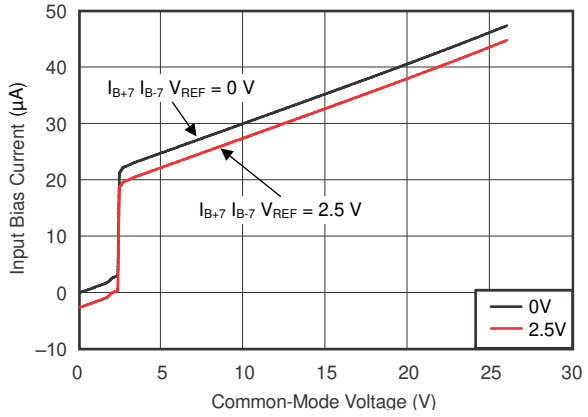


Figure 5-11. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 5 V

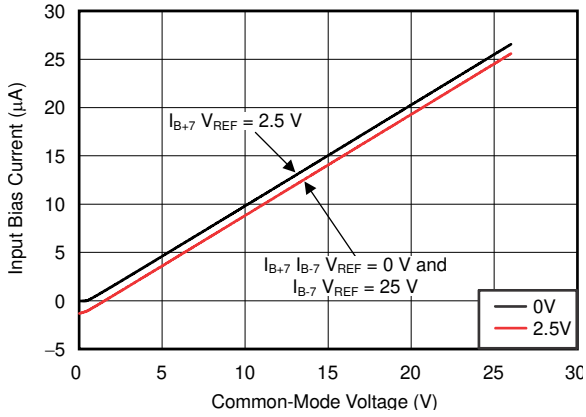


Figure 5-12. Input Bias Current vs Common-Mode Voltage With Supply Voltage = 0 V (Shutdown)

5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, (unless otherwise noted)

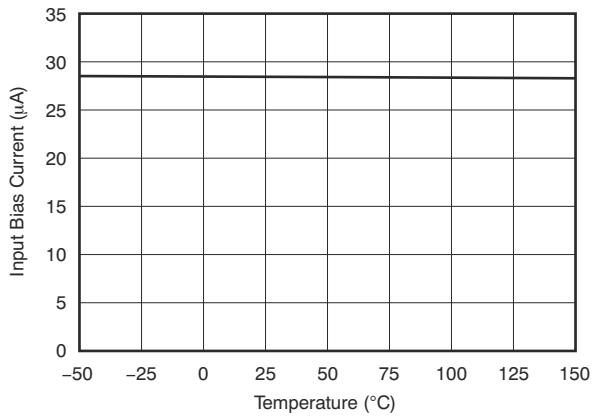


Figure 5-13. Input Bias Current vs Temperature

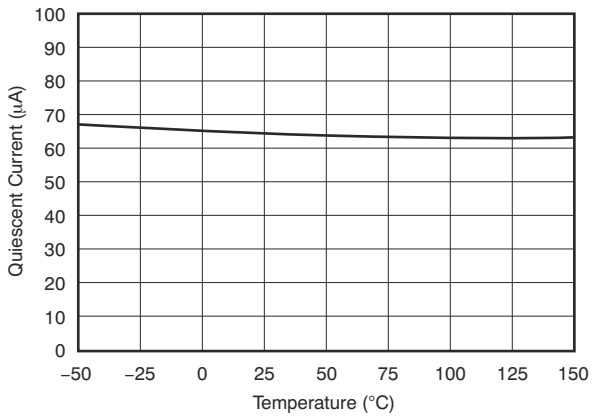
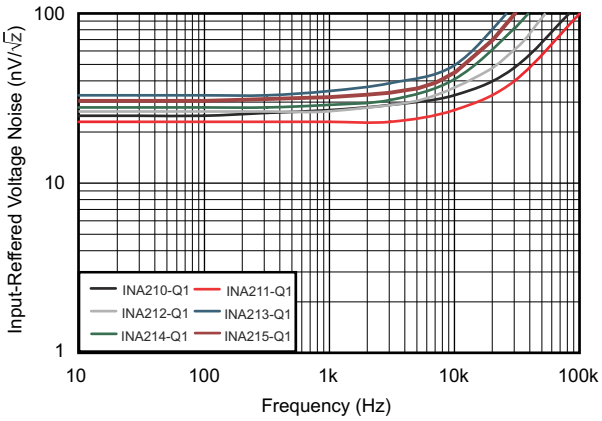
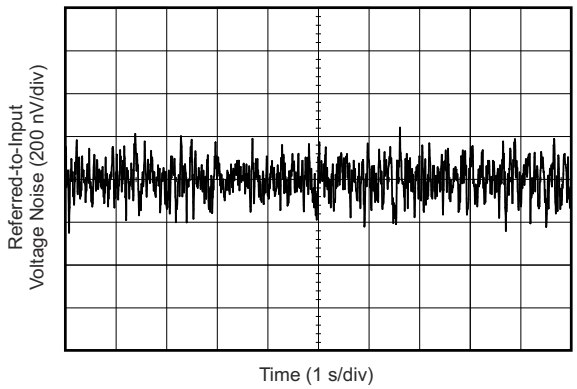


Figure 5-14. Quiescent Current vs Temperature



V_S = ±2.5 V V_{REF} = 0 V $V_{IN–}$, V_{IN+} = 0 V

Figure 5-15. Input-Referred Voltage Noise vs Frequency



V_S = ±2.5 V V_{REF} = 0 V V_{CM} = 0 V
V_{DIF} = 0 V

Figure 5-16. 0.1-Hz To 10-Hz Voltage Noise (Referred-To-Input)

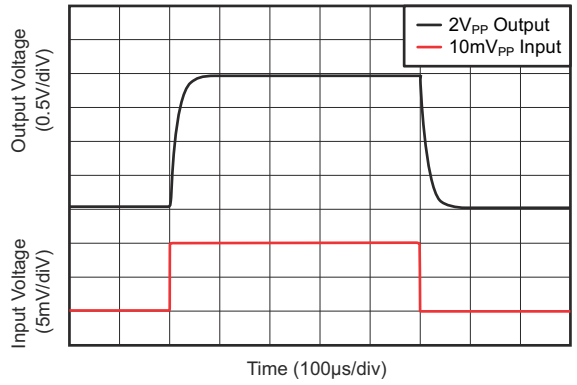


Figure 5-17. Step Response (10-mV_{PP} Input Step)

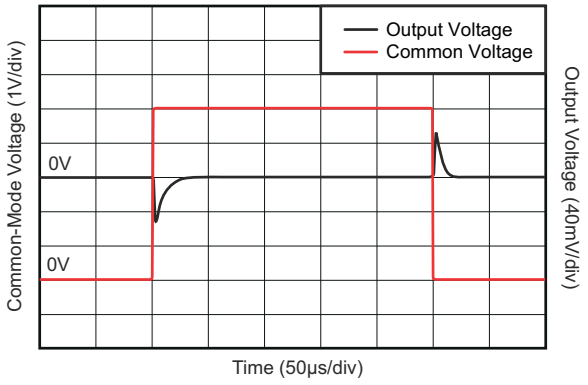
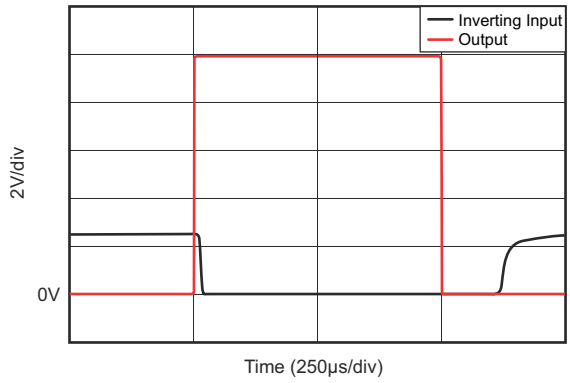


Figure 5-18. Common-Mode Voltage Transient Response

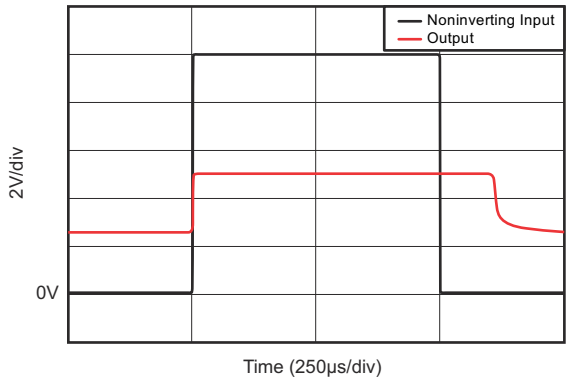
5.6 Typical Characteristics (continued)

at T_A = 25°C, V_S = 5 V, V_{IN+} = 12 V, and V_{REF} = V_S / 2, (unless otherwise noted)



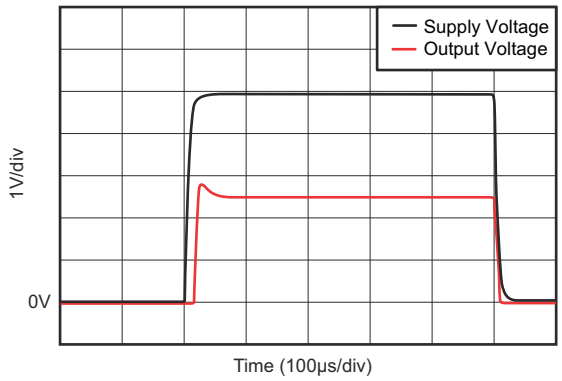
V_S = 5 V V_{REF} = 2.5 V V_{CM} = 12 V

Figure 5-19. Inverting Differential Input Overload



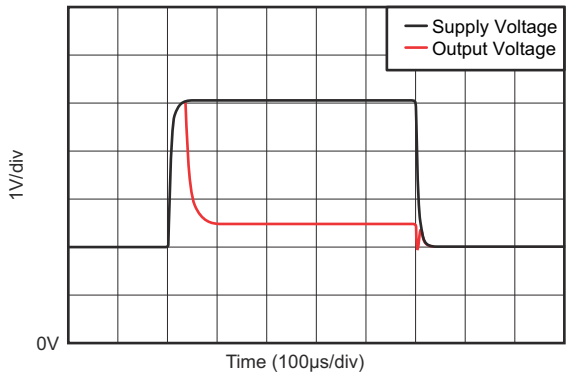
V_S = 5 V V_{REF} = 2.5 V V_{CM} = 12 V

Figure 5-20. Noninverting Differential Input Overload



V_S = 5 V V_{REF} = 2.5 V 1-kHz step with V_{DIF} = 0 V

Figure 5-21. Start-Up Response



V_S = 5 V V_{REF} = 2.5 V 1-kHz step with V_{DIF} = 0 V

Figure 5-22. Brownout Recovery

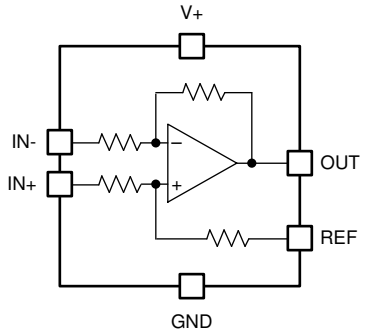
6 Detailed Description

6.1 Overview

The INA210-Q1 to INA215-Q1 are 26-V, common-mode, zero-drift topology, current-sensing amplifiers that can be used in both low-side and high-side configurations. These specially-designed, current-sensing amplifiers are able to accurately measure voltages developed across current-sensing resistors on common-mode voltages that far exceed the supply voltage powering the device. Current can be measured on input voltage rails as high as 26 V and the device can be powered from supply voltages as low as 2.7 V.

The zero-drift topology enables high-precision measurements with maximum input offset voltages as low as 35 µV with a maximum temperature contribution of 0.5 µV/°C over the full temperature range of –40°C to 125°C.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Basic Connections

Figure 6-1 shows the basic connections of the INA210-Q1 to INA215-Q1. Connect the input pins (IN+ and IN–) as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistor.

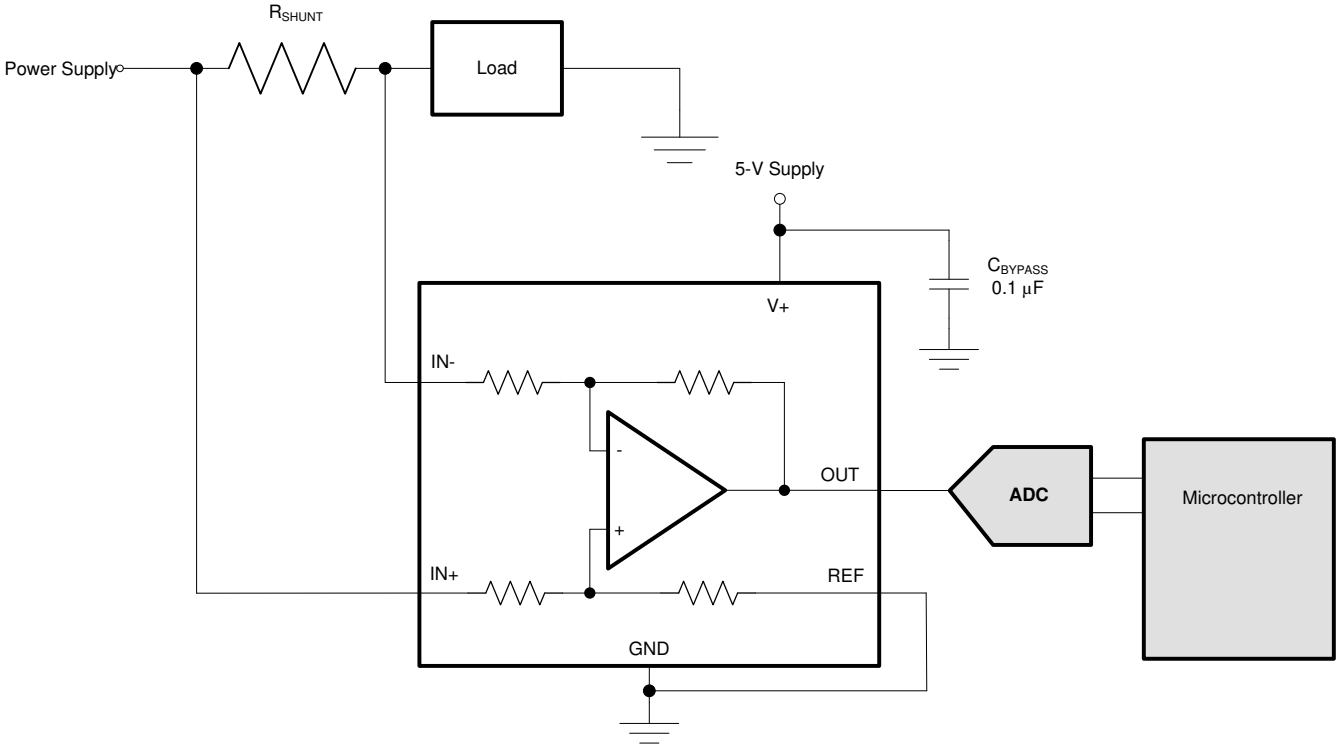


Figure 6-1. Typical Application

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies can require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

6.3.2 Selecting R_S

The zero-drift offset performance of the INA21x-Q1 family of devices offers several benefits. In general, the primary advantage of the low offset characteristic enables lower full-scale drops across the shunt. For example, non-zero-drift current-shunt monitors typically require a full-scale range of 100 mV.

The INA21x-Q1 family of devices provides equivalent accuracy at a full-scale range on the order of 10 mV. This accuracy reduces shunt dissipation by an order of magnitude with many additional benefits.

Alternatively, some applications must measure current over a wide dynamic range and can take advantage of the low offset on the low end of the measurement. Most often, these applications can use the lower-gain INA213-Q1, INA214-Q1, or INA215-Q1 to accommodate larger shunt drops on the upper end of the scale. For instance, an INA213-Q1 device operating on a 3.3-V supply can easily support a full-scale shunt drop of 60 mV, with only 100 µV of offset.

6.4 Device Functional Modes

6.4.1 Input Filtering

An obvious and straightforward location for filtering is at the output of the INA21x-Q1 family of devices. However, this location negates the advantage of the low output impedance of the internal buffer. The only other filtering option is at the input pins of the INA21x-Q1 family of devices. This location, however, requires consideration of the ±30% tolerance of the internal resistances. Figure 6-2 shows a filter placed at the input pins.

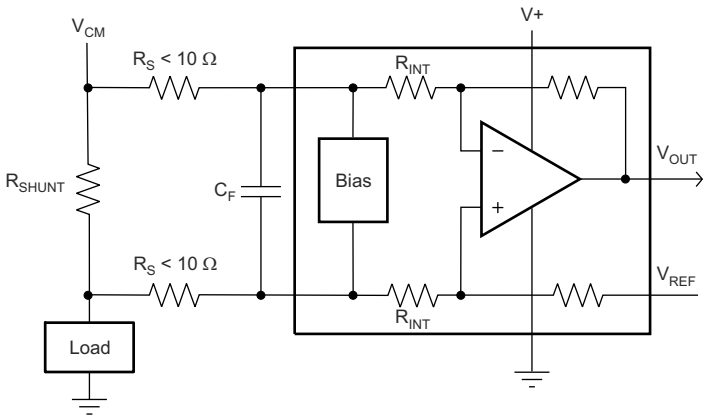


Figure 6-2. Filter at Input Pins

The addition of external series resistance, however, creates an additional error in the measurement so the value of these series resistors must be kept to 10 Ω (or less, if possible) to reduce impact to accuracy. The internal bias network shown in Figure 6-2 that is present at the input pins creates a mismatch in input bias currents when a differential voltage is applied between the input pins. If additional external series filter resistors are added to the circuit, the mismatch in bias currents results in a mismatch of voltage drops across the filter resistors. This mismatch creates a differential error voltage that subtracts from the voltage developed at the shunt resistor. This error results in a voltage at the device input pins that is different than the voltage developed across the shunt resistor. Without the additional series resistance, the mismatch in input bias currents has little effect on device operation. The amount of error these external filter resistors add to the measurement can be calculated using Equation 2 where the gain error factor is calculated using Equation 1.

The amount of variance in the differential voltage present at the device input relative to the voltage developed at the shunt resistor is based both on the external series resistance value as well as the internal input resistors, R_3 and R_4 (or R_{INT} as shown in Figure 6-2). The reduction of the shunt voltage reaching the device input pins appears as a gain error when comparing the output voltage relative to the voltage across the shunt resistor. A factor can be calculated to determine the amount of gain error that is introduced by the addition of external series resistance. Use Equation 1 to calculate the expected deviation from the shunt voltage to what is measured at the device input pins.

$$\text{Gain Error Factor} = \frac{(1250 \times R_{INT})}{(1250 \times R_S) + (1250 \times R_{INT}) + (R_S \times R_{INT})} \quad (1)$$

where:

- R_{INT} is the internal input resistor (R_3 and R_4), and
- R_S is the external series resistance.

With the adjustment factor from Equation 1 including the device internal input resistance, this factor varies with each gain version, as shown in Table 6-1. Table 6-2 lists each individual device gain-error factor.

Table 6-1. Input Resistance

PRODUCT	GAIN	R_{INT} (kΩ)
INA210-Q1	200	5
INA211-Q1	500	2
INA212-Q1	1000	1
INA213-Q1	50	20
INA214-Q1	100	10
INA215-Q1	75	13.3

Table 6-2. Device Gain Error Factor

PRODUCT	SIMPLIFIED GAIN ERROR FACTOR
INA210-Q1	$\frac{1000}{R_S + 1000}$
INA211-Q1	$\frac{10{,}000}{(13 \times R_S) + 10{,}000}$
INA212-Q1	$\frac{5000}{(9 \times R_S) + 5000}$
INA213-Q1	$\frac{20{,}000}{(17 \times R_S) + 20{,}000}$
INA214-Q1	$\frac{10{,}000}{(9 \times R_S) + 10{,}000}$
INA215-Q1	$\frac{8{,}000}{(7 \times R_S) + 8{,}000}$

Use Equation 2 to calculate the gain error that can be expected from the addition of the external series resistors.

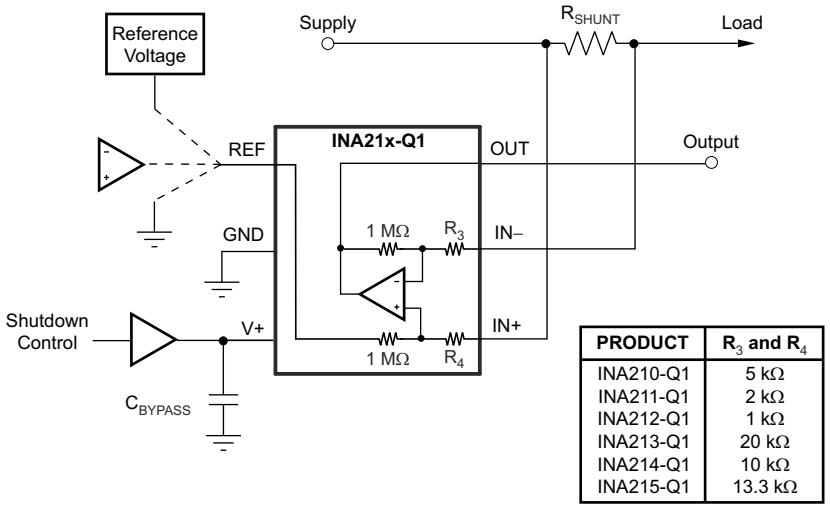
$$\text{Gain Error (\%)} = 100 - (100 \times \text{Gain Error Factor}) \quad (2)$$

For example, using an INA212-Q1 device and the corresponding gain error equation from Table 6-2, a series resistance of 10 Ω results in a gain error factor of 0.982. The corresponding gain error is then calculated using Equation 2, resulting in a gain error of approximately 1.77% solely because of the external 10-Ω series resistors. Using an INA213-Q1 with the same 10-Ω series resistor results in a gain error factor of 0.991 and a gain error of 0.84% again solely because of these external resistors.

6.4.2 Shutting Down the INA21x-Q1 Series

While the INA21x-Q1 family of devices does not have a shutdown pin, the low-power consumption of the device allows the output of a logic gate or transistor switch to power the device. This gate or switch turns on and turns off the INA21x-Q1 power-supply quiescent current.

However, in current-shunt monitoring applications, the amount of current drained from the shunt circuit in shutdown conditions must be considered. Evaluating this current drain involves considering the simplified schematic of the INA21x-Q1 family of devices in shutdown mode shown in Figure 6-3.



PRODUCT	R_3 and R_4
INA210-Q1	5 kΩ
INA211-Q1	2 kΩ
INA212-Q1	1 kΩ
INA213-Q1	20 kΩ
INA214-Q1	10 kΩ
INA215-Q1	13.3 kΩ

1-MΩ paths from shunt inputs to reference and INA21x-Q1 outputs.

Figure 6-3. Basic Circuit for Shutting Down INA21x-Q1 With a Grounded Reference

Slightly more than a 1-MΩ impedance (from the combination of 1-MΩ feedback and 5-kΩ input resistors) exists from each input of the INA21x-Q1 family of devices to the OUT pin and to the REF pin. The amount of current flowing through these pins depends on the respective ultimate connection. For example, if the REF pin is grounded, the calculation of the effect of the 1-MΩ impedance from the shunt to ground is straightforward. However, if the reference or operational amplifier (op amp) is powered when the INA21x-Q1 family of devices is shut down, the calculation is direct. Instead of assuming 1 MΩ to ground, however, assume 1 MΩ to the reference voltage. If the reference or op amp is also shut down, some knowledge of the reference or op amp output impedance under shutdown conditions is required. For instance, if the reference source behaves as an open circuit when not powered, little or no current flows through the 1-MΩ path.

Regarding the 1-MΩ path to the output pin, the output stage of a disabled INA21x-Q1 device does constitute a good path to ground; consequently, this current is directly proportional to a shunt common-mode voltage present across a 1-MΩ resistor.

Note

When the device is powered up, an additional, nearly constant and well-matched 25-µA current flows in each of the inputs as long as the shunt common-mode voltage is 3 V or higher. Below 2-V common-mode, the only current effects are the result of the 1-MΩ resistors.

6.4.3 REF Input Impedance Effects

As with any difference amplifier, the INA21x-Q1 common-mode rejection ratio is affected by any impedance present at the REF input. This concern is not a problem when the REF pin is connected directly to most references or power supplies. When using resistive dividers from the power supply or a reference voltage, buffer the REF pin by an op amp.

In systems where the INA21x-Q1 output can be sensed differentially, such as by a differential input analog-to-digital converter (ADC) or by using two separate ADC inputs, the effects of external impedance on the REF input can be cancelled. Figure 6-4 shows a method of taking the output from the INA21x-Q1 family of devices by using the REF pin as a reference.

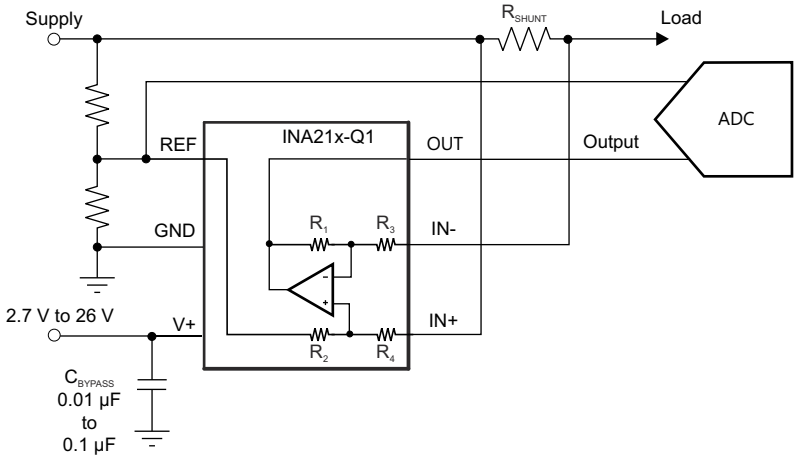


Figure 6-4. Sensing INA21x-Q1 to Cancel Effects of Impedance on the REF Input

6.4.4 Using the INA21x-Q1 with Common-Mode Transients Above 26 V

With a small amount of additional circuitry, the INA21x-Q1 family of devices can be used in circuits subject to transients higher than 26 V, such as automotive applications. Use only Zener diode or Zener-type transient absorbers (sometimes referred to as *transzorbs*)—any other type of transient absorber has an unacceptable time delay. Begin by adding a pair of resistors as a working impedance for the Zener diode, as shown in Figure 6-5. Keeping these resistors as small as possible is preferable, typically around 10 Ω. Larger values can be used with an effect on gain that is discussed in the *Section 6.4.1* section. Because this circuit limits only short-term transients, many applications are satisfied with a 10-Ω resistor along with conventional Zener diodes of the lowest power rating that can be found. This combination uses the least amount of board space. These diodes can be found in packages as small as SOT-523 or SOD-523.

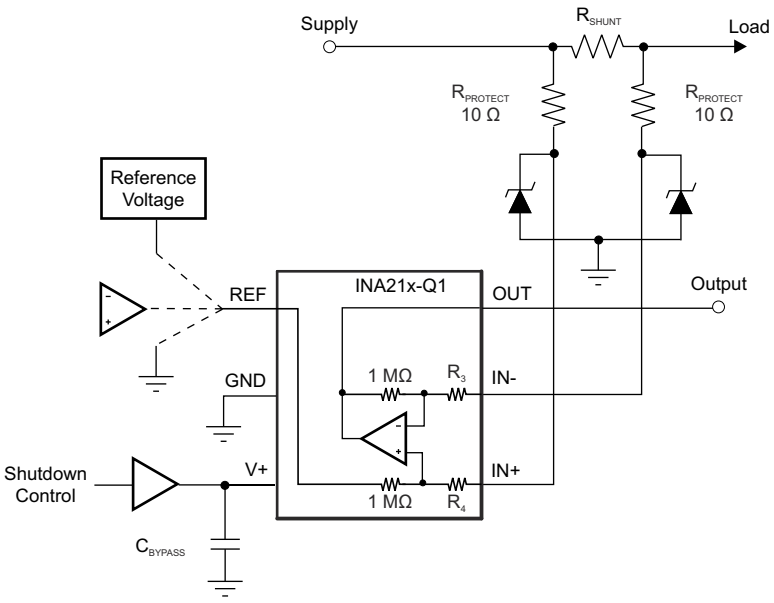


Figure 6-5. INA21x-Q1 Transient Protection Using Dual Zener Diodes

In the event that low-power Zener diodes do not have sufficient transient absorption capability and a higher power transzorb must be used, the most package-efficient solution then involves using a single transzorb and back-to-back diodes between the device inputs. The most space-efficient solutions are dual series-connected diodes in a single SOT-523 or SOD-523 package. Figure 6-6 shows this method. In either of these examples, the total board area required by the INA21x-Q1 family of devices with all protective components is less than that of an SO-8 package, and only slightly greater than that of an MSOP-8 package.

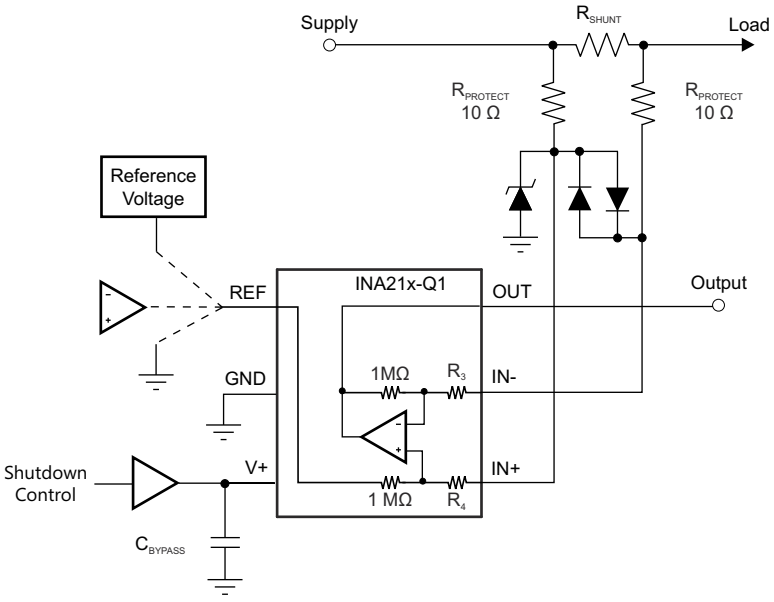


Figure 6-6. INA21x-Q1 Transient Protection Using a Single Transzorb and Input Clamps

6.4.5 Improving Transient Robustness

CAUTION

Applications involving large input transients with excessive dV/dt above 2 kV per microsecond present at the device input pins can cause damage to the internal ESD structures on version A devices.

The potential damage from large input transients is a result of the internal latching of the ESD structure to ground when this transient occurs at the input. With significant current available in most current-sensing applications, the large current flowing through the input transient-triggered, ground-shorted ESD structure quickly results in damage to the silicon. External filtering can be used to attenuate the transient signal prior to reaching the inputs to avoid the latching condition. Care must be taken to ensure that external series input resistance does not significantly impact gain error accuracy. For accuracy purposes, keep these resistances under 10 Ω if possible. Ferrite beads are recommended for this filter because of the inherently low-dc ohmic value. Ferrite beads with less than 10 Ω of resistance at dc and over 600 Ω of resistance at 100 MHz to 200 MHz are recommended. The recommended capacitor values for this filter are between 0.01 µF and 0.1 µF to ensure adequate attenuation in the high-frequency region. Figure 6-7 illustrates this protection scheme.

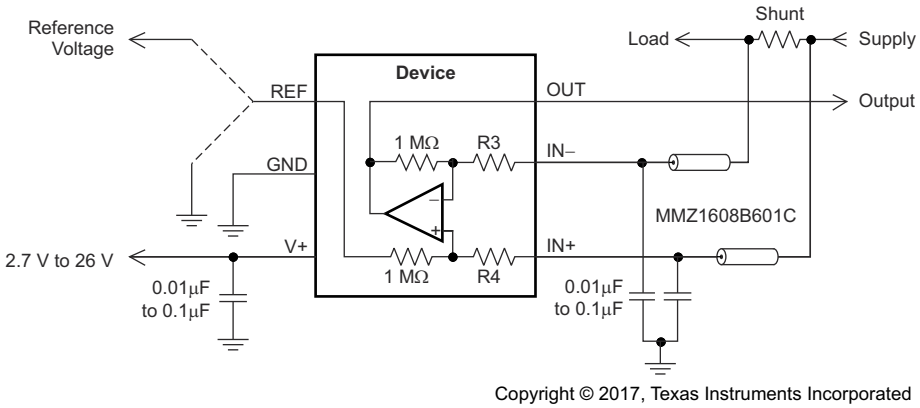


Figure 6-7. Transient Protection

To minimize the cost of adding these external components to protect the device in applications where large transient signals may be present, version B and C devices are now available with new ESD structures that are not susceptible to this latching condition. Version B and C devices are incapable of sustaining these damage-causing latched conditions so they do not have the same sensitivity to the transients that the version A devices have, thus making the version B and C devices a better fit for these applications.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Application Information

The INA21x-Q1 family of devices measure the voltage developed across a current-sensing resistor when current passes through the resistor. The ability to drive the reference pin to adjust the functionality of the output signal offers multiple configurations, as discussed throughout the *Section 7.2* section.

7.2 Typical Applications

7.2.1 Unidirectional Operation

Unidirectional operation allows the INA21x-Q1 family of devices to measure currents through a resistive shunt in one direction. The most frequent case of unidirectional operation sets the output at ground by connecting the REF pin to ground. In unidirectional applications where the highest possible accuracy is desirable at very low inputs, bias the REF pin to a convenient value above 50 mV to get the device output swing into the linear range for zero inputs.

A less frequent case of unipolar output biasing is to bias the output by connecting the REF pin to the supply. In this case, the quiescent output for zero input is at quiescent supply. This configuration only responds to negative currents (inverted voltage polarity at the device input).

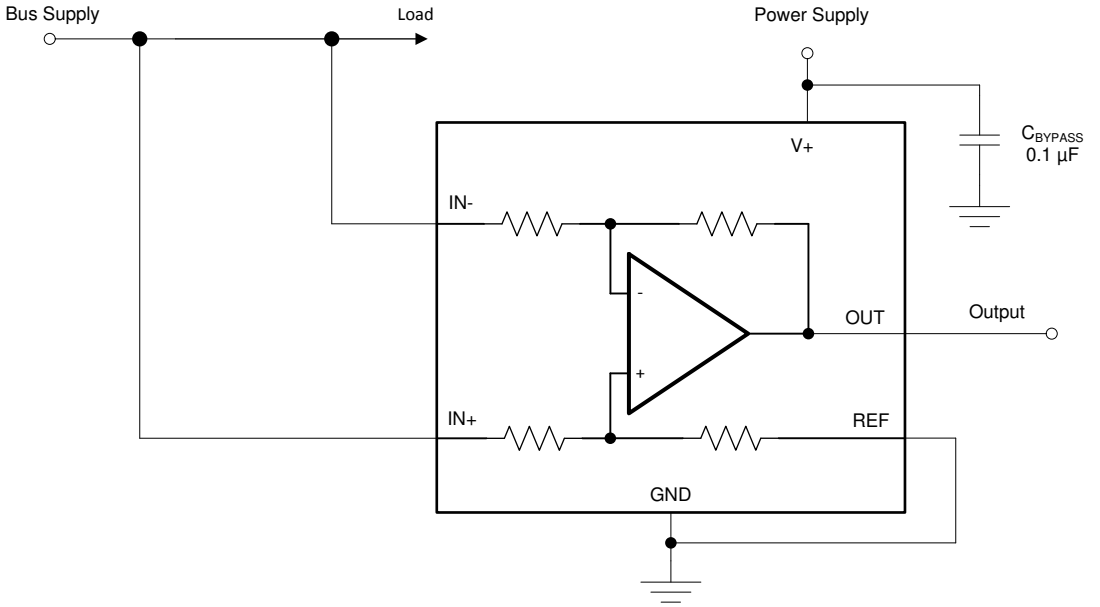


Figure 7-1. Unidirectional Application Schematic

7.2.1.1 Design Requirements

The device can be configured to monitor current flowing in one direction (unidirectional) or in both directions (bidirectional) depending on how the REF pin is configured. The most common case is unidirectional where the output is set to ground when no current is flowing by connecting the REF pin to ground, as shown in Figure 7-1. When the input signal increases, the output voltage at the OUT pin increases.

7.2.1.2 Detailed Design Procedure

The linear range of the output stage is limited in how close the output voltage can approach ground under zero input conditions. In unidirectional applications where measuring very-low input currents is desirable, bias the REF pin to a convenient value above 50 mV to get the output into the linear range of the device. To limit common-mode rejection errors, TI recommends buffering the reference voltage connected to the REF pin.

A less frequently-used output biasing method is to connect the REF pin to the supply voltage, V+. This method results in the output voltage saturating at 200 mV below the supply voltage when no differential input signal is present. This method is similar to the output-saturated low condition with no input signal when the REF pin is connected to ground. The output voltage in this configuration only responds to negative currents that develop negative differential input voltage relative to the device IN– pin. Under these conditions, when the differential input signal increases negatively, the output voltage moves downward from the saturated supply voltage. The voltage applied to the REF pin must not exceed the device supply voltage.

7.2.1.3 Application Curve

Figure 7-2 shows an example output response of a unidirectional configuration. With the REF pin connected directly to ground, the output voltage is biased to this zero output level. The output rises above the reference voltage for positive differential input signals but cannot fall below the reference voltage for negative differential input signals because of the grounded reference voltage.

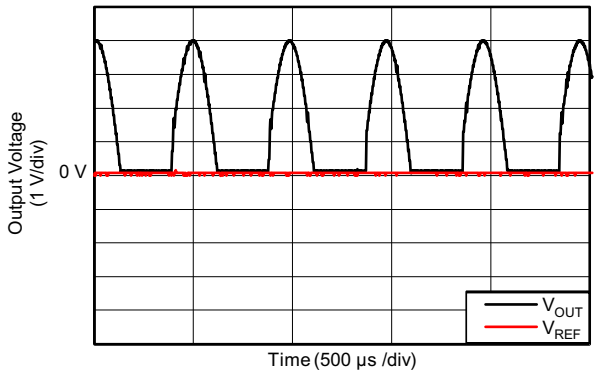


Figure 7-2. Unidirectional Application Output Response

7.2.2 Bidirectional Operation

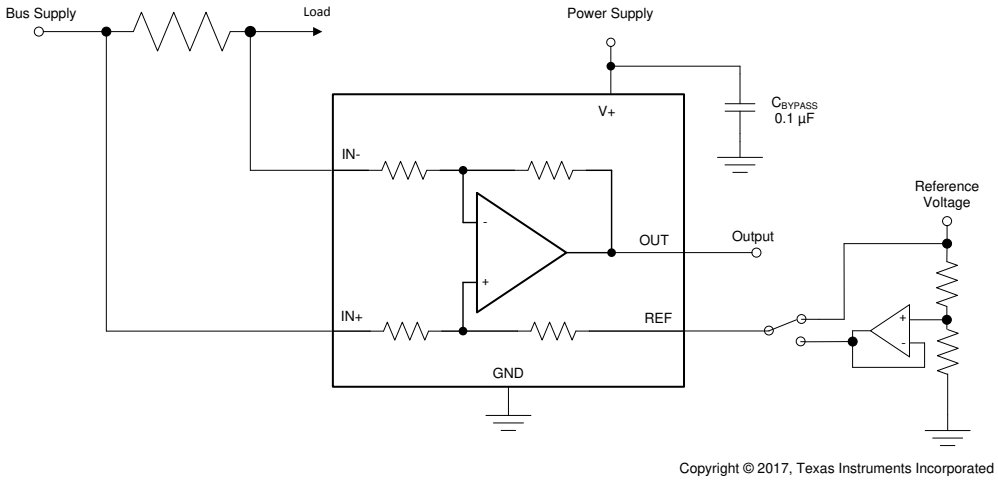


Figure 7-3. Bidirectional Application Schematic

7.2.2.1 Design Requirements

The device is a bidirectional, current-sense amplifier capable of measuring currents through a resistive shunt in two directions. This bidirectional monitoring is common in applications that include charging and discharging operations where the current flow-through resistor can change directions.

7.2.2.2 Detailed Design Procedure

The ability to measure this current flowing in both directions is enabled by applying a voltage to the REF pin, as shown in Figure 7-3. The voltage applied to REF (V_{REF}) sets the output state that corresponds to the zero-input level state. The output then responds by increasing above the V_{REF} value for positive differential signals (relative to the IN– pin) and responds by decreasing below the V_{REF} value for negative differential signals. This reference voltage applied to the REF pin can be set anywhere between 0 V to V+. For bidirectional applications, the V_{REF} value is typically set at mid-scale for equal signal range in both current directions. In some cases, however, the V_{REF} value is set at a voltage other than mid-scale when the bidirectional current and corresponding output signal are note required to be symmetrical.

7.2.2.3 Application Curve

Figure 7-4 shows an example output response of a bidirectional configuration. With the REF pin connected to a reference voltage, 2.5 V in this case, the output voltage is biased upwards by this reference level. The output rises above the reference voltage for positive differential input signals and falls below the reference voltage for negative differential input signals.

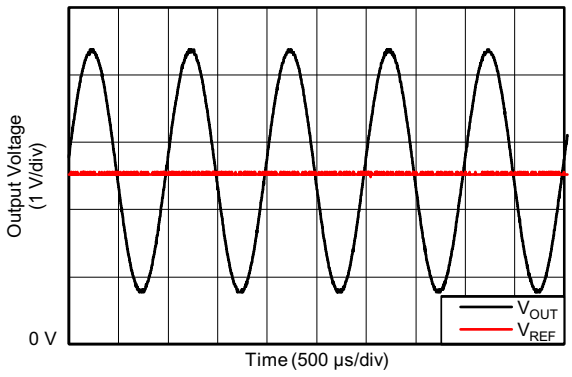


Figure 7-4. Bidirectional Application Output Response

8 Power Supply Recommendations

The input circuitry of the INA21x-Q1 family of devices can accurately measure beyond the power-supply voltage, V+. For example, the V+ power supply can be 5 V, whereas the load power-supply voltage can be as high as 26 V. However, the output voltage range of the OUT pin is limited by the voltages on the power-supply pin. The INA21x-Q1 family of devices can withstand the full input-signal range up to 26 V at the input pins, regardless of whether the device has power applied or not.

9 Layout

9.1 Layout Guidelines

- Connect the input pins to the sensing resistor using a Kelvin or 4-wire connection. This connection technique ensures that only the current-sensing resistor impedance is detected between the input pins. Poor routing of the current-sensing resistor commonly results in additional resistance present between the input pins. Given the very-low ohmic value of the current resistor, any additional high-current carrying impedance can cause significant measurement errors.
- Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 µF. Additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies.

9.2 Layout Example

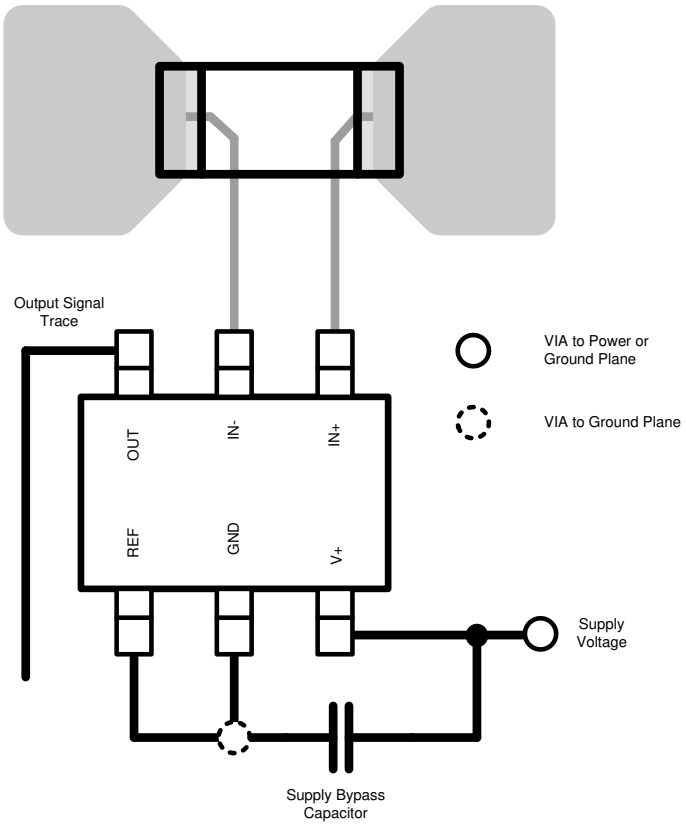


Figure 9-1. Recommended Layout

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

INA210-215EVM user's guide

10.2 Related Links

Table 10-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA210-Q1	Click here	Click here	Click here	Click here	Click here
INA211-Q1	Click here	Click here	Click here	Click here	Click here
INA212-Q1	Click here	Click here	Click here	Click here	Click here
INA213-Q1	Click here	Click here	Click here	Click here	Click here
INA214-Q1	Click here	Click here	Click here	Click here	Click here
INA215-Q1	Click here	Click here	Click here	Click here	Click here

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision J (April 2020) to Revision K (October 2023) **Page**

- Updated format to match new TI layout and flow. Tables, figures and cross-references use a new numbering sequence throughout the document ... 1

Changes from Revision I (August 2019) to Revision J (April 2020) **Page**

- Added Functional Safety-Capable information ... 1

Changes from Revision H (September 2017) to Revision I (August 2019) **Page**

- Changed V_S and V_{IN} maximum values from 26 V to 28 V in *Absolute Maximum Ratings* table ... 4
- Changed differential V_{IN} minimum value from –26 V to –28 V in *Absolute Maximum Ratings* table ... 4
- Added new Note 3 with caution regarding operation between 26 V and 28 V ... 4

Changes from Revision G (May 2016) to Revision H (September 2017) **Page**

- Deleted *Device Options* table ... 3
- Added V_{DIF} to analog input parameter in *Absolute Maximum Ratings* table ... 4
- Added V_S table note in *Absolute Maximum Ratings* table ... 4
- Changed formatting of *Thermal Information* table note ... 5
- Deleted first table note in *Electrical Characteristics* table ... 5
- Added version C to input test conditions in *Electrical Characteristics* table ... 5
- Added version C test conditions to gain error parameter in *Electrical Characteristics* table ... 5
- Changed Figure 5-7, Figure 5-10 , Figure 5-15, Figure 5-17, Figure 5-18, Figure 5-19, Figure 5-20 , Figure 5-21 and Figure 5-22 to match commercial data sheet ... 7
- Added test conditions to Figure 5-8, Figure 5-9, Figure 5-10, and Figure 5-11 and Figure 5-12 from INA21x commercial data sheet ... 7
- Changed x-axis unit in Figure 5-17 from "ms" to "µs" ... 7

Changes from Revision F (April 2016) to Revision G (May 2016) **Page**

- Released INA210-Q1, INA211-Q1, and INA215-Q1 to production ... 1
- Deleted second footnote from *Device Information* table ... 1

Changes from Revision E (December 2014) to Revision F (February 2015) **Page**

- Changed *Choice of Gain* Features bullet: added INA210-Q1, INA211-Q1, and INA215-Q1 sub-bullets, deleted A from INA213-Q1 1
- Changed *Device Information* table: added INA210-Q1, INA211-Q1, INA215-Q1 rows, deleted A from INA213A-Q1, changed package term from SOT to SC70 1
- Changed first Features bullet 1
- Changed first paragraph of Description section 1
- Changed Simplified Schematic: changed figure table 1
- Deleted footnote 1 from *Pin Functions* table 3
- Changed *Absolute Maximum Ratings* operating temperature from –55°C to 150°C to –40°C to 125°C 4
- Changed Changed *ESD Ratings* table: changed title, made CDM values all one row because corner pins and all other pins tested the same, added separation of specs for versions A and B, and moved the storage temperature to *Absolute Maximum Ratings* table; added version B devices 4
- Changed *Electrical Characteristics* table: changed conditions and changed all INA213A-Q1 to INA213-Q1 5
- Changed Input, V_{CM} parameter in *Electrical Characteristics* table 5
- Changed Input, *CMRR* and V_{OS} parameters in *Electrical Characteristics* table 5
- Changed Output, *Gain* parameter in *Electrical Characteristics* table 5
- Deleted test conditions from Output, *Nonlinearity error* parameter in *Electrical Characteristics* table 5
- Changed Frequency Response, *BW* parameter in *Electrical Characteristics* table 5
- Changed conditions of *Typical Characteristics* section 7
- Changed Figure 7 7
- Changed Figure 15 7
- Changed first sentence of *Overview* section 11
- Changed first sentence of *Basic Connections* section 12
- Changed last paragraph of *Selecting* R_S section 12
- Changed Table 1 and Table 2 13
- Changed Figure 25 15
- Changed *Improving Transient Robustness* section: changed first paragraph, added caution and last paragraph 18

Changes from Revision D (October 2013) to Revision E (October 2014) **Page**

- Added *Handling Rating* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 4
- Deleted θ_{JA} thermal resistance parameter from *Electrical Characteristics* 5

Changes from Revision C (August 2013) to Revision D (October 2013) **Page**

- Changed INA213-Q1 device to INA213A-Q1 device throughout document 1
- Deleted T_A, Operating Temperature from *ABSOLUTE MAXIMUM RATINGS* table 4

Changes from Revision B (June 2010) to Revision C (July 2013) **Page**

- Changed device names to -Q1 throughout....1
- Added INA212-Q1: 1000 V/V to Features....1
- Changed Applications bullets to be all automotive specific....1
- Added INA212-Q1 offers a fixed gain of 1000 V/V to Description....1
- Added INA212-Q1 to image....1
- Deleted Ordering Information table....4
- Changed HBM to 2000 V, removed MM....4
- Changed T_A to -40 to 125°C....4
- Added INA212-Q1 values to CMRR V_{OS} and Gain in Electrical Characteristics table....5
- Changed Bandwidth parameter in the *ELECTRICAL CHARACTERISTICS* to differentiate between devices....5
- Changed *GAIN vs FREQUENCY* graph to show difference between devices....7
- Added INA212-Q1 device name in App Information....12
- Added INA212-Q1 to image....15

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA210BQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13F	Samples
INA210CQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17D	Samples
INA211BQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13G	Samples
INA211CQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17E	Samples
INA212AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJW	Samples
INA212BQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13H	Samples
INA212CQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17F	Samples
INA213AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OBX	Samples
INA213BQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13I	Samples
INA213CQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17G	Samples
INA214AQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OFT	Samples
INA214BQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	13J	Samples
INA214CQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17H	Samples
INA215BQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	13K	Samples
INA215CQDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	17I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF INA210-Q1, INA211-Q1, INA212-Q1, INA213-Q1, INA214-Q1, INA215-Q1 :

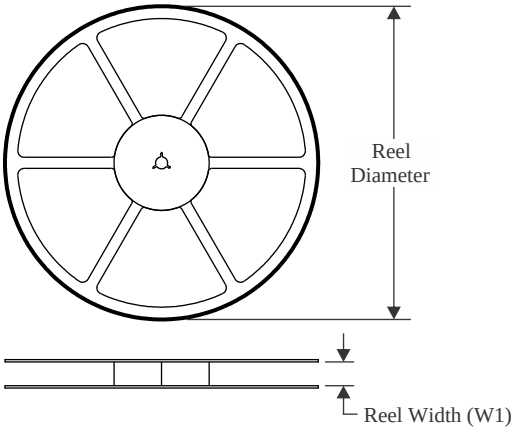
- Catalog : INA210, INA211, INA212, INA213, INA214, INA215

NOTE: Qualified Version Definitions:

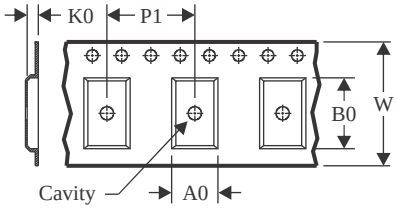
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

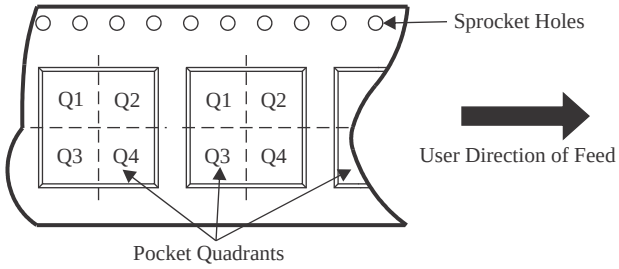


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

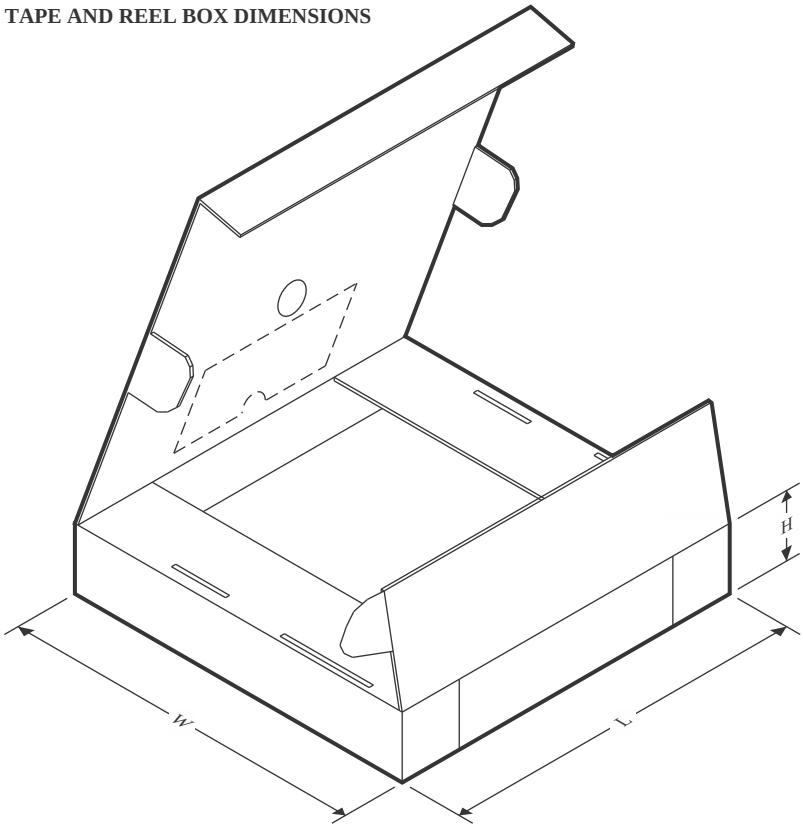
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA210BQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA210CQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211BQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA211CQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212AQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212BQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA212CQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213AQDCKRQ1	SC70	DCK	6	3000	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
INA213AQDCKRQ1	SC70	DCK	6	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
INA213BQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA213CQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214AQDCKRQ1	SC70	DCK	6	3000	178.0	8.4	2.4	2.5	1.2	4.0	8.0	Q3
INA214BQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA214CQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215BQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
INA215CQDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

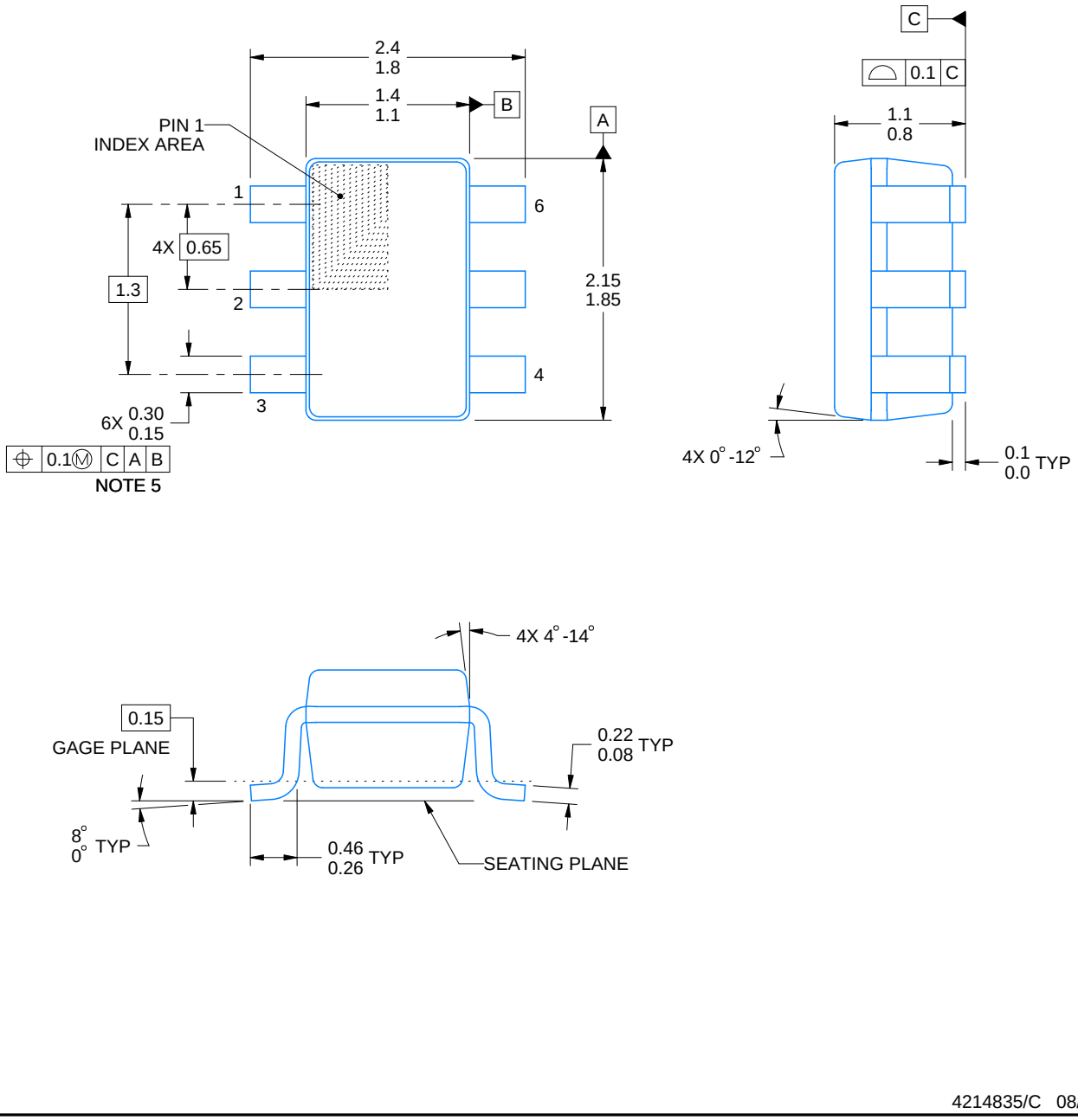
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA210BQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA210CQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA211BQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA211CQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA212AQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA212BQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA212CQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA213AQDCKRQ1	SC70	DCK	6	3000	340.0	340.0	38.0
INA213AQDCKRQ1	SC70	DCK	6	3000	213.0	191.0	35.0
INA213BQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA213CQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA214AQDCKRQ1	SC70	DCK	6	3000	340.0	340.0	38.0
INA214BQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA214CQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA215BQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0
INA215CQDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

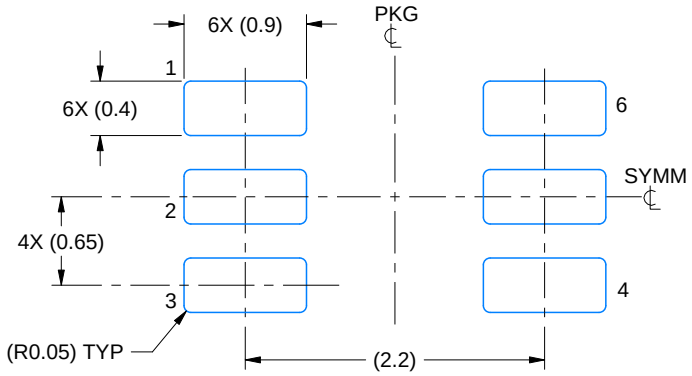
SMALL OUTLINE TRANSISTOR



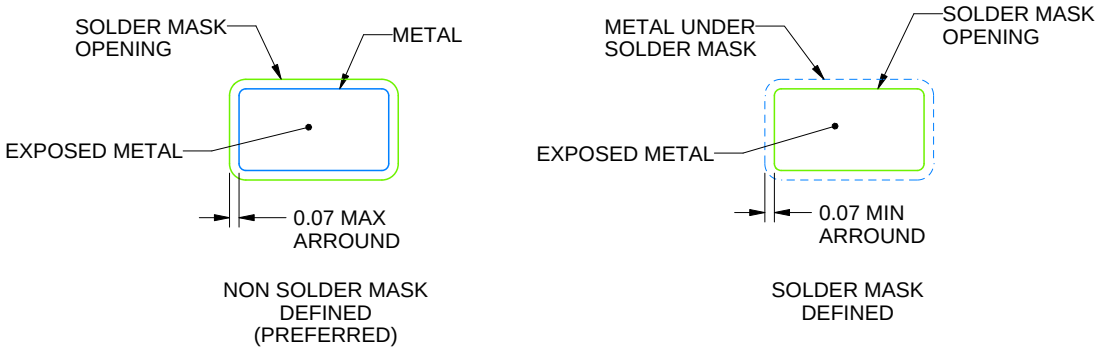
4214835/C 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

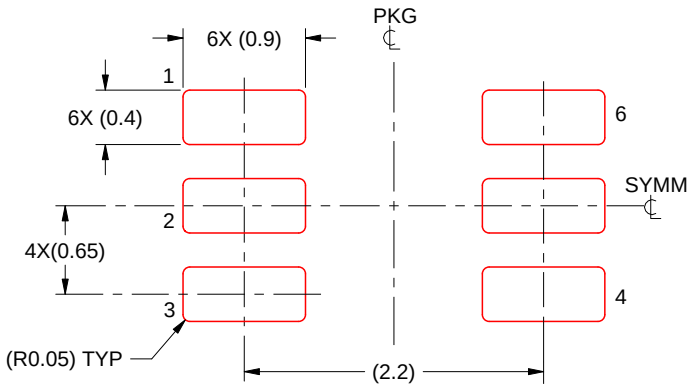


SOLDER MASK DETAILS

4214835/C 08/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214835/C 08/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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