

SN74AUC1G79 Single Positive-Edge-Triggered D-type Flip-Flop

1 Features

- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- Available in the Texas Instruments NanoFree™ Package
- Optimized for 1.8-V Operation and Is 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- I_{off} Supports Partial-Power-Down Mode Operation
- Sub-1-V Operable
- Max t_{pd} of 1.9 ns at 1.8 V
- Low Power Consumption, 10- μ A Maximum I_{CC}
- ± 8 -mA Output Drive at 1.8 V

2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-Ray Player and Home Theater
- Embedded PC
- MP3 Player/Recorder (Portable Audio)
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

3 Description

This single positive-edge-triggered D-type flip-flop is operational at 0.8-V to 2.7-V V_{CC} , but is designed specifically for 1.65-V to 1.95-V V_{CC} operation.

When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|----------------|------------|-------------------|
| SN74AUC1G79DBV | SOT-23 (5) | 2.90 mm x 1.60 mm |
| SN74AUC1G79DCK | SC70 (5) | 2.00 mm x 1.25 mm |
| SN74AUC1G79YZP | DSBGA (5) | 1.75 mm x 1.25 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)

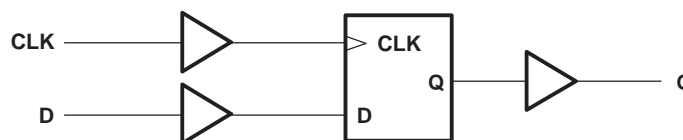


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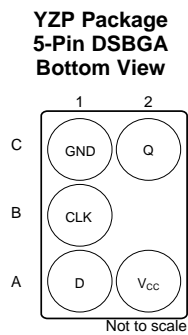
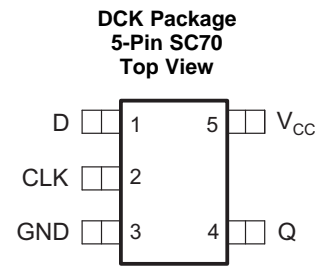
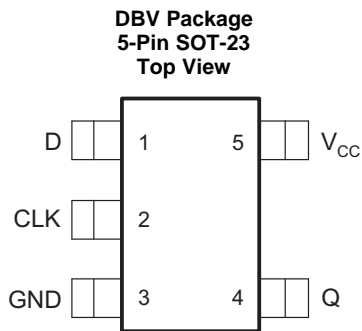
4 Revision History

Changes from Revision K (April 2007) to Revision L

Page

| | |
|--|----------|
| • Deleted DRY package throughout data sheet..... | 1 |
| • Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Configuration and Functions</i> , <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section..... | 1 |
| • Deleted <i>Ordering Information</i> table, see <i>Mechanical, Packaging, and Orderable Information</i> at the end of the data sheet | 1 |
| • Changed pin names in the pinout diagram for the YZP package, from: "A" to:"D," from:"B" to:"CLK," and from:"Y" to: "Q" | 3 |

5 Pin Configuration and Functions



See mechanical drawings for dimensions.

Pin Functions

| NAME | PIN | | I/O | DESCRIPTION |
|-----------------|----------|-----|-----|-----------------|
| | DBV, DCK | YZP | | |
| CLK | 2 | B1 | I | Clock input |
| D | 1 | A1 | I | Data input |
| GND | 3 | C1 | — | Ground |
| Q | 4 | C2 | O | Latched output |
| V _{CC} | 5 | A2 | — | Positive supply |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|---|--------------------|-----------------------|------|
| V _{CC} | Supply voltage | -0.5 | 3.6 | V |
| V _I | Input voltage ⁽²⁾ | -0.5 | 3.6 | V |
| V _O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 3.6 | V |
| V _O | Output voltage range ⁽²⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | -50 | mA |
| I _O | Continuous output current | | ±20 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | 2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | 1000 |
| | | Machine Model (A115-A) | 200 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

See⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------|---------------------------|-----------------------------------|------------------------|------|
| V _{CC} | Supply voltage | 0.8 | 2.7 | V |
| V _{IH} | High-level input voltage | V _{CC} = 0.8 V | V _{CC} | V |
| | | V _{CC} = 1.1 V to 1.95 V | 0.65 × V _{CC} | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | |
| V _{IL} | Low-level input voltage | V _{CC} = 0.8 V | 0 | V |
| | | V _{CC} = 1.1 V to 1.95 V | 0.35 × V _{CC} | |
| | | V _{CC} = 2.3 V to 2.7 V | 0.7 | |
| V _I | Input voltage | 0 | 3.6 | V |
| V _O | Output voltage | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 0.8 V | -0.7 | mA |
| | | V _{CC} = 1.1 V | -3 | |
| | | V _{CC} = 1.4 V | -5 | |
| | | V _{CC} = 1.65 V | -8 | |
| | | V _{CC} = 2.3 V | -9 | |
| I _{OL} | Low-level output current | V _{CC} = 0.8 V | 0.7 | mA |
| | | V _{CC} = 1.1 V | 3 | |
| | | V _{CC} = 1.4 V | 5 | |
| | | V _{CC} = 1.65 V | 8 | |
| | | V _{CC} = 2.3 V | 9 | |

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

Recommended Operating Conditions (continued)

See⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------|------------------------------------|-----|-----|------|
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 20 | ns/V |
| T_A | Operating free-air temperature | -40 | 85 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74AUC1G79 | | | UNIT | |
|-------------------------------|--|------------|-------------|------|------|
| | DBV (SOT-23) | DCK (SC70) | YZP (DSBGA) | | |
| | 5 PINS | 5 PINS | 5 PINS | | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 206 | 252 | 132 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V_{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|-----------|---|----------------|----------------|--------------------|----------|---------|
| V_{OH} | $I_{OH} = -100 \mu A$ | 0.8 V to 2.7 V | $V_{CC} - 0.1$ | | | V |
| | $I_{OH} = -0.7 \text{ mA}$ | 0.8 V | 0.55 | | | |
| | $I_{OH} = -3 \text{ mA}$ | 1.1 V | 0.8 | | | |
| | $I_{OH} = -5 \text{ mA}$ | 1.4 V | 1 | | | |
| | $I_{OH} = -8 \text{ mA}$ | 1.65 V | 1.2 | | | |
| | $I_{OH} = -9 \text{ mA}$ | 2.3 V | 1.8 | | | |
| V_{OL} | $I_{OL} = 100 \mu A$ | 0.8 V to 2.7 V | | | 0.2 | V |
| | $I_{OL} = 0.7 \text{ mA}$ | 0.8 V | 0.25 | | | |
| | $I_{OL} = 3 \text{ mA}$ | 1.1 V | | | 0.3 | |
| | $I_{OL} = 5 \text{ mA}$ | 1.4 V | | | 0.4 | |
| | $I_{OL} = 8 \text{ mA}$ | 1.65 V | | | 0.45 | |
| | $I_{OL} = 9 \text{ mA}$ | 2.3 V | | | 0.6 | |
| I_I | D or CLK input $V_I = V_{CC}$ or GND | 0 to 2.7 V | | | ± 5 | μA |
| I_{off} | V_I or $V_O = 2.7 \text{ V}$ | 0 | | | ± 10 | μA |
| I_{CC} | $V_I = V_{CC}$ or GND, $I_O = 0$ | 0.8 V to 2.7 V | | | 10 | μA |
| C_i | $V_I = V_{CC}$ or GND | 2.5 V | | | 2.5 | μF |

(1) All typical values are at $T_A = 25^\circ C$.

6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | $V_{CC} = 0.8 \text{ V}$ | $V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$ | | $V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$ | | $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | UNIT | |
|-------------|---|--|-----|--|-----|---|-----|--|-----|------|-----|
| | | TYP | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | MHz |
| f_{clock} | Clock frequency | 50 | 200 | | 225 | | 250 | | 275 | | ns |
| t_w | Pulse duration, CLK high or low | 4.6 | 1.7 | | 1.7 | | 1.7 | | 1.7 | | ns |
| t_{su} | Setup time before CLK \uparrow , data high or low | 1.5 | 1.1 | | 0.7 | | 0.7 | | 0.5 | | ns |
| t_h | Hold time, data after CLK \uparrow | 0 | 0 | | 0 | | 0 | | 0.1 | | ns |

SN74AUC1G79

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6.7 Switching Characteristics: $C_L = 15 \text{ pF}$

 over recommended operating free-air temperature range, $C_L = 15 \text{ pF}$ (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 0.8 \text{ V}$ | $V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$ | | $V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$ | | $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | | $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | UNIT |
|-----------|--------------|-------------|--------------------------|--|-----|--|-----|---|-----|-----|--|-----|------|
| | | | TYP | MIN | MAX | MIN | MAX | MIN | TYP | MAX | MIN | MAX | |
| f_{max} | | | 50 | 200 | | 225 | | 250 | | | 275 | | MHz |
| t_{pd} | CLK | Q | 5 | 1 | 3.9 | 0.8 | 2.5 | 0.3 | 1 | 1.9 | 0.3 | 1.3 | ns |

6.8 Switching Characteristics: $C_L = 30 \text{ pF}$

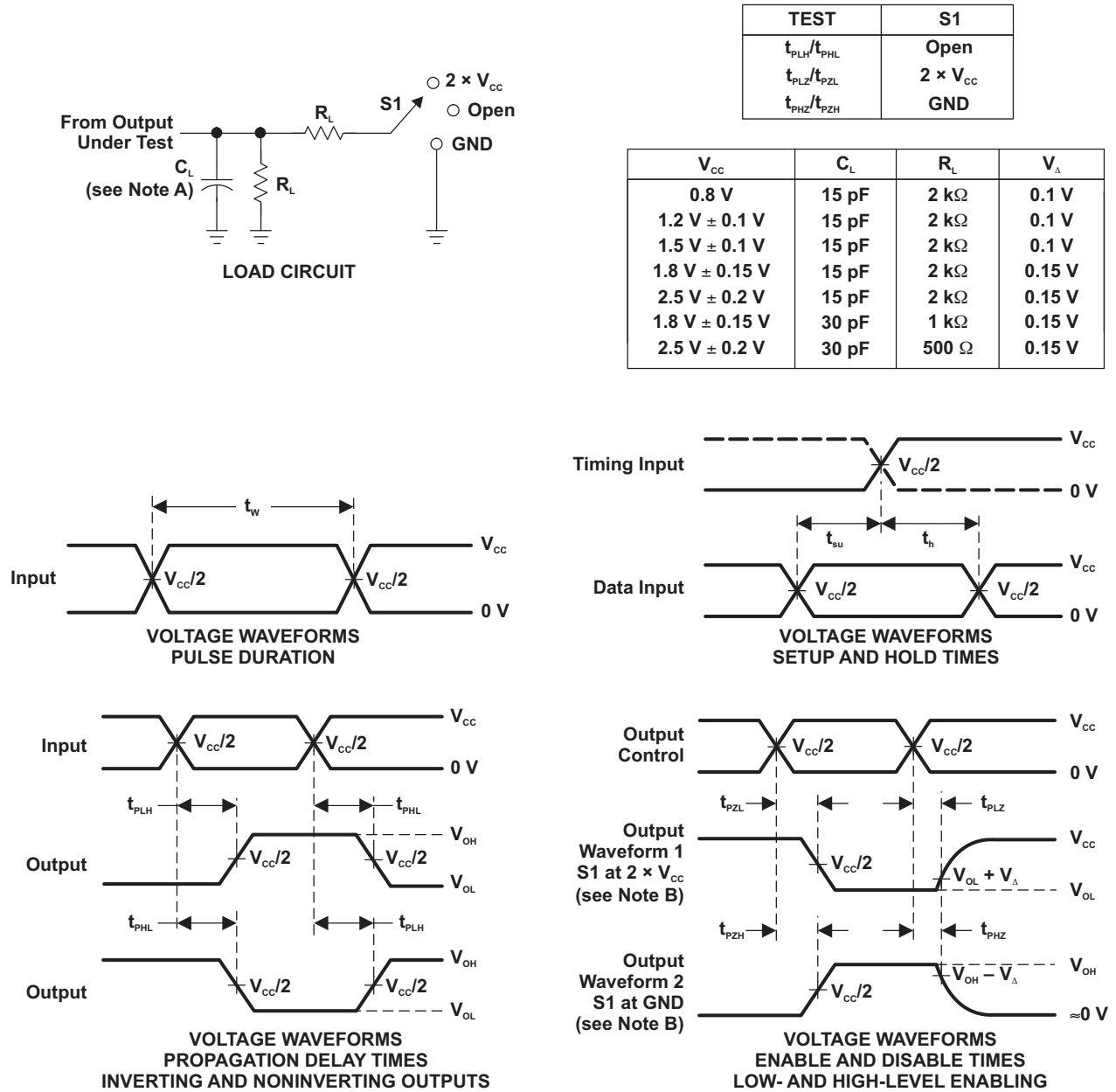
 over recommended operating free-air temperature range, $C_L = 30 \text{ pF}$ (unless otherwise noted) (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | | $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | UNIT |
|-----------|--------------|-------------|---|-----|-----|--|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | |
| f_{max} | | | | | | 250 | 275 | ns |
| t_{pd} | CLK | Q | 0.8 | 1.5 | 2.4 | 0.6 | 1.8 | ns |

6.9 Operating Characteristics
 $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CC} = 0.8 \text{ V}$ | $V_{CC} = 1.2 \text{ V}$ | $V_{CC} = 1.5 \text{ V}$ | $V_{CC} = 1.8 \text{ V}$ | $V_{CC} = 2.5 \text{ V}$ | UNIT |
|-----------|---|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|------|
| | | TYP | TYP | TYP | TYP | TYP | |
| C_{pd} | Power dissipation capacitance $f = 10 \text{ MHz}$ | 18 | 18 | 18 | 18.5 | 20.5 | pF |

7 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$, slew rate ≥ 1 V/ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram

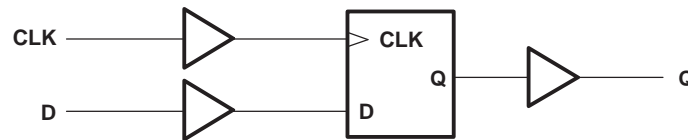


Figure 2. Logic Diagram (Positive Logic)

8.2 Device Functional Modes

[Table 1](#) lists the functional modes of the SN74AUC1G79.

Table 1. Function Table

| INPUTS | | OUTPUT |
|--------|---|----------------|
| CLK | D | Q |
| ↑ | H | H |
| ↑ | L | L |
| L | X | Q ₀ |

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.4 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.
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9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74AUC1G79DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | U79R | Samples |
| SN74AUC1G79DCKR | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (UR5, URF, URR) | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AUC1G79DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74AUC1G79DCKR | SC70 | DCK | 5 | 3000 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AUC1G79DBVR | SOT-23 | DBV | 5 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74AUC1G79DCKR | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |

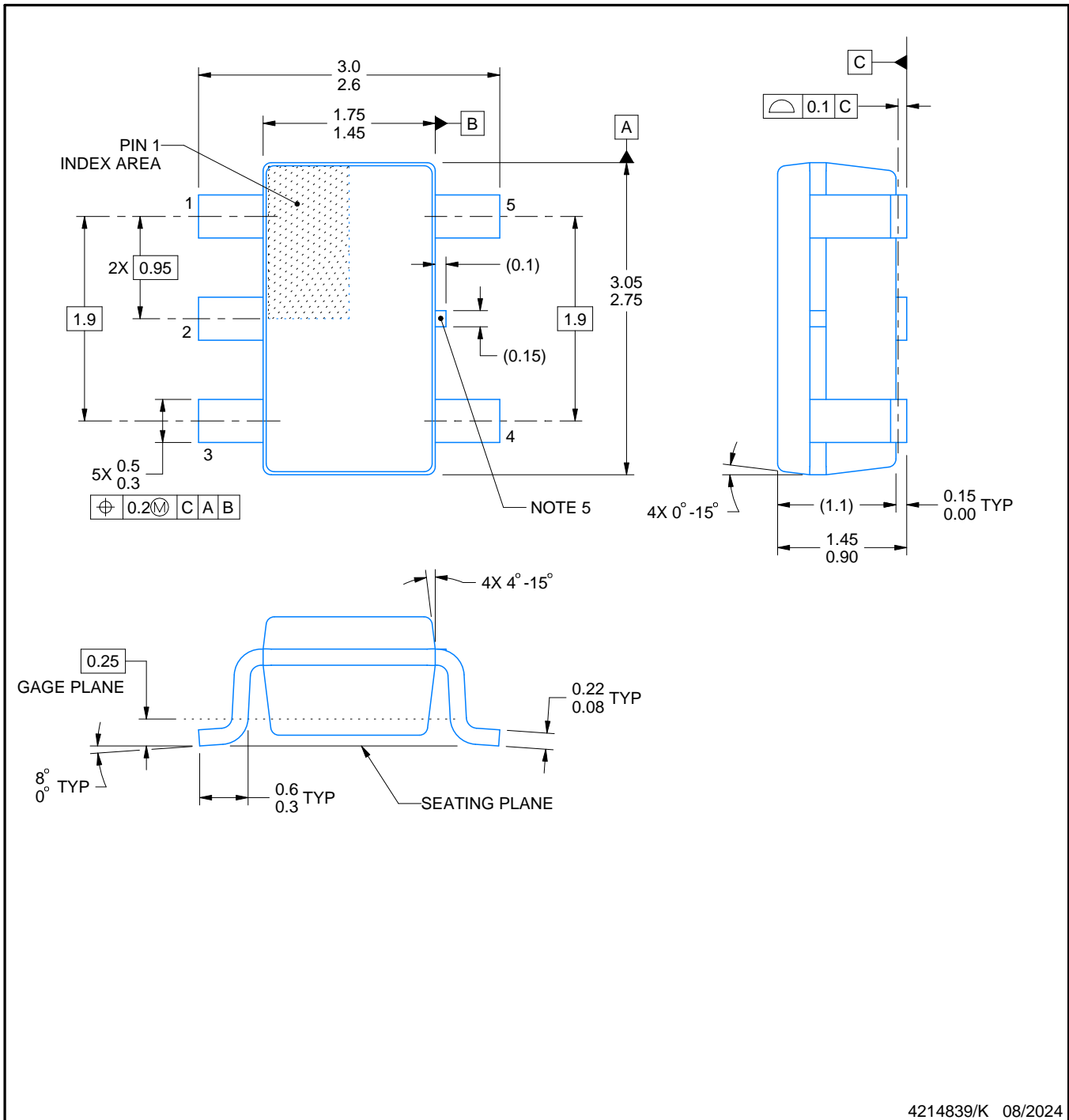


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

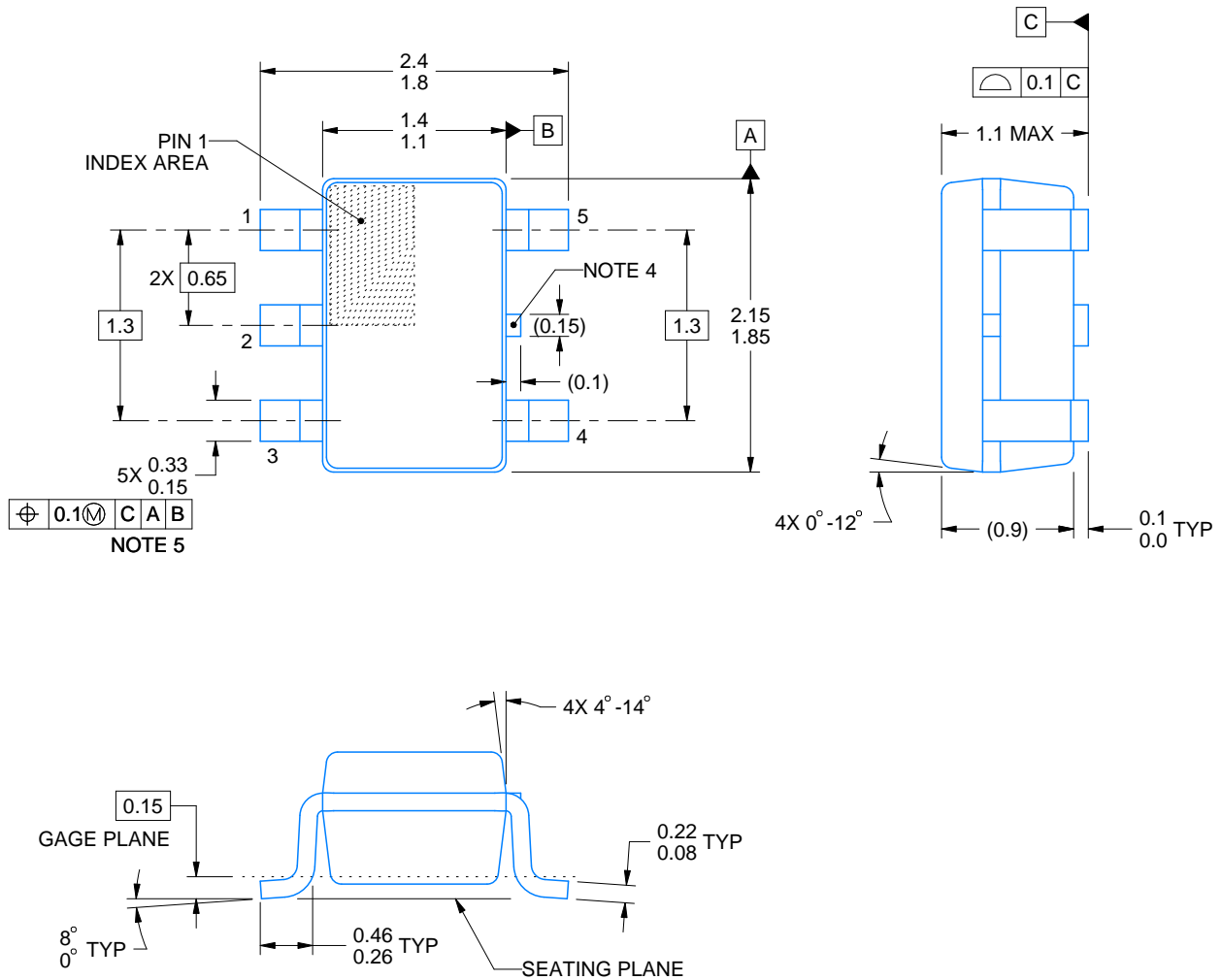
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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