SN54F374, SN74F374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

SDFS077A - D2932, MARCH 1987 - REVISED OCTOBER 1993

- Eight D-Type Flip-Flops in a Single Package
- 3-State Bus-Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (SOIC) and Shrink Small-Outline (SSOP) Packages, Ceramic Chip Carriers, and Plastic and Ceramic DIPs

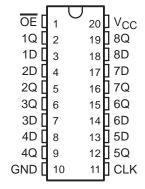
description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

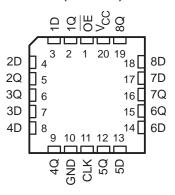
The eight flip-flops of the 'F374 are edge-triggered D-type flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

SN54F374 . . . J PACKAGE SN74F374 . . . DB, DW, OR N PACKAGE (TOP VIEW)



SN54F374 . . . FK PACKAGE (TOP VIEW)



The output enable (\overline{OE}) input does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74F374 is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54F374 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F374 is characterized for operation from 0°C to 70°C.

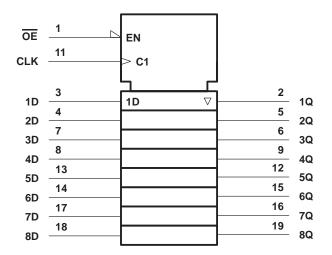
FUNCTION TABLE (each flip-flop)

		INPUTS		OUTPUT
O	Ε	CLK	Q	
		1	Н	Н
	L	\uparrow	L	L
	L	H or L	Χ	Q_0
H	1	Х	Χ	Z

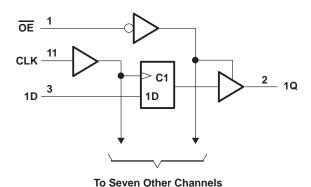


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logic symbol†



logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V _{CC}		
Input voltage range, V _I (see Note 1) .		
Input current range		30 mA to 5 mA
Voltage range applied to any output in	the disabled or power-off state .	
Voltage range applied to any output in	the high state	$-0.5 \text{ V to V}_{\text{CC}}$
Current into any output in the low state	: SN54F374	40 mA
	SN74F374	48 mA
Operating free-air temperature range:	SN54F374	–55°C to 125°C
	SN74F374	0°C to 70°C
Storage temperature range		65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54F374			S	1	UNIT	
		MIN	NOM	MAX	MIN	NOM	MAX	UNII
Vcc	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			8.0	V
lıK	Input clamp current			-18			-18	mA
ІОН	High-level output current			-3			-3	mA
IOL	Low-level output current			20			24	mA
TA	Operating free-air temperature	-55		125	0		70	°C



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

SN54F374, SN74F374 OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

			S	N54F37	4	S	N74F374	1	
PARAMETER	TES	ST CONDITIONS	MIN	TYP†	MAX	MIN	TYP†	MAX	UNIT
VIK	$V_{CC} = 4.5 \text{ V},$	I _I = –18 mA			-1.2			-1.2	V
	V 45V	$I_{OH} = -1 \text{ mA}$	2.5	3.4		2.5	3.4		
Voн	V _{CC} = 4.5 V	$I_{OH} = -3 \text{ mA}$	2.4	3.3		2.4	3.3		V
	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = -1 \text{ mA to } -3 \text{ mA}$				2.7			
V	V 45V	I _{OL} = 20 mA		0.3	0.5				V
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 24 mA					0.35	0.5	V
lozh	V _{CC} = 5.5 V,	$V_0 = 2.7 \text{ V}$			50			50	μΑ
lozL	V _{CC} = 5.5 V,	V _O = 0.5 V			-50			-50	μΑ
lį	V _{CC} = 5.5 V,	$V_I = 7 V$			0.1			0.1	mA
lіН	$V_{CC} = 5.5 \text{ V},$	V _I = 2.7 V			20			20	μΑ
I _{IL}	$V_{CC} = 5.5 \text{ V},$	V _I = 0.5 V			- 0.6			- 0.6	mA
los [‡]	V _{CC} = 5.5 V,	V _O = 0	-60		-150	-60		-150	mA
ICCZ	V _{CC} = 5.5 V,	See Note 2		55	86		55	86	mA

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			T _A =	V _{CC} = 5 V, T _A = 25°C 'F374		F374	SN74	F374	UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX		
f _{clock}	Clock frequency		0	100	0	60	0	70	MHz	
		CLK high	7		7		7			
t _W	Pulse duration	CLK low	6		6		6		ns	
	Octor for a data before OUKA	High	2		2.5		2			
t _{su}	Setup time, data before CLK↑	Low	2		2		2		ns	
4.	Hold time data after OLKA	High	2		2		2			
th	Hold time, data after CLK	Hold time, data after CLK↑	Low	2		2.5		2		ns

[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. NOTE 2: I_{CCZ} is measured with $\overline{\text{OE}}$ at 4.5 V and all other inputs grounded.

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switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)			$V_{CC} = 5 \text{ V},$ $C_{L} = 50 \text{ pF},$ $R_{L} = 500 \Omega,$ $T_{A} = 25^{\circ}\text{C}$			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω , T_A = MIN to MAX \dagger				
			′F374			SN54	F374	SN74	F374		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX		
f _{max}			100			60		70		MHz	
^t PLH	OL IX	Q	3.2	6.1	8.5	3.2	10.5	3.2	10		
^t PHL	CLK	α	3.2	6.1	8.5	3.2	11	3.2	10	ns	
^t PZH	ŌĒ	0	1.2	8.6	11.5	1.2	14	1.2	12.5		
t _{PZL}	OE	Q	1.2	5.4	7.5	1.2	10	1.2	8.5	ns	
t _{PHZ}	ŌĒ	0	1.2	4.9	7	1.2	8	1.2	8	ns	
tPLZ	OE	Q	1.2	3.9	5.5	1.2	7.5	1.2	6.5	110	

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. NOTE 3: Load circuits and waveforms are shown in Section 1.



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9759001Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9759001Q2A SNJ54F 374FK	Samples
5962-9759001QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759001QR A SNJ54F374J	Samples
5962-9759001QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759001QR A SNJ54F374J	Samples
5962-9759001QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759001QS A SNJ54F374W	Samples
5962-9759001QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759001QS A SNJ54F374W	Samples
JM38510/34105B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105B2A	Samples
JM38510/34105B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105B2A	Samples
JM38510/34105BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105BRA	Samples
JM38510/34105BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105BRA	Samples
JM38510/34105BSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105BSA	Samples
JM38510/34105BSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105BSA	Samples
M38510/34105B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105B2A	Samples
M38510/34105B2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105B2A	Samples
M38510/34105BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105BRA	Samples





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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Sample
M38510/34105BRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105BRA	Samples
M38510/34105BSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105BSA	Samples
M38510/34105BSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 34105BSA	Samples
SN54F374J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54F374J	Samples
SN54F374J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54F374J	Samples
SN74F374DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F374	Samples
SN74F374DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F374	Samples
SN74F374DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	F374	
SN74F374DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	F374	
SN74F374DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F374	Samples
SN74F374DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	F374	Samples
SN74F374N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F374N	Samples
SN74F374N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN74F374N	Samples
SN74F374NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F374	Samples
SN74F374NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	74F374	Samples
SNJ54F374FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9759001Q2A SNJ54F 374FK	Samples
SNJ54F374FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9759001Q2A SNJ54F 374FK	Sample
SNJ54F374J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759001QR A	Samples



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Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54F374J	
SNJ54F374J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759001QR A SNJ54F374J	Samples
SNJ54F374W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759001QS A SNJ54F374W	Samples
SNJ54F374W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9759001QS A SNJ54F374W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

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OTHER QUALIFIED VERSIONS OF SN54F374, SN74F374:

Catalog: SN74F374

Military: SN54F374

NOTE: Qualified Version Definitions:

- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

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TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

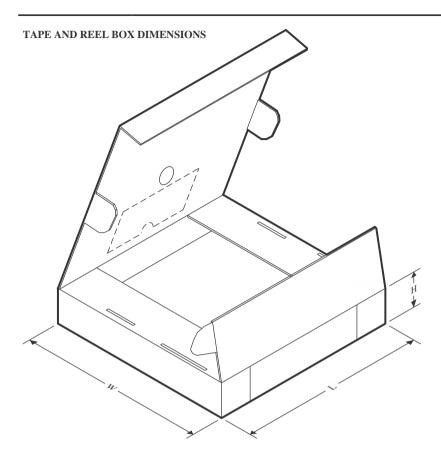


*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F374DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74F374DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74F374NSR	so	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1



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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F374DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74F374DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74F374NSR	SO	NS	20	2000	367.0	367.0	45.0

PACKAGE MATERIALS INFORMATION

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TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9759001Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9759001QSA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/34105B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/34105BSA	W	CFP	20	25	506.98	26.16	6220	NA
M38510/34105B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/34105BSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74F374N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54F374FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54F374W	W	CFP	20	25	506.98	26.16	6220	NA

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.





SOIC



- 1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- 5. Reference JEDEC registration MS-013.



SOIC



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOIC



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.

 D. Index point is provided on cap for terminal identification only.

 E. Falls within Mil—Std 1835 GDFP2—F20





SMALL OUTLINE PACKAGE



- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

 2. This drawing is subject to change without notice.

 3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
- exceed 0.15 mm per side.
- 4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- 5. Reference JEDEC registration MO-150.



SMALL OUTLINE PACKAGE



NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SMALL OUTLINE PACKAGE



NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



14 LEADS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package is hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
- E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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