

SN74HCS264-Q1 Automotive 8-Bit Parallel-Out Serial Shift Registers With Schmitt-Trigger Inputs and Inverted Outputs

1 Features

- AEC-Q100 Qualified for automotive applications:
 - Device temperature grade 1: -40°C to $+125^{\circ}\text{C}$, T_A
 - Device HBM ESD Classification Level 2
 - Device CDM ESD Classification Level C6
- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
 - Typical I_{CC} of 100 nA
 - Typical input leakage current of ± 100 nA
- ± 7.8 -mA output drive at 6 V

2 Applications

- [Output expansion](#)
- [LED matrix control](#)
- [7-segment display control](#)
- 8-bit data storage

3 Description

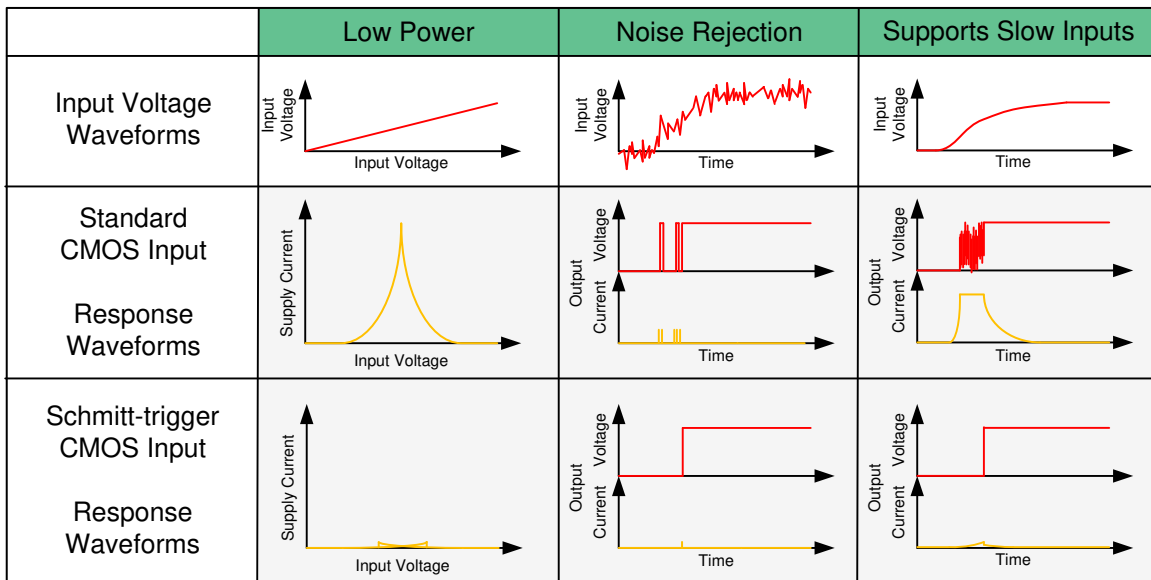
The SN74HCS264-Q1 device contains an 8-bit shift register with AND-gated serial inputs and an asynchronous clear (CLR) input. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. All inputs include Schmitt-trigger architecture, adding noise margin and eliminating any input transition rate requirement. Clocking occurs on the low-to-high-level transition of CLK.

Upon a clock trigger, the device will store the result of the (A • B) input data line in the first register and propagate each register's data to the next register. The outputs are inverted from the data stored.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74HCS264PW-Q1	TSSOP (16)	5.00 mm × 4.40 mm
SN74HCS264D-Q1	SOIC (16)	9.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Benefits of Schmitt-trigger inputs



Table of Contents

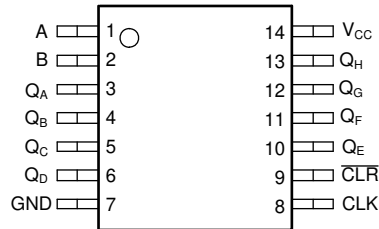
1 Features	1	8.2 Functional Block Diagram.....	9
2 Applications	1	8.3 Feature Description.....	9
3 Description	1	8.4 Device Functional Modes.....	10
4 Revision History	2	9 Application and Implementation	11
5 Pin Configuration and Functions	3	9.1 Application Information.....	11
Pin Functions.....	3	9.2 Typical Application.....	11
6 Specifications	4	10 Power Supply Recommendations	14
6.1 Absolute Maximum Ratings.....	4	11 Layout	14
6.2 ESD Ratings.....	4	11.1 Layout Guidelines.....	14
6.3 Recommended Operating Conditions.....	4	11.2 Layout Example.....	14
6.4 Thermal Information.....	4	12 Device and Documentation Support	15
6.5 Electrical Characteristics.....	5	12.1 Documentation Support.....	15
6.6 Timing Characteristics.....	5	12.2 Receiving Notification of Documentation Updates..	15
6.7 Switching Characteristics.....	6	12.3 Support Resources.....	15
6.8 Operating Characteristics.....	6	12.4 Trademarks.....	15
6.9 Typical Characteristics.....	7	12.5 Electrostatic Discharge Caution.....	15
7 Parameter Measurement Information	8	12.6 Glossary.....	15
8 Detailed Description	9	13 Mechanical, Packaging, and Orderable Information	16
8.1 Overview.....	9		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
July 2020	*	Initial Release

5 Pin Configuration and Functions



D or PW Package 14-Pin SOIC or TSSOP Top View

Pin Functions

PIN		I/O	DESCRIPTION
SOIC or TSSOP NO.	NAME		
1	A	I	Serial input A
2	B	I	Serial input B
3	Q _A	O	Parallel output A
4	Q _B	O	Parallel output B
5	Q _C	O	Parallel output C
6	Q _D	O	Parallel output D
7	GND	—	Ground
8	CLK	I	Clock, rising edge triggered
9	$\overline{\text{CLR}}$	I	Clear 1 Active-Low
10	Q _E	O	Parallel output E
11	Q _F	O	Parallel output F
12	Q _G	O	Parallel output G
13	Q _H	O	Parallel output H
14	V _{CC}	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20 mA
I _{OK}	Output clamp current ⁽²⁾	V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35 mA
	Continuous current through V _{CC} or GND			±70 mA
T _J	Junction temperature ⁽³⁾			150 °C
T _{stg}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) Guaranteed by design.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±4000
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500

- (1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2	5	6	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
T _A	Ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74HCS264-Q1		UNIT
		PW (TSSOP)	D (SOIC)	
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	141.2	122.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	78.8	80.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	85.8	80.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	27.7	40.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	85.5	80.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V_{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$) ⁽¹⁾			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V_{OH}	High-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OH} = -20\ \mu\text{A}$	2 V to 6 V	$V_{CC} - 0.1$	$V_{CC} - 0.002$		V
			$I_{OH} = -6\ \text{mA}$	4.5 V	4.0	4.3		
			$I_{OH} = -7.8\ \text{mA}$	6 V	5.4	5.75		
V_{OL}	Low-level output voltage	$V_I = V_{IH}$ or V_{IL}	$I_{OL} = 20\ \mu\text{A}$	2 V to 6 V		0.002	0.1	V
			$I_{OL} = 6\ \text{mA}$	4.5 V		0.18	0.30	
			$I_{OL} = 7.8\ \text{mA}$	6 V		0.22	0.33	
I_I	Input leakage current	$V_I = V_{CC}$ or 0		6 V		± 100	± 1000	nA
I_{CC}	Supply current	$V_I = V_{CC}$ or 0, $I_O = 0$		6 V		0.1	2	μA
C_i	Input capacitance			2 V to 6 V			5	pF

(1) Guaranteed by design.

6.6 Timing Characteristics

$C_L = 50\ \text{pF}$; over operating free-air temperature range (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER			V_{CC}	Operating free-air temperature (T_A)				UNIT
				25°C		-40°C to 125°C		
				MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		2 V	28		15		
			4.5 V	68		50		
			6 V	97		62		
t_w	Pulse duration	$\overline{\text{CLR}}$ low	2 V	7		12	ns	
			4.5 V	6		7		
			6 V	6		7		
		CLK high or low	2 V	8		12		
			4.5 V	6		7		
			6 V	6		7		
t_{su}	Setup time	Data	2 V	11		17	ns	
			4.5 V	4		6		
			6 V	4		6		
		$\overline{\text{CLR}}$ inactive	2 V	6		9		
			4.5 V	3		4		
			6 V	3		4		

PARAMETER			V _{CC}	Operating free-air temperature (T _A)				UNIT
				25°C		–40°C to 125°C		
				MIN	MAX	MIN	MAX	
t _h	Hold time	Data after CLK↑	2 V	0		0		ns
			4.5 V	0		0		
			6 V	0		0		

6.7 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER		FROM	TO	V _{CC}	Operating free-air temperature (T _A)						UNIT	
					25°C			–40°C to 125°C				
					MIN	TYP	MAX	MIN	TYP	MAX		
f _{max}	Max switching frequency			2 V	28			15			MHz	
				4.5 V	68			50				
				6 V	97			62				
t _{PHL}	Propagation delay	$\overline{\text{CLR}}$	Any Q	2 V		20	25			42	ns	
				4.5 V		8	12			18		
				6 V		7	11			15		
t _{pd}	Propagation delay	CLK	Any Q	2 V		20	26			42	ns	
				4.5 V		8	12			16		
				6 V		7	11			14		
t _t	Transition-time		Any output	2 V						9	ns	
				4.5 V						5		9
				6 V						4		8

6.8 Operating Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
C _{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		40		pF

6.9 Typical Characteristics

$T_A = 25^\circ\text{C}$

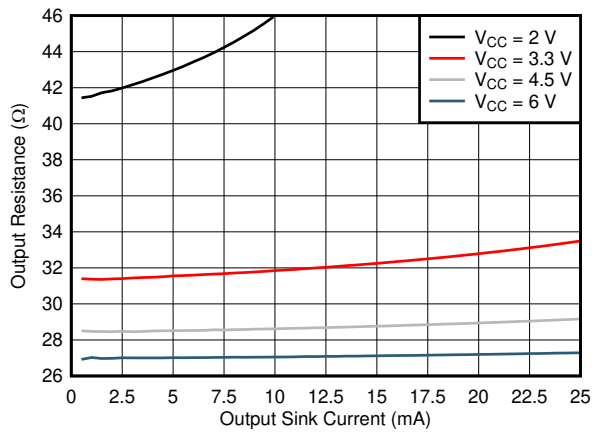


Figure 6-1. Output driver resistance in LOW state.

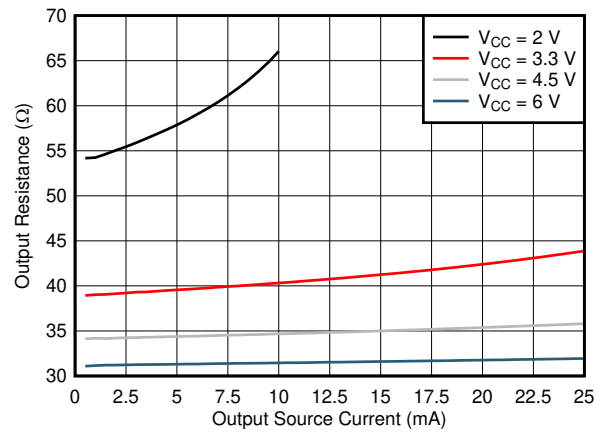


Figure 6-2. Output driver resistance in HIGH state.

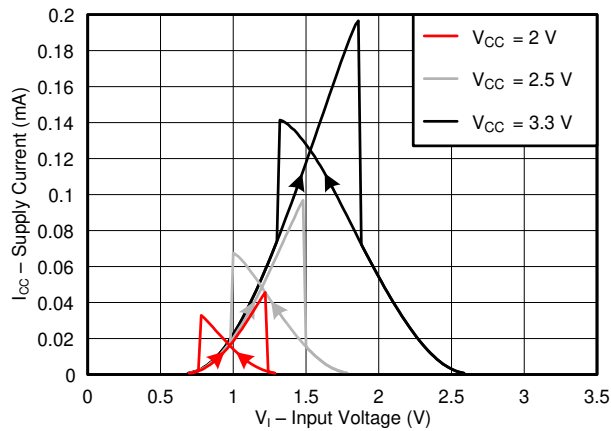


Figure 6-3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

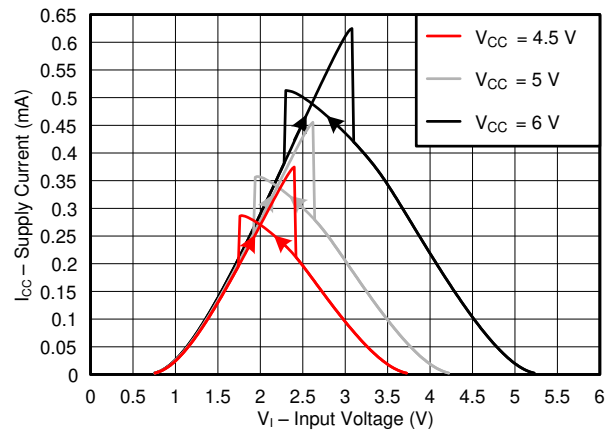


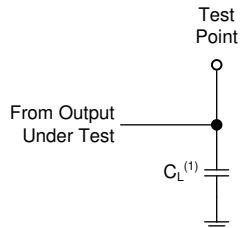
Figure 6-4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \ \Omega$, $t_t < 2.5 \text{ ns}$.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit

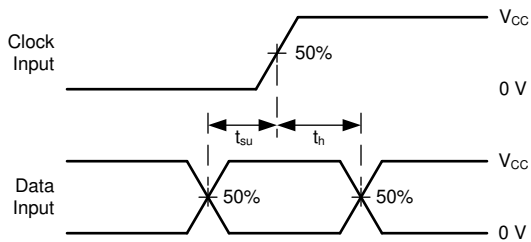


Figure 7-3. Voltage Waveforms, Setup and Hold Times

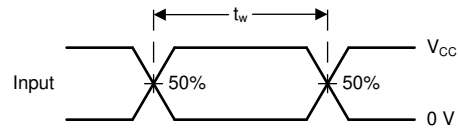
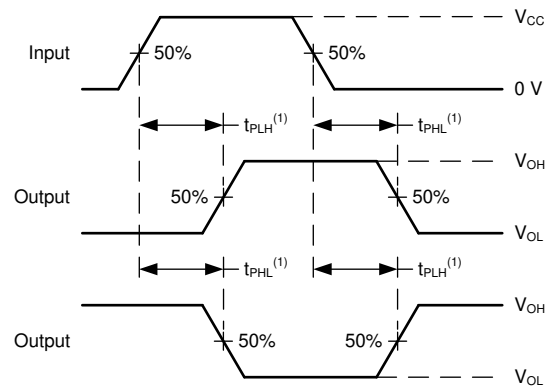
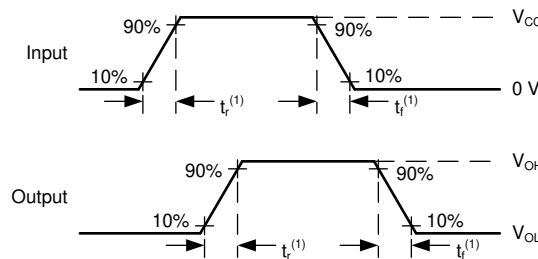


Figure 7-2. Voltage Waveforms, Pulse Duration



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 7-4. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 7-5. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Overview

The SN74HCS264-Q1 is an 8-bit shift register with 2 serial inputs (A and B) connected through an AND gate, as well as an asynchronous clear ($\overline{\text{CLR}}$). The device requires a high signal on both A and B in order to set the input data line high; a low signal on either input will set the input data line low. Data at A and B can be changed while CLK is high or low, provided that the minimum set-up time requirements are met.

The CLK pin of the SN74HCS264-Q1 is rising-edge triggered, activating on the transition from LOW to HIGH. Upon a positive-edge trigger, the device will store the result of the ($A \bullet B$) input data line in the first register and propagate each register's data to the next register. The data of the last register, Q_H , will be discarded at each clock trigger. If a low signal is applied to the $\overline{\text{CLR}}$ pin, then the SN74HCS264-Q1 will set all registers to a logical low value immediately.

8.2 Functional Block Diagram

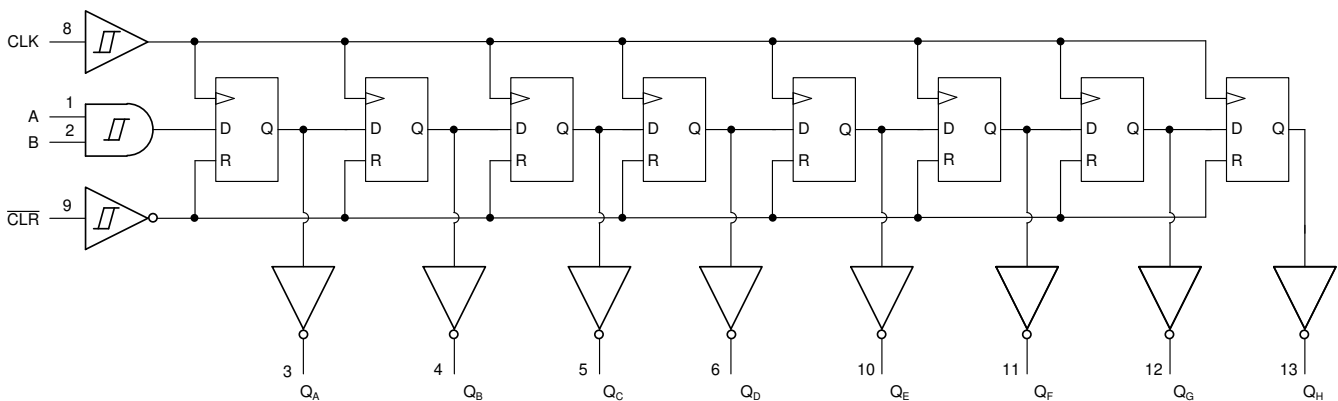


Figure 8-1. Logic Diagram (Positive Logic) for SN74HCS264-Q1

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ($R = V \div I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Electrical Placement of Clamping Diodes for Each Input and Output](#).

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

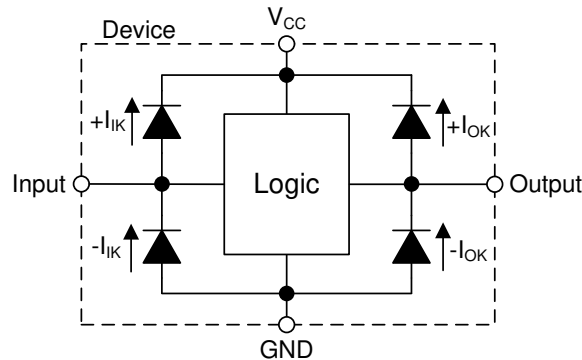


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

[Function Table](#) lists the functional modes of the SN74HCS264-Q1.

Table 8-1. Function Table

INPUTS				FUNCTION
A	B	CLR	CLK	
X	X	L	X	Shift register is cleared. All internal storage registers go low; all outputs are high.
L	X	H	↑	First stage of the shift register goes low; the output at Q _A goes high. Other stages store the data of each previous stage, respectively. All outputs are inverted from the internally stored data.
X	L	H	↑	First stage of the shift register goes low; the output at Q _A goes high. Other stages store the data of each previous stage, respectively. All outputs are inverted from the internally stored data.
H	H	H	↑	First stage of the shift register goes high; the output at Q _A goes low. Other stages store the data of each previous stage, respectively. All outputs are inverted from the internally stored data.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In this application, the SN74HCS264-Q1 is used to control seven-segment displays. Unlike other I/O expanders, the SN74HCS264-Q1 does not need a communication interface for control. It can be easily operated with simple GPIO pins. Additional control is provided with two serial inputs that feed into an AND gate. Data is inverted at the outputs.

At power-up, the initial state of the shift registers is unknown. To give them a defined state, the shift register needs to be cleared. An RC can be connected to the CLR pin as shown in Figure 1-1 below to initialize the shift register to all zeros resulting in all outputs being High.

9.2 Typical Application

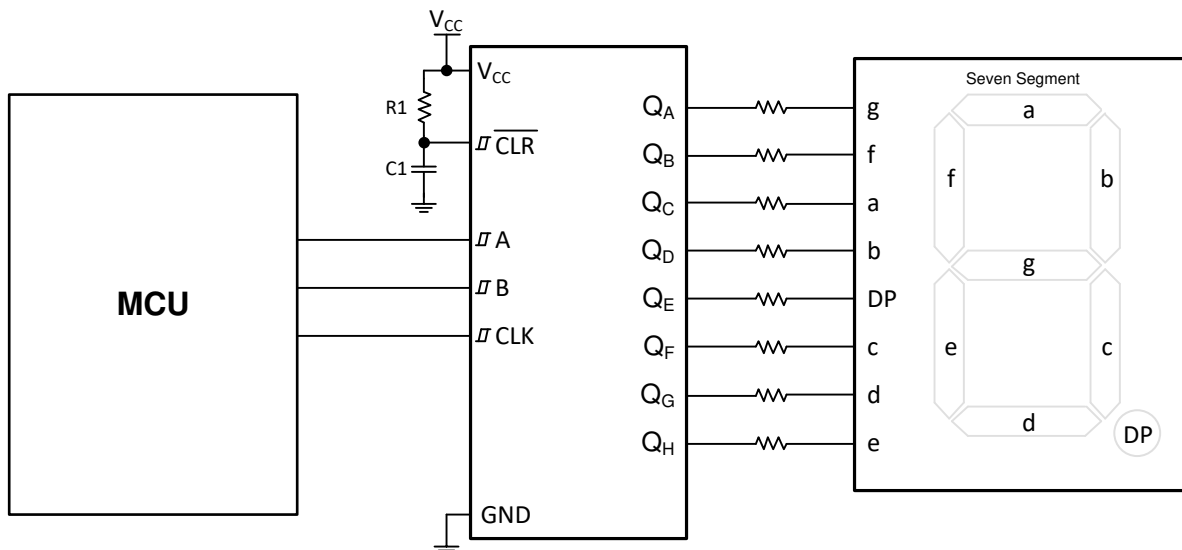


Figure 9-1. Typical application block diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS264-Q1 plus the maximum static supply current, I_{CC} , listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS264-Q1 plus the maximum supply current, I_{CC} , listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS264-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HCS264-Q1 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS264-Q1, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SN74HCS264-Q1 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS264-Q1 to the receiving device(s).
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

9.2.3 Application Curve

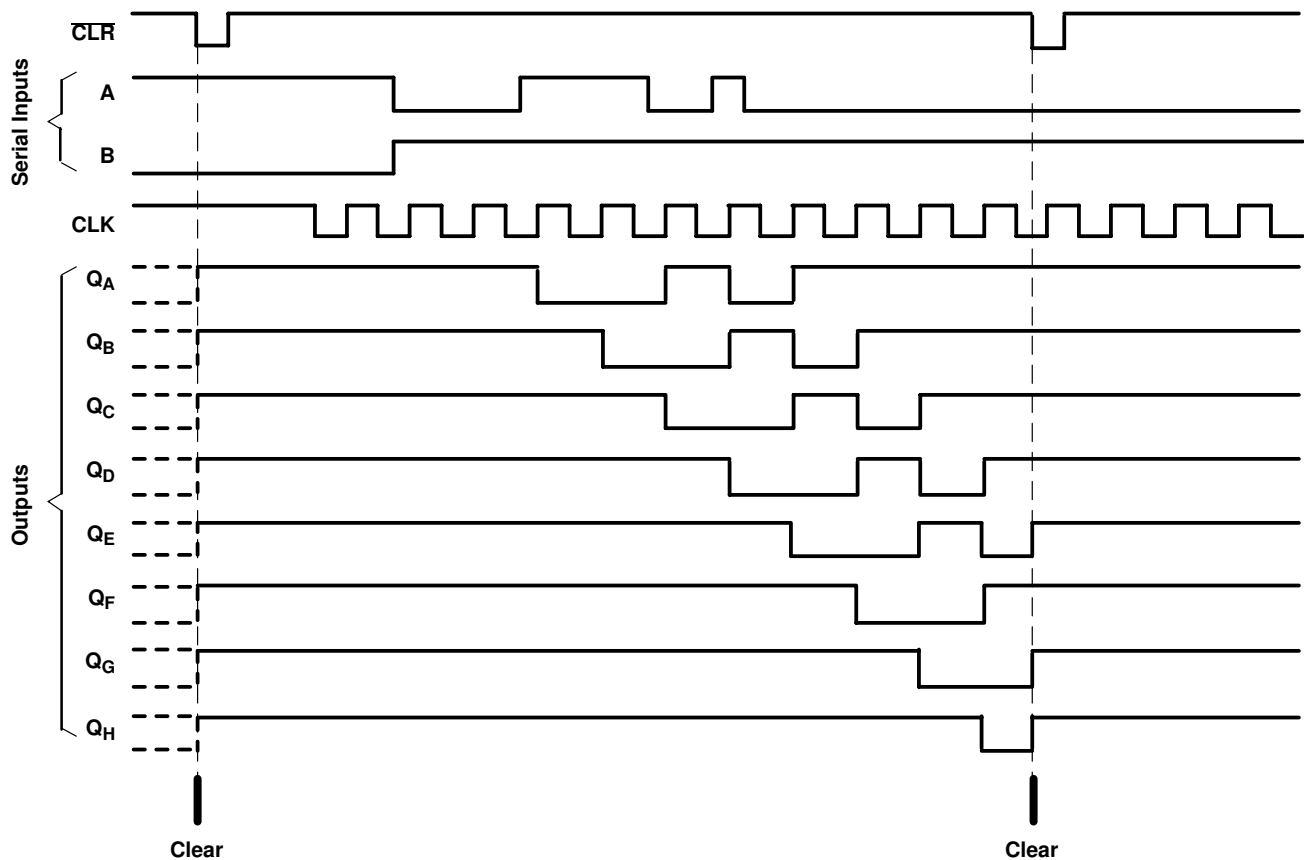


Figure 9-2. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

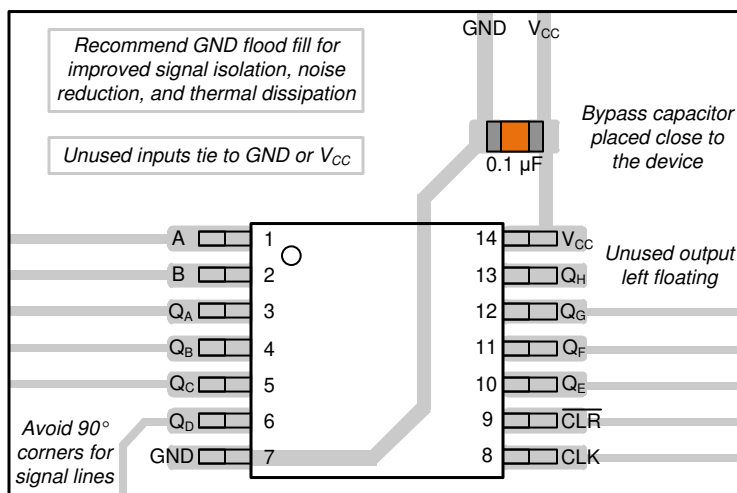


Figure 11-1. Example layout for the SN74HCS264-Q1.

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [HCMOS Design Considerations application report](#) (SCLA007)
- Texas Instruments, [CMOS Power Consumption and \$C_{pd}\$ Calculation application report](#) (SDYA009)
- Texas Instruments, [Designing With Logic application report](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on [Subscribe to updates](#) to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS264QDRQ1	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS264Q	Samples
SN74HCS264QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS264Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74HCS264-Q1 :

- Catalog: [SN74HCS264](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS264QDRQ1	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS264QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS264QDRQ1	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCS264QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

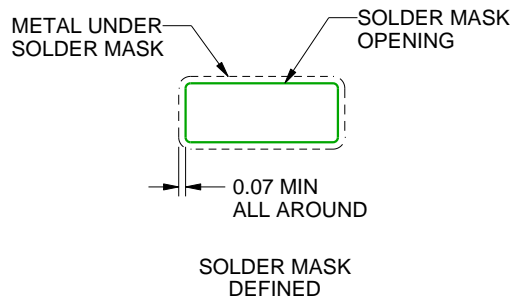
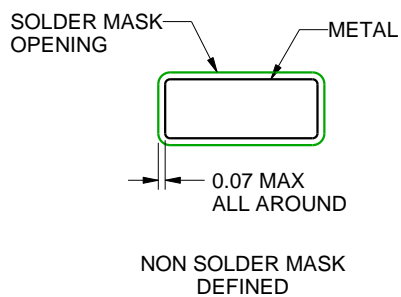
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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