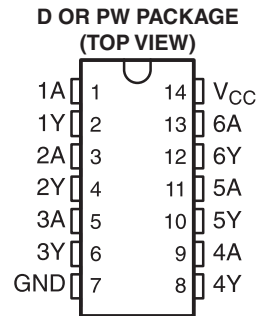


## HEX BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

Check for Samples: [SN74LVC07A-Q1](#)

### FEATURES

- Qualified for Automotive Applications
- Operates From 1.65 V to 5 V
- Inputs and Open-Drain Outputs Accept Voltages up to 5.5 V
- Latch-Up Performance Exceeds 250 mA Per JESD 17



### DESCRIPTION/ORDERING INFORMATION

This hex buffer/driver is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The outputs of the SN74LVC07A device are open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 24 mA.

Inputs can be driven from 1.8-V, 2.5-V, 3.3-V (LVTTTL), or 5-V (CMOS) devices. This feature allows the use of this device as a translator in a mixed-system environment.

### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	SN74LVC07AQDRQ1	LVC07AQ
	TSSOP – PW	Reel of 2000	SN74LVC07AQPWRQ1	LVC07AQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

**Table 1. FUNCTION TABLE  
(EACH BUFFER/DRIVER)**

INPUT A	OUTPUT Y
H	H
L	L

### LOGIC DIAGRAM, EACH BUFFER/DRIVER (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Output voltage range	-0.5	6.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		-50 mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		-50 mA
I <sub>O</sub>	Continuous output current			±50 mA
Continuous current through V <sub>CC</sub> or GND				±100 mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	D package		86 °C/W
		PW package		113
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	1.65	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.65 × V <sub>CC</sub>
		V <sub>CC</sub> = 2.3 V to 2.7 V		1.7
		V <sub>CC</sub> = 2.7 V to 3.6 V		2
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V		0.35 × V <sub>CC</sub>
		V <sub>CC</sub> = 2.3 V to 2.7 V		0.7
		V <sub>CC</sub> = 2.7 V to 3.6 V		0.8
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	5.5	V
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V		4
		V <sub>CC</sub> = 2.3 V		12
		V <sub>CC</sub> = 2.7 V		12
		V <sub>CC</sub> = 3 V		24
T <sub>A</sub>	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 3.6 V			0.2	V
	I <sub>OL</sub> = 4 mA	1.65 V			0.45	
	I <sub>OL</sub> = 12 mA	2.3 V			0.7	
		2.7 V			0.4	
	I <sub>OL</sub> = 24 mA	3 V			0.65	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	3.6 V			±5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	3.6 V			10	μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	2.7 V to 3.6 V			500	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V			5	pF

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#) through [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A	Y	1	3.5	1	2.8		3	1	2.9	ns

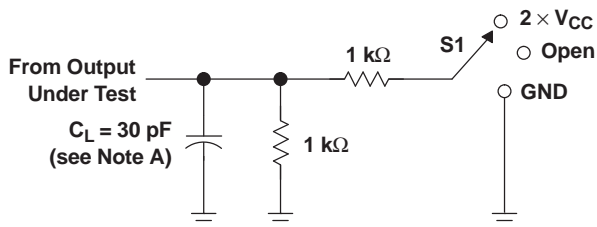
## Operating Characteristics

 T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	UNIT
		TYP	TYP	TYP	
C <sub>pd</sub> Power dissipation capacitance per buffer/driver	f = 10 MHz	1.8	2	2.5	pF

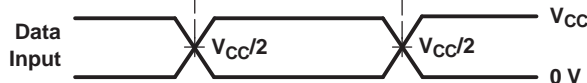
**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$

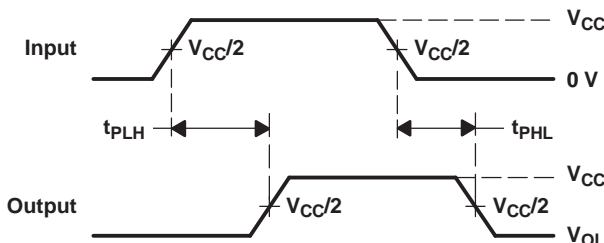


**LOAD CIRCUIT**

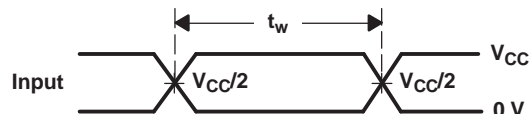
TEST	S1
$t_{pZL}$ (see Note F)	$2 \times V_{CC}$
$t_{pLZ}$ (see Note G)	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	$2 \times V_{CC}$



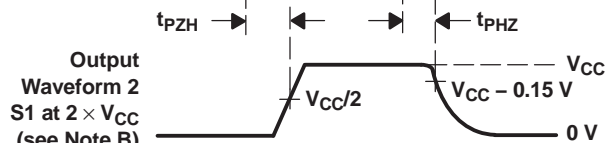
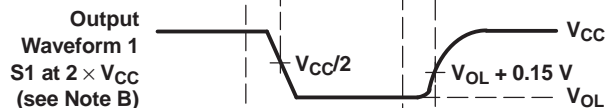
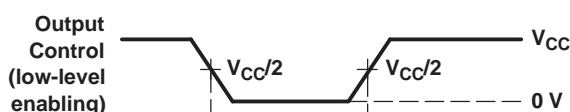
**VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS  
PULSE DURATION**



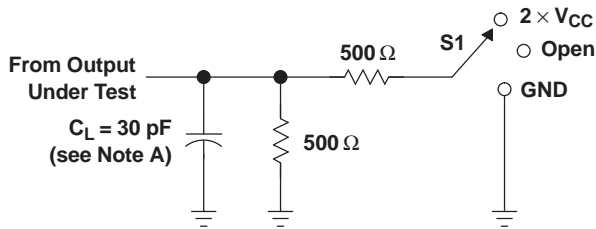
**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. Since this device has open-drain outputs,  $t_{pLZ}$  and  $t_{pZL}$  are the same as  $t_{pd}$ .  
 F.  $t_{pZL}$  is measured at  $V_{CC}/2$ .  
 G.  $t_{pLZ}$  is measured at  $V_{OL} + 0.15\text{ V}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

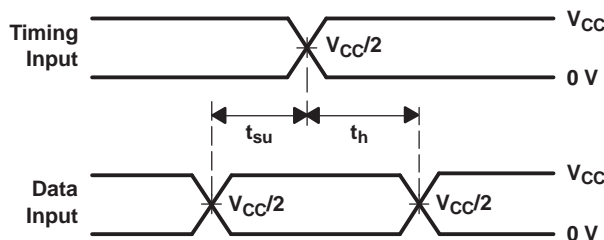
PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$

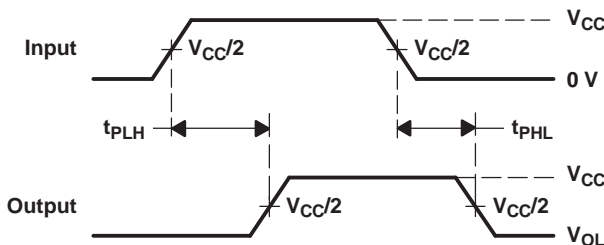


LOAD CIRCUIT

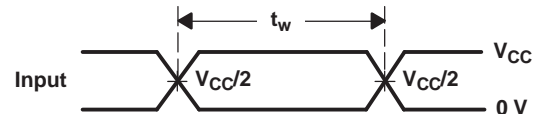
TEST	S1
$t_{pZL}$ (see Note F)	$2 \times V_{CC}$
$t_{pLZ}$ (see Note G)	$2 \times V_{CC}$
$t_{pHZ}/t_{pZH}$	$2 \times V_{CC}$



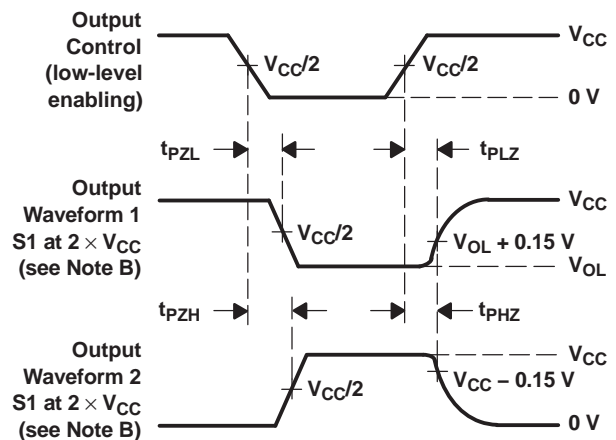
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS PULSE DURATION



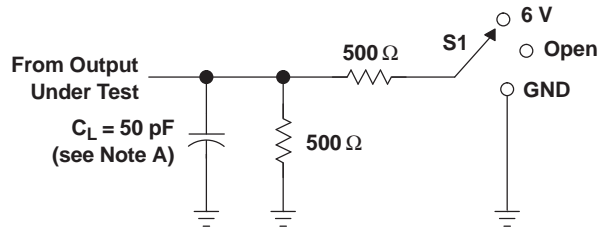
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2\text{ ns}$ ,  $t_f \leq 2\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. Since this device has open-drain outputs,  $t_{pLZ}$  and  $t_{pZL}$  are the same as  $t_{pd}$ .  
 F.  $t_{pZL}$  is measured at  $V_{CC}/2$ .  
 G.  $t_{pLZ}$  is measured at  $V_{OL} + 0.15\text{ V}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION**

$V_{CC} = 2.7 \text{ and } 3.3 \text{ V} \pm 0.3 \text{ V}$

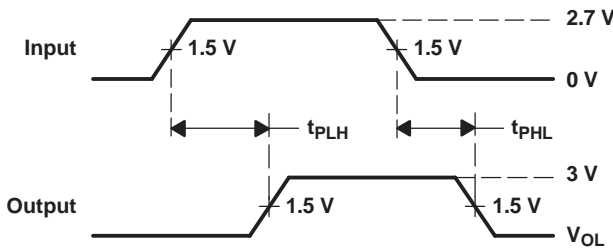


**LOAD CIRCUIT**

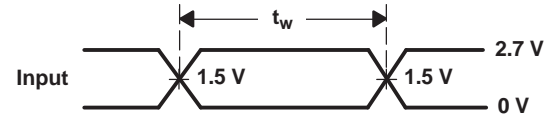
TEST	S1
$t_{pZL}$ (see Note F)	6 V
$t_{pLZ}$ (see Note G)	6 V
$t_{PHZ}/t_{PZH}$	6 V



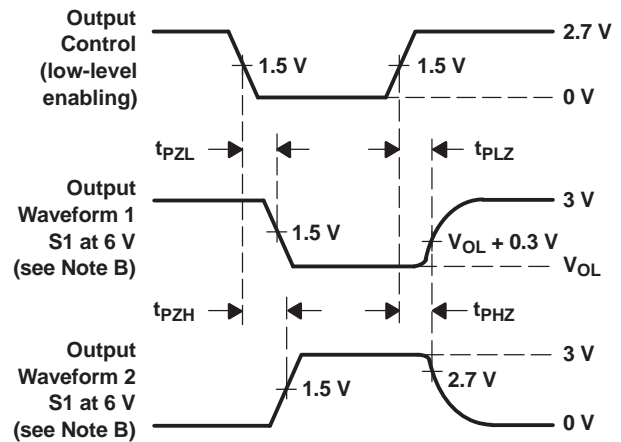
**VOLTAGE WAVEFORMS SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS PULSE DURATION**



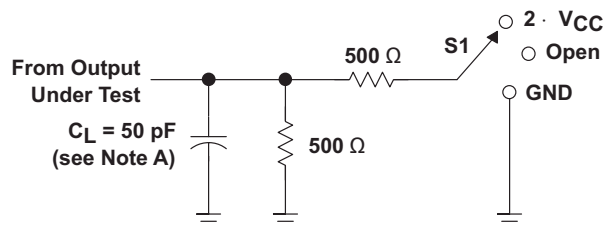
**VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES**

- NOTES: A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E. Since this device has open-drain outputs,  $t_{pLZ}$  and  $t_{pZL}$  are the same as  $t_{pd}$ .
- F.  $t_{pZL}$  is measured at 1.5 V.
- G.  $t_{pLZ}$  is measured at  $V_{OL} + 0.3 \text{ V}$ .
- H. All parameters and waveforms are not applicable to all devices.

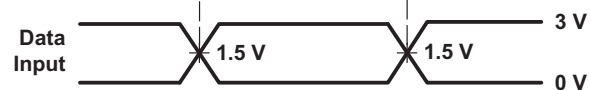
**Figure 3. Load Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION

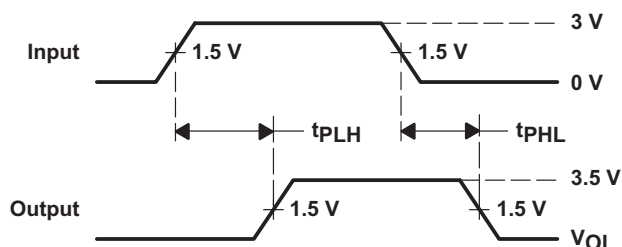
$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$



LOAD CIRCUIT

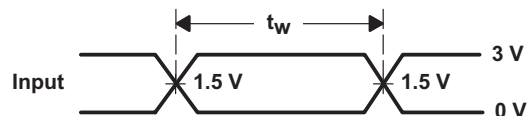


VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES

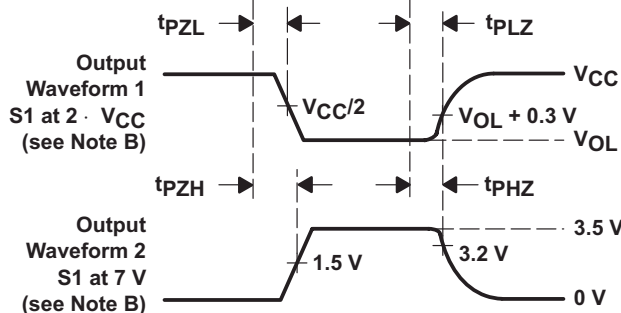
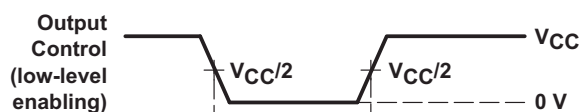


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES

TEST	S1
$t_{pZL}$ (see Note F)	2 · $V_{CC}$
$t_{pLZ}$ (see Note G)	2 · $V_{CC}$
$t_{PHZ}/t_{PZH}$	7 V



VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\text{ ns}$ ,  $t_f \leq 2.5\text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. Since this device has open-drain outputs,  $t_{pLZ}$  and  $t_{pZL}$  are the same as  $t_{pd}$ .  
 F.  $t_{pZL}$  is measured at  $V_{CC}/2$ .  
 G.  $t_{pLZ}$  is measured at  $V_{OL} + 0.3\text{ V}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

### REVISION HISTORY

Changes from Revision C (December, 2007) to Revision D	Page
• Changed from "Operates From 1.65 V to 3.6 V" to "Operates From 1.65 V to 5 V" .....	1
• Changed from "This hex buffer/driver is designed for 1.65-V to 3.6-V $V_{CC}$ operation" to "This hex buffer/driver is designed for 1.65-V to 5.5-V $V_{CC}$ operation" .....	1
• Changed supply voltage max value from 3.6 to 5.5 .....	2
• Added 4th PMI image .....	7



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC07AQPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC07AQ	<b>Samples</b>
SN74LVC07AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC07AQ	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LVC07A-Q1 :**

- Catalog: [SN74LVC07A](#)
- Enhanced Product: [SN74LVC07A-EP](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC07AQPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC07AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC07AQPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC07AQPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0

PW0014A



**PACKAGE OUTLINE**  
**TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE AND DISCLAIMER

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