TPS544E27 4V to 18V Input, 40A, Buck Converter With SVID and PMBus®

1 Features

- Single chip power supply for SVID rails
- Intel® VR14 and VR13 compliant
- VR14.Cloud compliant with telemetry level 2 and security level 2
- PMBus® 1.5 interface with NVM for configuration, telemetry (V/I/T), and fault reporting
- Input voltage: 4V to 18V
- Output voltage: 0.25V to 5.5V
- Supports external 5V bias improving efficiency and enabling 2.7V minimum input voltage
- Output current: 40A continuous and 50A peak
- Cycle-by-cycle valley I_{OUT} OCF limit programmable up to 50A
- Input power monitoring (PIN sense)
- Programmable DCM or FCCM operation
- Switching frequency: 400kHz to 2MHz
- Programmable internal loop compensation including droop (DC Load Line)
- Programmable soft-start time from 0.5ms to 16ms
- Programmable soft-stop time from 0.5ms to 4ms
- Programmable output voltage slew rate: 0.625mV/µs to 25mV/µs
- Programmable V_{IN} UVLO, V_{OUT} OVF/UVF, and OTF
- Safe start-up into prebiased outputs
- Precision voltage reference and differential remote sense for high output accuracy
  - ±0.5% tolerance from 0°C to 85°C junction
  - ±1% tolerance from –40°C to 125°C junction
- Analog output current output pin (IMON)
- D-CAP+™ control topology with fast transient response
- Open-drain power-good output (VRRDY)

2 Applications

- Server and cloud-computing POLs
- Hardware accelerator
- Network interface card
- Broadband, networking, and optical
- Wireless infrastructure

3 Description

The TPS544E27 device is highly integrated buck converter with D-CAP+ control topology for fast transient response. All programmable parameters can be configured by the PMBus interface and stored in non-volatile memory (NVM) as the new default values to minimize the external component count. These features make the device well-designed for space-constrained applications.

The TPS544E27 device is designed to work with Intel CPUs and fits well for single-phase, low-to-mid current SVID rails in the Intel server and SoC platforms requiring VR13, VR14, or VR14.Cloud compliance.

Fault management and status reports for the overcurrent fault (OCF), V_{OUT} overvoltage fault (OVF), undervoltage fault (UVF), and overtemperature fault are provided on the device. The TPS544E27 device provides a full set of telemetry, including output voltage, output current, and device temperature. Additionally, input power monitoring through an external sensing resistor is provided for board-level power management.

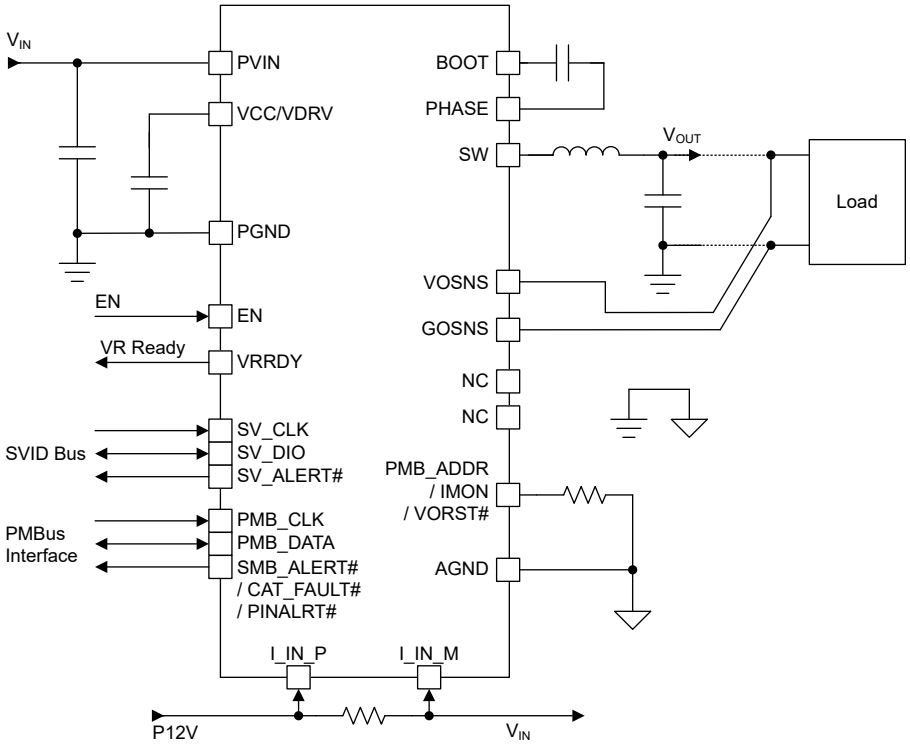
TPS544E27 is a lead-free device and is RoHS compliant without exemption.

Package Information

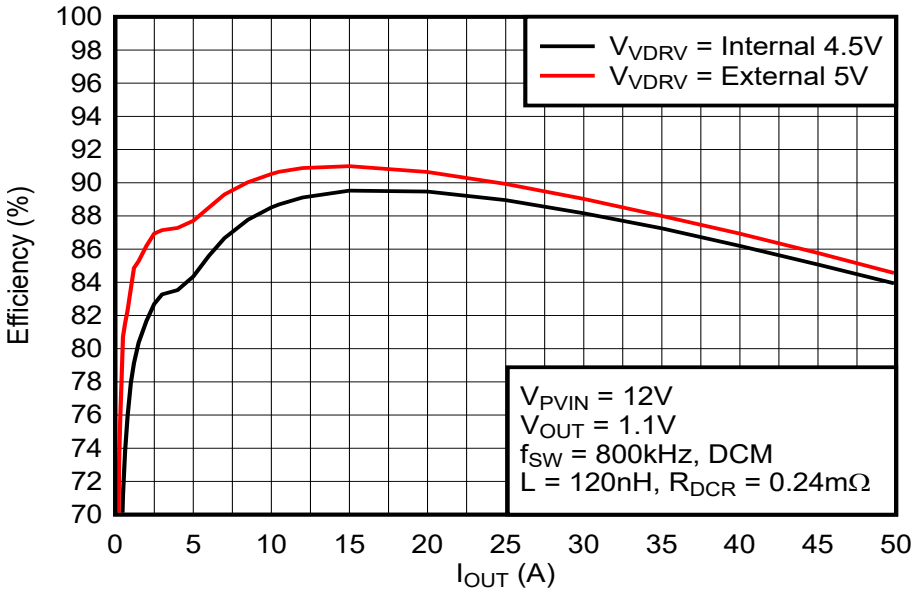
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TPS544E27	RXX (WQFN-FCRLF, 37)	5.00mm × 6.00mm

(1) For more information, see Section 7.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

ADVANCE INFORMATION



Simplified Schematic



Typical Efficiency

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4 Pin Configuration and Functions

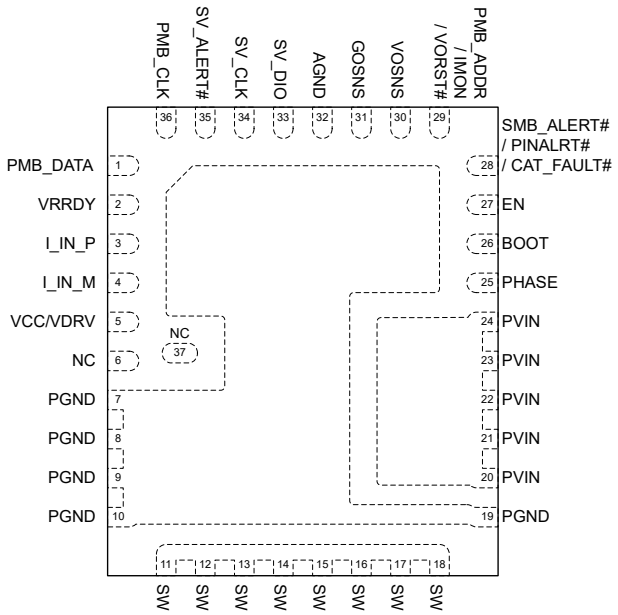

Figure 4-1. RXX 37-Pin WQFN-FCRLF Package (Top View)

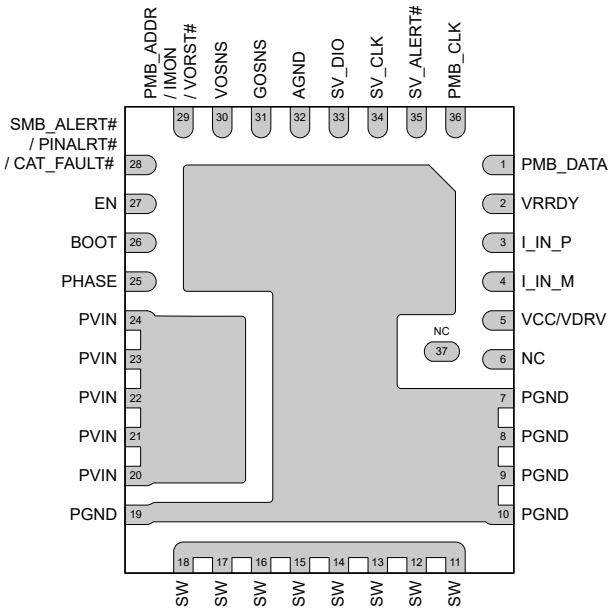

Figure 4-2. RXX 37-Pin WQFN-FCRLF Package (Bottom View)

Table 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
AGND	32	G	Ground pin, reference point for internal control circuitry
BOOT	26	P	Supply rail for the high-side gate driver (boost terminal). Connect the bootstrap capacitor from this pin to PHASE pin. A high temperature (X7R) 0.1µF or greater value ceramic capacitor is recommended.
EN	27	I	Enable pin, an active-high input pin that, when asserted high, causes the VR to begin the soft-start sequence for the output voltage rail. When deasserted low, the VR deasserts VRRDY and begins the shutdown sequence of the output voltage rail and continue to completion.
GOSNS	31	I	Negative input of the differential remote sense circuit, connect to the ground sense point on the load side.
I_IN_M	4	I	Connect to the negative side of the local input power sense resistor. Input voltage for VIN telemetry is also sensed at this pin. If input power sensing is not being used then connect I_IN_P and I_IN_M together, and connect both to PVIN for VIN telemetry. The pins can also be connected to ground or another voltage if VIN telemetry is not needed.
I_IN_P	3	I	Connect to the positive side of a local input power sense resistor. If input power sensing is not being used then connect I_IN_P to I_IN_M.
NC	6, 37	—	Not connected. These pins are floating internally.
PGND	7 – 10, 19	G	Power ground for the internal power stage
PHASE	25	O	Return for high-side MOSFET driver. Shorted to SW internally. Connect the BOOT pin bypass capacitor to this pin.
PMB_ADDR / IMON / VORST#	29	I/O	Multipurpose pin. During the device initialization, the PMBus address of the controller is set by tying an external resistor between this pin and AGND. For proper resistor detection, do not load this pin with more than 20pF during the device initialization at VCC power-up. DC_LL, VBOOT and OFFSET source 0 or 1 are selected as well. After device initialization, this pin can be used as an analog current monitor output. This pin is a current sense of low-side MOSFET. The analog IMON feature is enabled through the EN_AIMON bit. When using the IMON feature, do not load this pin with more than 50pF. This pin also performs a V_{OUT} reset function that can be enabled through the EN_VORST bit. If the EN_VORST bit is set, the analog IMON output is disabled.

Table 4-1. Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
PMB_CLK	36	I	PMBus serial clock pin
PMB_DATA	1	I/O	PMBus bi-directional serial data pin
PVIN	20 – 24	P	Power input for both the power stage and the analog circuit. PVIN is the input of the internal VCC LDO.
SMB_ALERT# / PINALRT# / CAT_FAULT#	28	O	Multipurpose open-drain output pin. 1. SMB_ALERT# is PMBus serial active low alert line. 2. PINALRT# function (active low) 3. CAT_FAULT# active low Catastrophic Fault indicator. The functionality can be selected through the SEL_ALRT_FN field in the PMBus (D0h) SYS_CFG_USER1 command.
SV_ALERT#	35	O	SVID active low ALERT# signal. This output is asserted to indicate the status of the VR has changed.
SV_CLK	34	I	SVID clock pin
SV_DIO	33	I/O	SVID bi-directional data pin
SW	11 – 18	O	Output switching terminal of the power converter. Connect these pins to the output inductor.
VCC/VDRV	5	P	Internal LDO output and also input for gate driver circuit. An external 5V bias can be connected to this pin to save the power losses on the internal LDO. The voltage source on this pin powers both the internal control circuitry and gate driver.
VOSNS	30	I	Positive input of the differential remote sense circuit, connect to the V_{OUT} sense point on the load side
VRRDY	2	O	Voltage regulator “Ready” output signal. The VRRDY indicator is asserted when the controller is ready to accept SVID commands after EN is asserted. VRRDY is also deasserted low when a shutdown fault occurs. This open-drain output requires an external pullup resistor.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

ADVANCE INFORMATION

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5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

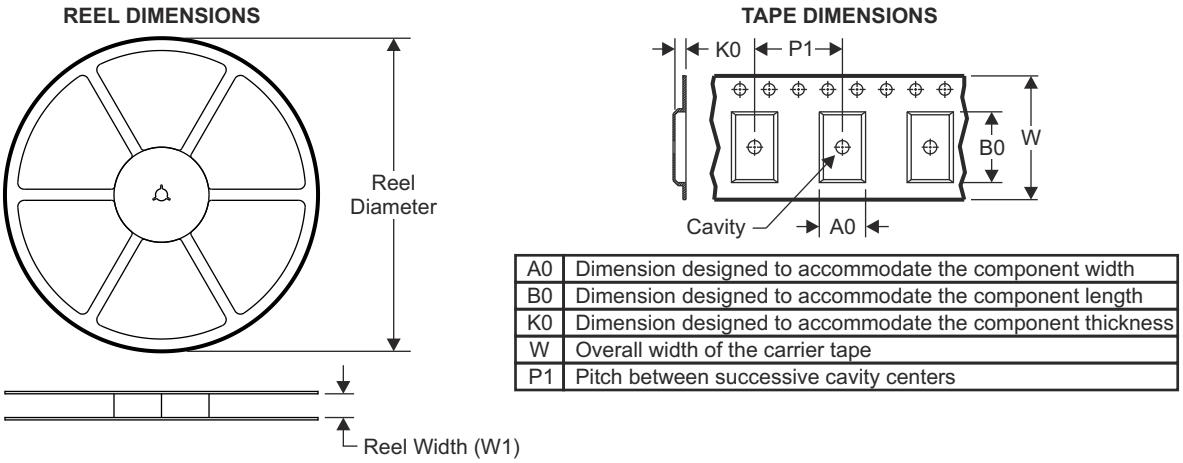
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2024	*	Initial Release

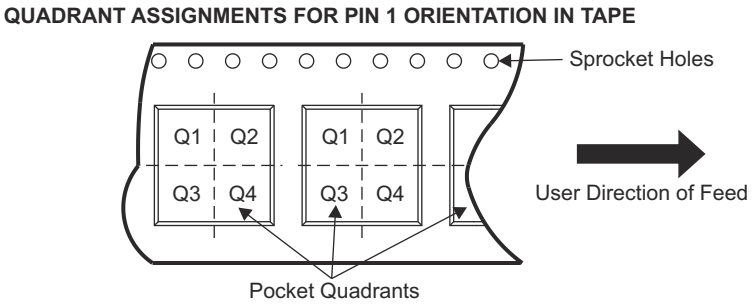
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PTPS544E27RXXR	WQFN-FCRLF	RXX	37	3000	330	12.4	5.25	6.3	1.0	8.0	12.0	Q1

ADVANCE INFORMATION

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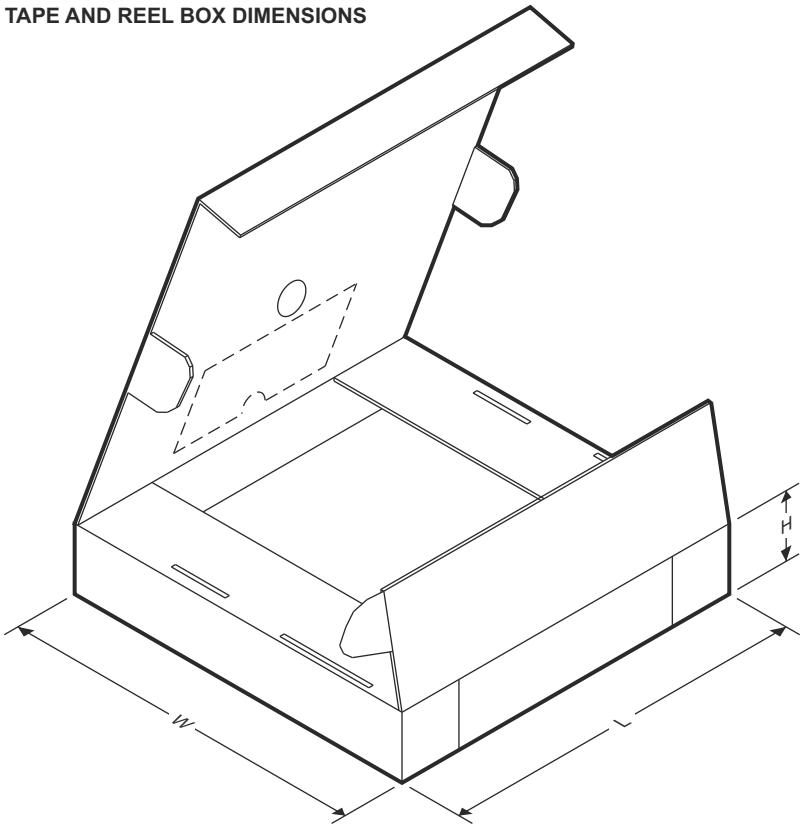
TAPE AND REEL BOX DIMENSIONS



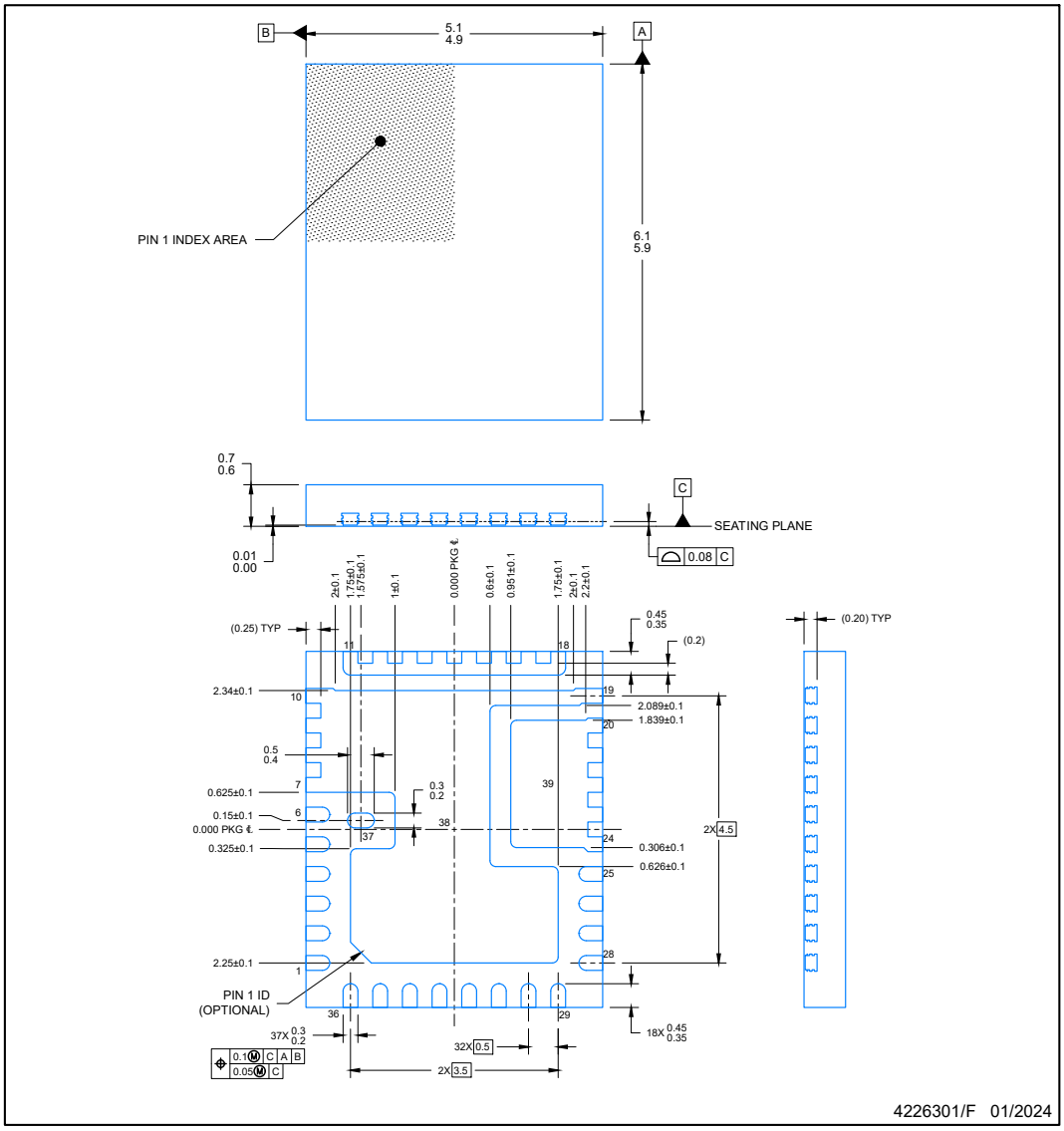
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PTPS544E27RXXR	WQFN-FCRLF	RXX	37	3000	338	355	50

PACKAGE OUTLINE

RXX0037A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



NOTES:

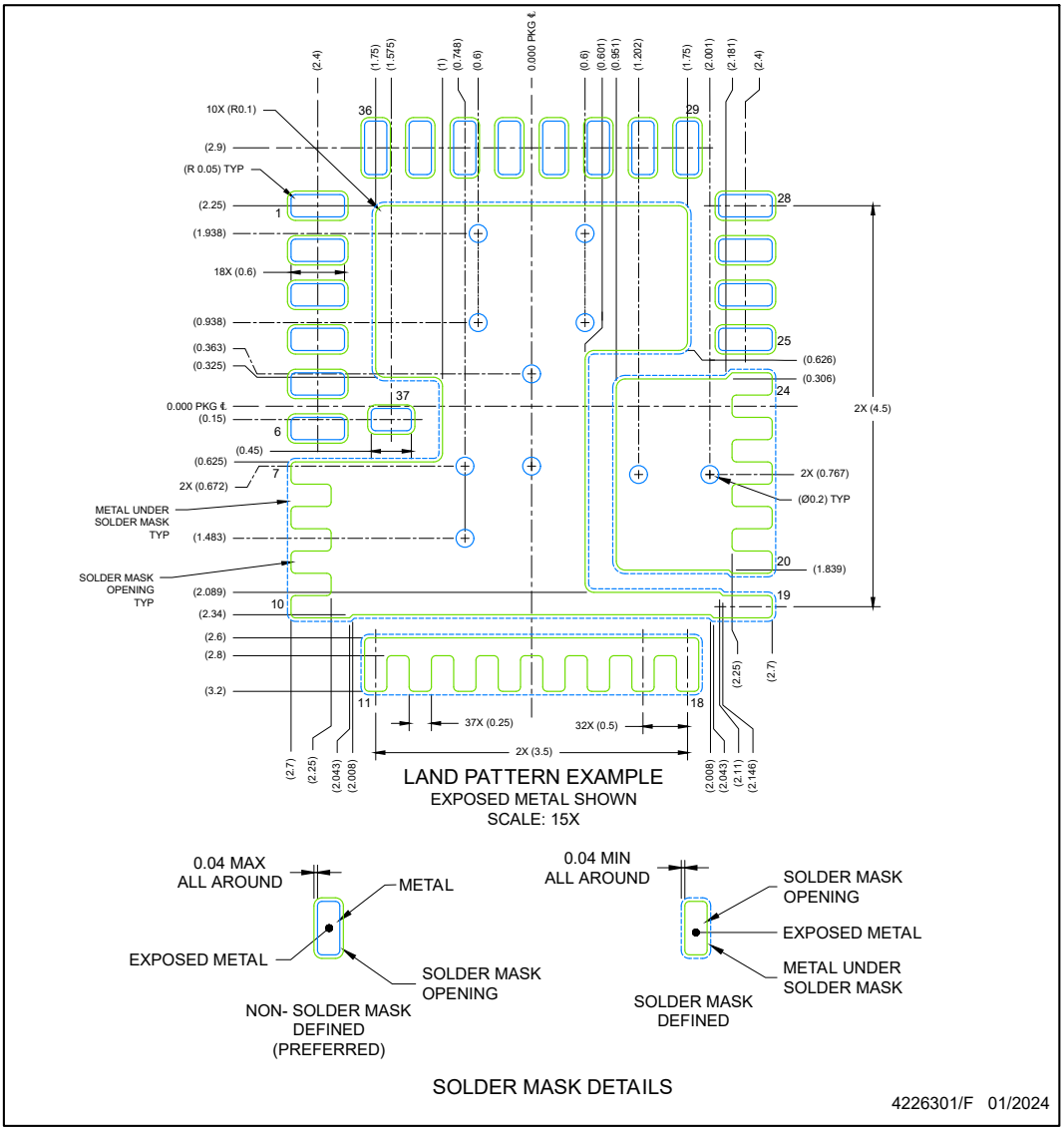
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RXX0037A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



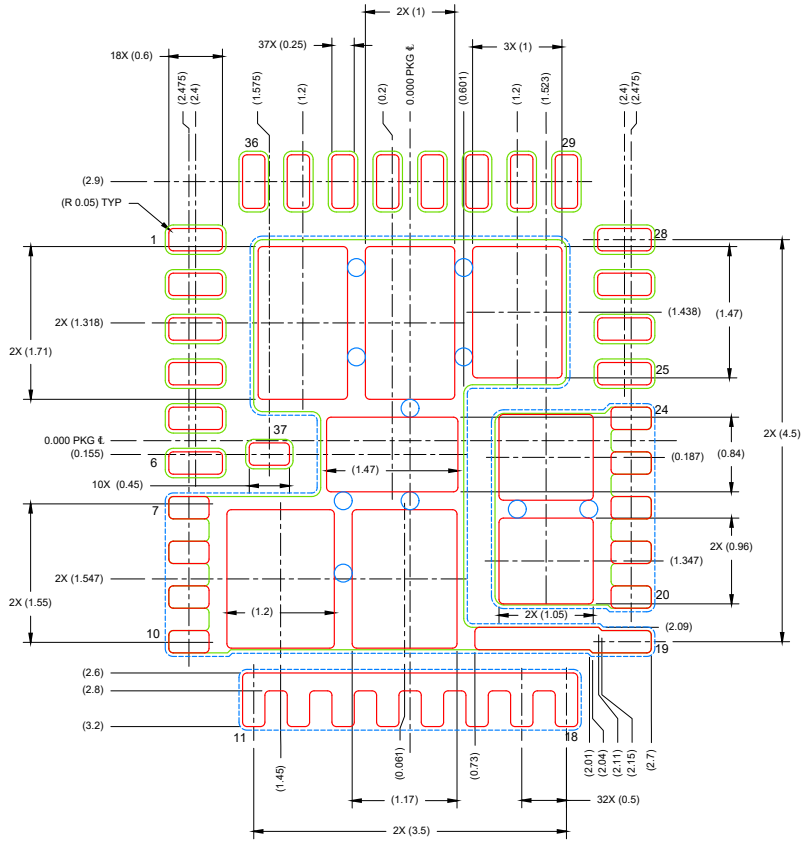
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
6. Recommended board layout is designed for 2oz copper for high current applications.

EXAMPLE STENCIL DESIGN

RXX0037A — **WQFN-FCRLF - 0.7 mm max height**

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SOLDER COVERAGE :
Thermal Pad connected to pin 7-10, 19 : 80%
Thermal Pad connected to pin 20-24 : 86%
SCALE: 15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS544E27RXXR	ACTIVE	WQFN-FCRLF	RXX	37	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

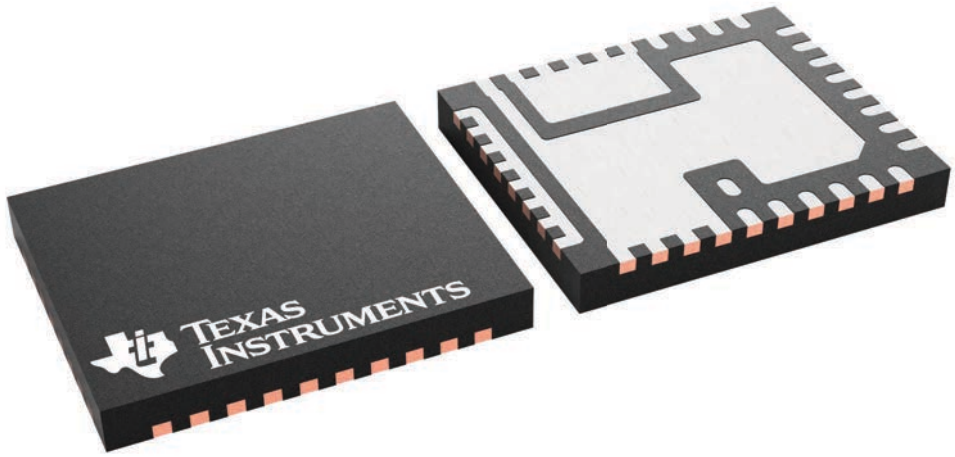
RXX 37

VQFN-FCRLF - 1.05 mm max height

5 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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