TPS736xx-Q1, Cap-Free, NMOS, 400-mA Low-Dropout Regulator With Reverse Current Protection

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Stable With No Output Capacitor or Any Value or Type of Capacitor
- Input Voltage Range of 1.7 V to 5.5 V
- Ultra-Low Dropout Voltage: 75-mV Typical
- Excellent Load Transient Response—With Or Without Optional Output Capacitor
- New NMOS Topology Delivers Low Reverse Leakage Current
- Low Noise: 30-μV_{RMS} Typical (10 Hz to 100 kHz)
- 0.5% Initial Accuracy
- 1% Overall Accuracy Over Line, Load, and Temperature
- Less Than 1-µA Maximum I_Q in Shutdown Mode
- Thermal Shutdown and Specified Minimum and Maximum Current Limit Protection
- Available in Multiple Output Voltage Versions
  - Fixed Outputs of 1.2 V to 3.3 V
  - Adjustable Output from 1.2 V to 5.5 V

2 Applications

- Infotainment
- ADAS
- Automotive Clusters
- Body Control Modules

3 Description

The TPS736xx-Q1 family of low-dropout (LDO) linear voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. It also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

The TPS736xx-Q1 uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1 µA and ideal for portable applications. The extremely low output noise (30 μV_{RMS} with 0.1-µF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS73601-Q1, TPS73625-Q1, TPS73633-Q1	SOT-23 (5)	2.90 mm 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application

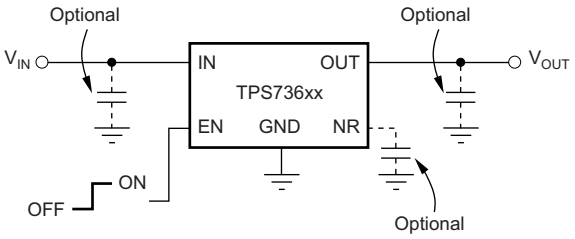


Table of Contents

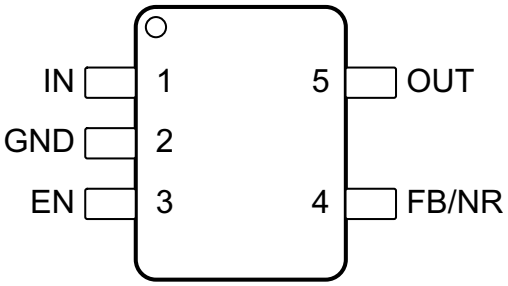
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2010) to Revision A	Page
• Added *Applications* section, *Device Information* table, *Table of Contents*, *Revision History* section, *Specifications* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Deleted *Ordering Information* table	1
• Moved operating ambient temperature specification from the *Electrical Characteristics* table to *Absolute Maximum Ratings*	3

5 Pin Configuration and Functions

DBV Package
5-Pin S0T-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See *Enable Pin and Shutdown* for more information. EN can be connected to IN if not used.
FB	4	I	FB pin for adjustable voltage version only—this is the input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	2	G	Ground
IN	1	P	Input supply
NR	4	I	NR pin for fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
OUT	5	P	Output of the regulator. There are no output capacitor requirements for stability.

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

	MIN	MAX	UNIT
V_{IN}	–0.3	6	V
V_{EN}	–0.3	6	V
V_{OUT}	–0.3	5.5	V
V_{NR}, V_{FB}	–0.3	6	V
Peak output current	Internally limited		
Output short-circuit duration	Indefinite		
Junction temperature, T_J	–40	150	°C
Operating ambient temperature, T_A	–40	125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Unregulated input voltage	1.7	5.5	V
V_O	Output voltage	0	5.5	V
I_{OUT}	Output current	0	500	mA

6.4 Thermal Information

THERMAL METRIC(1)		TPS73601-Q1, TPS73625-Q1, TPS73633-Q1 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	221.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	74.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating temperature range (T_A = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V(1), I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage(1)(2)			1.7		5.5	V
V_{FB}	Internal reference (TPS73601)		T_J = 25°C	1.198	1.2	1.21	V
V_{OUT}	Output voltage (TPS73601)(3)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1)(4)	Nominal	T_J = 25°C	–0.5%		0.5%	
		over V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V; 10 mA ≤ I_{OUT} ≤ 400 mA	–1%	±0.5%	1%	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation(1)		$V_{O(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1 mA ≤ I_{OUT} ≤ 400 mA		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 400 mA		0.0005		
V_{DO}	Dropout voltage(5) (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)		I_{OUT} = 400 mA		75	200	mV
Z_O(DO)	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	400	650	800	mA
			3.6 V ≤ V_{IN} ≤ 4.2 V, 0°C ≤ T_J ≤ 70°C	500		800	mA
I_{SC}	Short-circuit current		V_{OUT} = 0 V		450		mA
I_{REV}	Reverse leakage current(6) ($-I_{IN}$)		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1	10	µA
I_{GND}	GND pin current		I_{OUT} = 10 mA (I_Q)		400	550	µA
			I_{OUT} = 400 mA		800	1000	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5, –40°C ≤ T_J ≤ 100°C		0.02	1.3	µA
I_{FB}	FB pin current (TPS73601)				0.1	0.45	µA

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6 V, when V_{IN} ≤ 1.6 V, the output locks to V_{IN} and may result in a damaging over-voltage level on the output. To avoid this situation, disable the device before powering down the V_{IN}.
(3) TPS73601 is tested at V_{OUT} = 2.5 V.
(4) Tolerance of external resistors not included in this specification.
(5) V_{DO} is not measured for fixed output versions with $V_{OUT(nom)}$ < 1.8 V.
(6) Fixed-voltage versions only; see *Application and Implementation* for more information.

Electrical Characteristics (continued)

Over operating temperature range (T_A = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V[(1)], I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100 Hz, I_{OUT} = 400 mA		58		dB
		f = 10 KHz, I_{OUT} = 400 mA		37		
V_N	Output noise voltage BW = 10 Hz – 100 KHz	C_{OUT} = 10 µF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
		C_{OUT} = 10 µF, C_{NR} = 0.01 µF		8.5 × V_{OUT}		
t_{STR}	Start-up time	V_{OUT} = 3 V, R_L = 30 Ω C_{OUT} = 1 µF, C_{NR} = 0.01 µF		600		µs
V_{EN}(HI)	EN pin high (enabled)		1.7		V_{IN}	V
V_{EN}(LO)	EN pin low (shutdown)		0		0.5	V
I_{EN}(HI)	EN pin current (enabled)	V_{EN} = 5.5 V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

6.6 Typical Characteristics

For all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

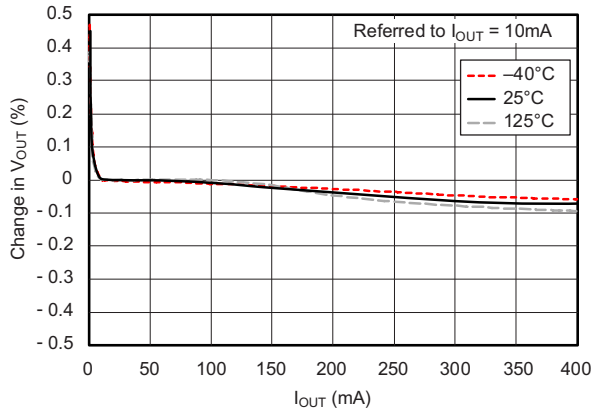


Figure 1. Load Regulation

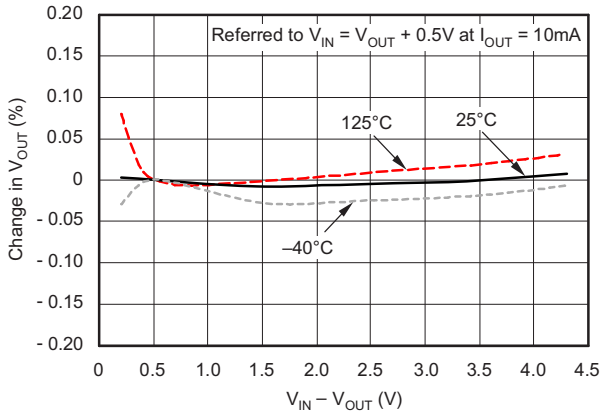


Figure 2. Line Regulation

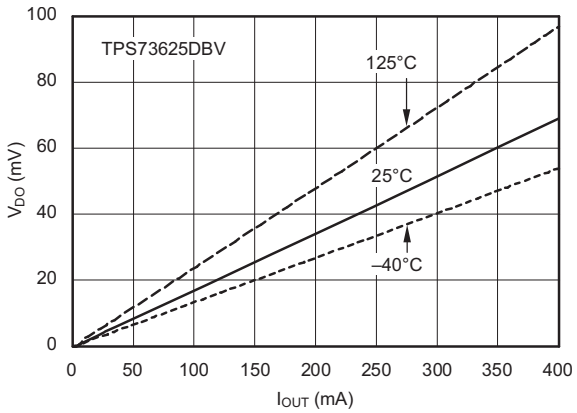


Figure 3. Dropout Voltage vs Output Current

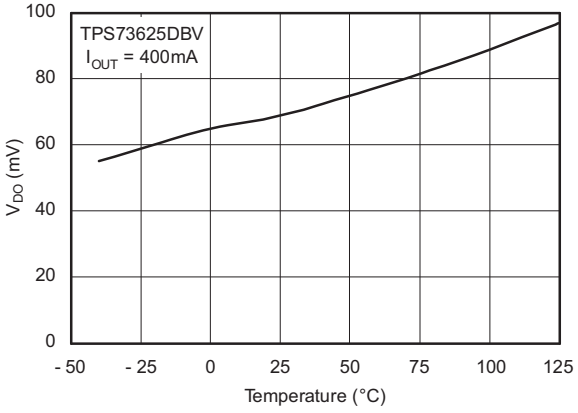


Figure 4. Dropout Voltage vs Temperature

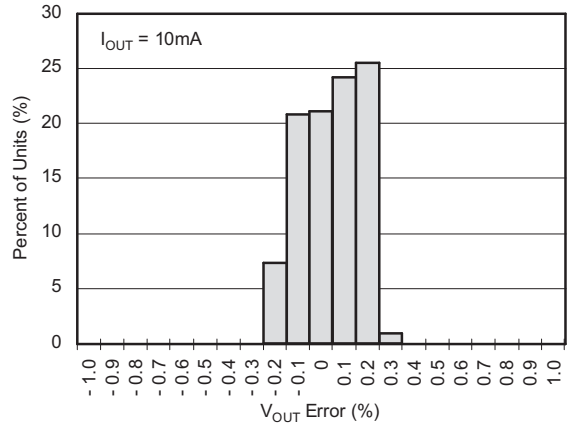


Figure 5. Output Voltage Accuracy Histogram

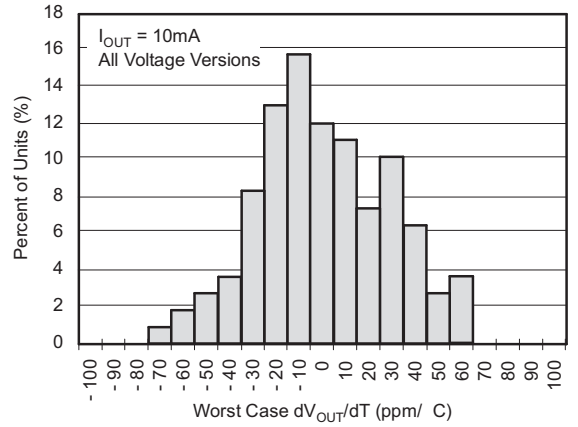


Figure 6. Output Voltage Drift Histogram

Typical Characteristics (continued)

For all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

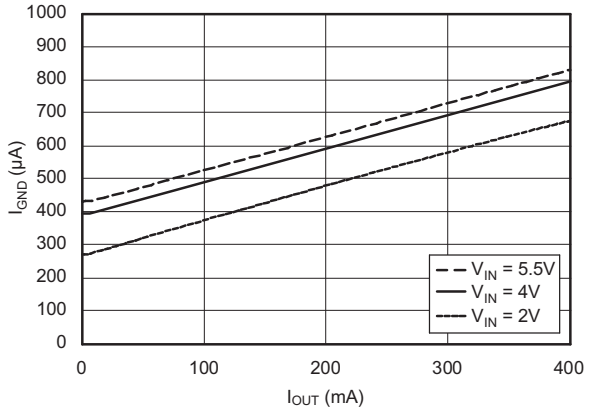


Figure 7. Ground Pin Current vs Output Current

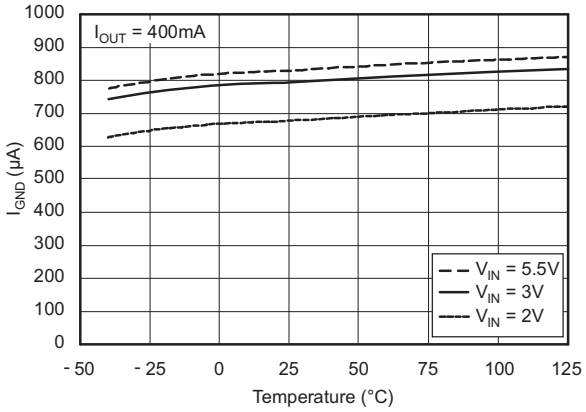


Figure 8. Ground Pin Current vs Temperature

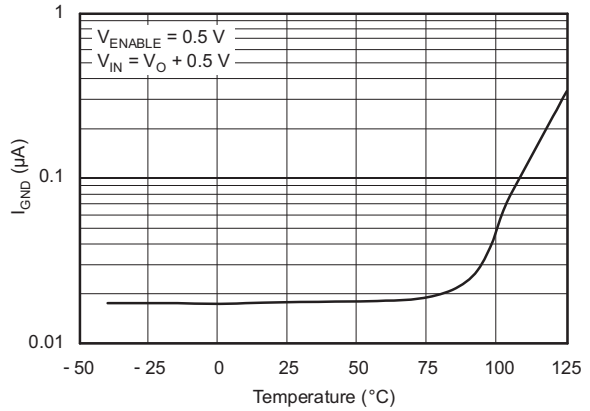


Figure 9. Ground Pin Current in Shutdown vs Temperature

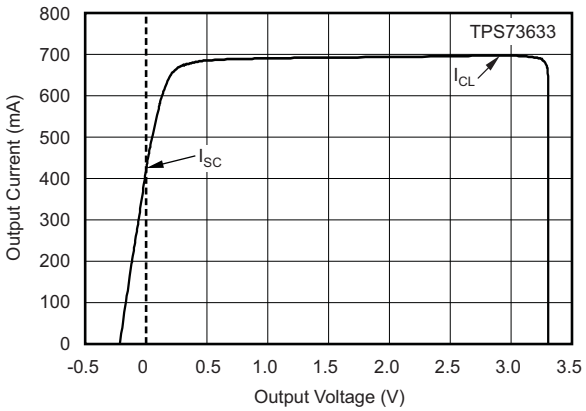


Figure 10. Current Limit vs V_{OUT} (Foldback)

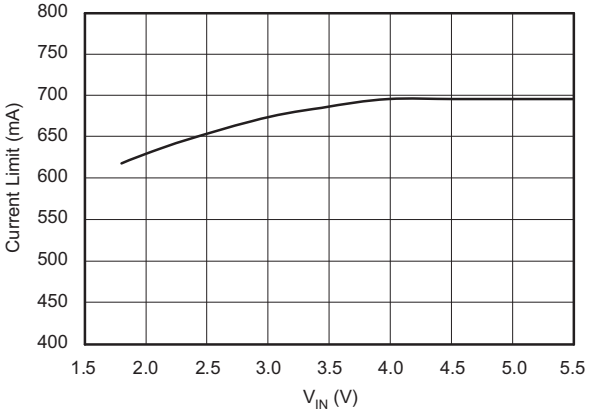


Figure 11. Current Limit vs V_{IN}

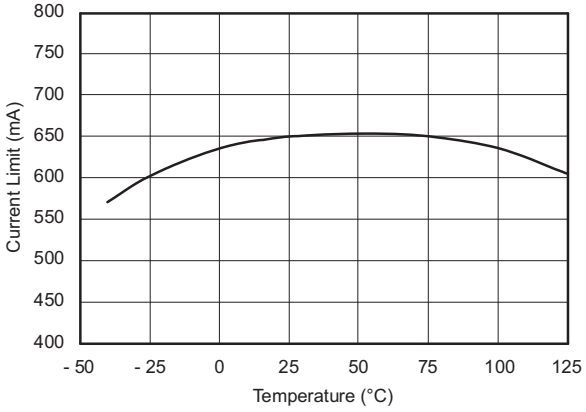


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

For all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

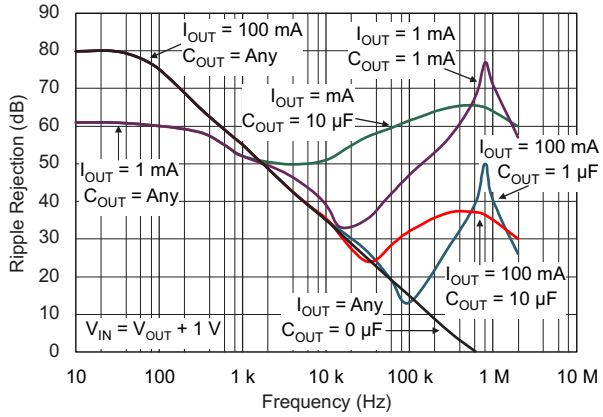


Figure 13. PSRR (Ripple Rejection) vs Frequency

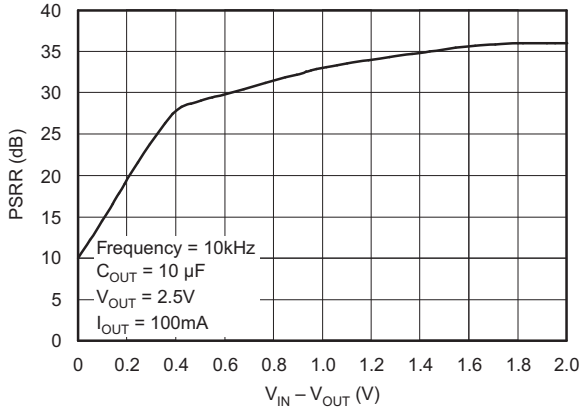


Figure 14. PSRR (Ripple Rejection) vs V_{IN} – V_{OUT}

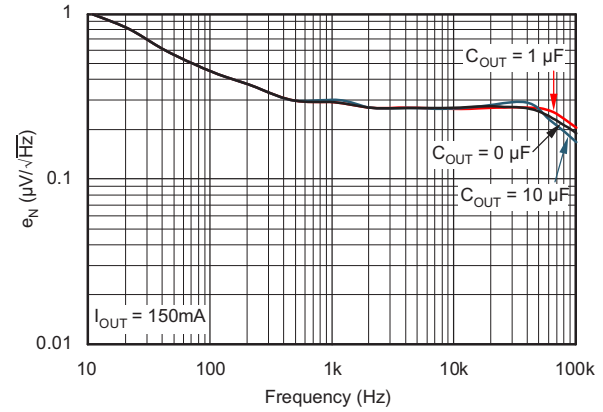


Figure 15. Noise Spectral Density C_{NR} = 0 µF

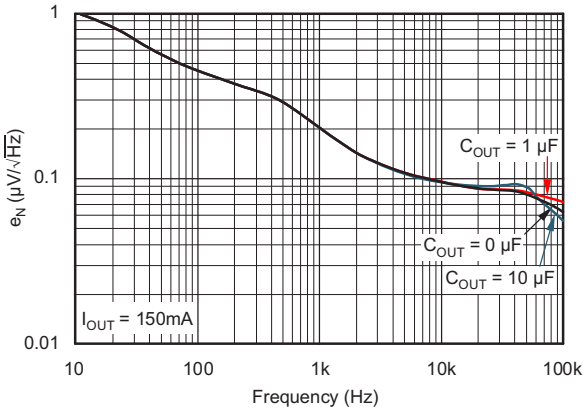


Figure 16. Noise Spectral Density C_{NR} = 0.01 µF

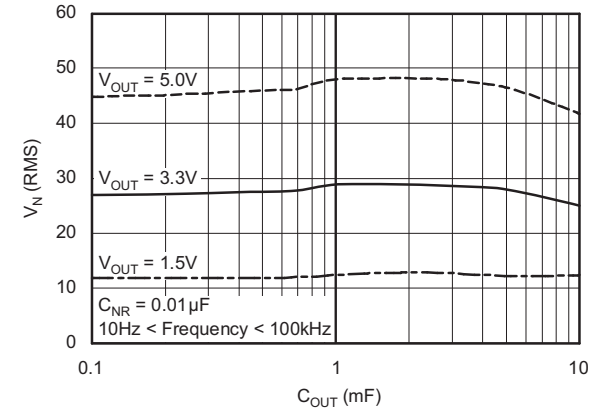


Figure 17. RMS Noise Voltage vs C_{OUT}

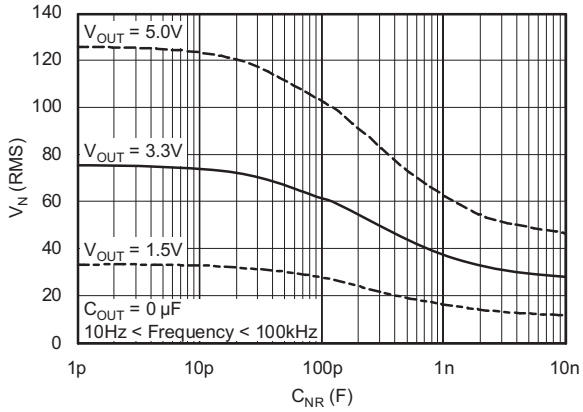


Figure 18. RMS Noise Voltage vs C_{NR}

Typical Characteristics (continued)

For all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

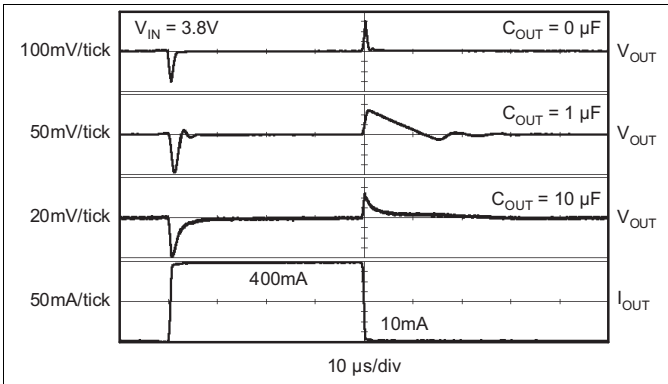


Figure 19. TPS73633 Load Transient Response

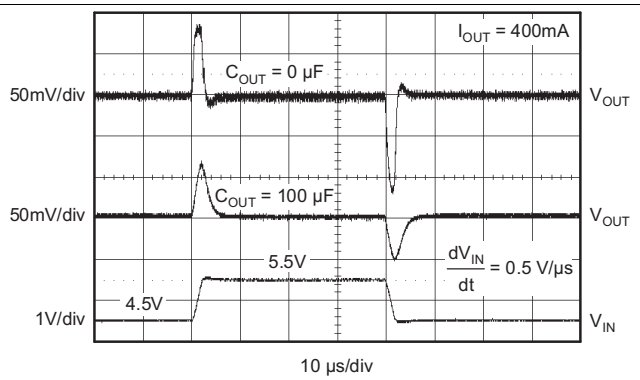


Figure 20. TPS73633 Line Transient Response

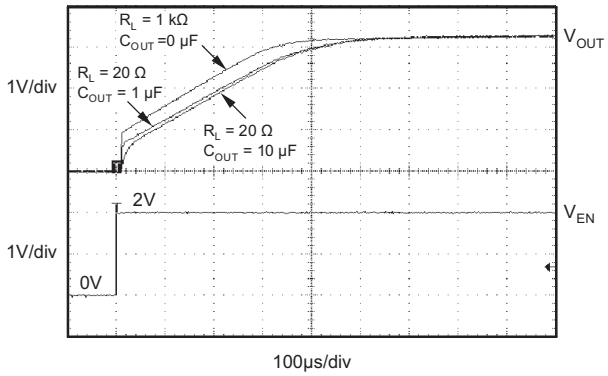


Figure 21. TPS73633 Turnon Response

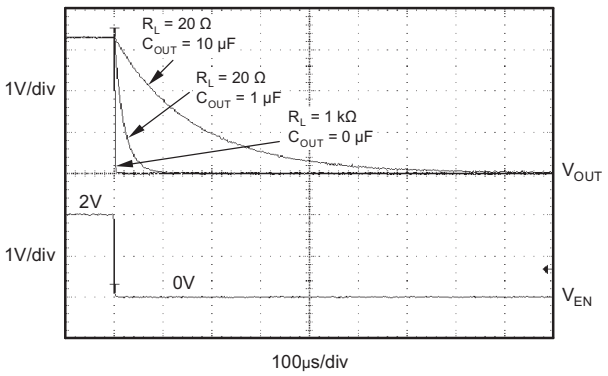


Figure 22. TPS73633 Turnoff Response

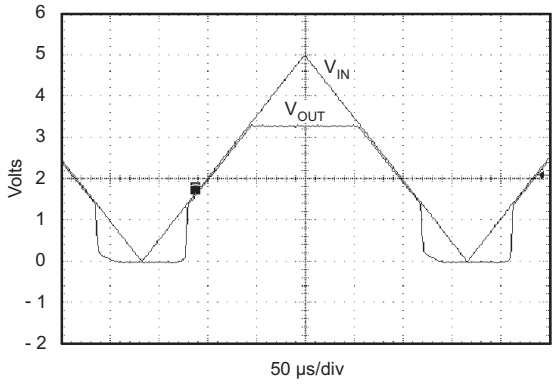


Figure 23. TPS73633 Power Up and Power Down

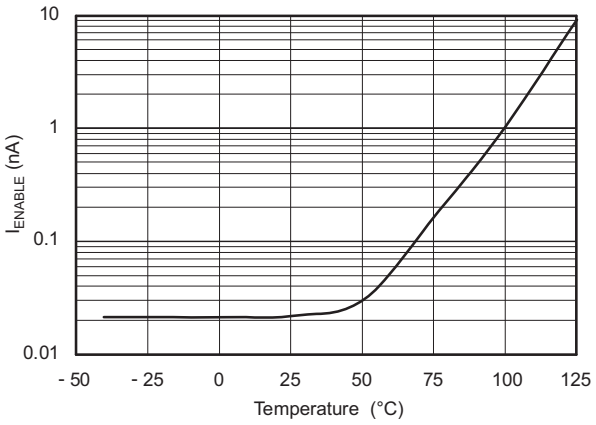


Figure 24. I_{ENABLE} vs Temperature

Typical Characteristics (continued)

For all voltage versions, at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted.

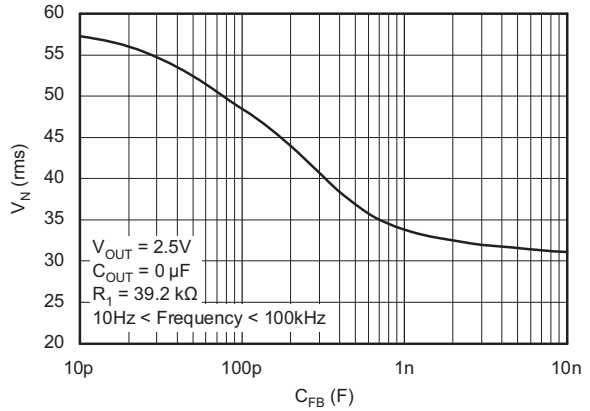


Figure 25. TPS73601 RMS Noise Voltage vs C_{FB}

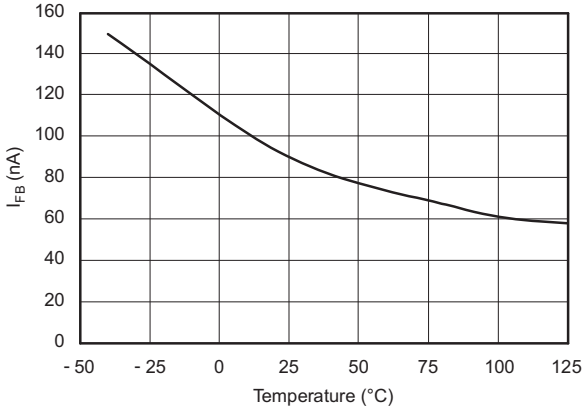


Figure 26. TPS73601 I_{FB} vs Temperature

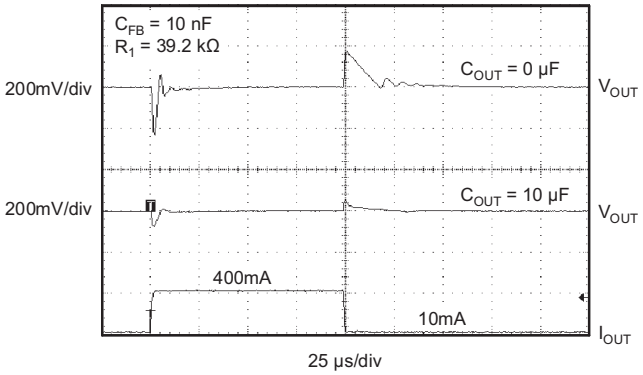


Figure 27. TPS73601 Load Transient, Adjustable Version

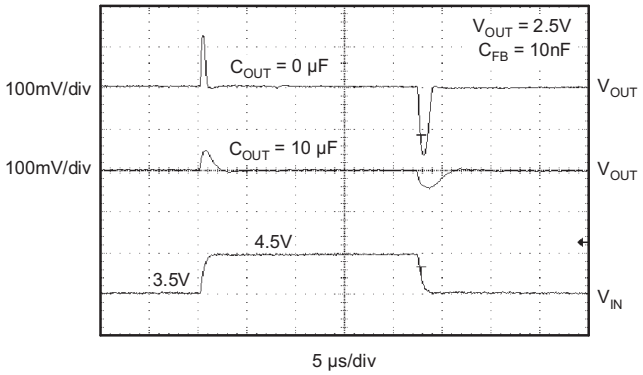


Figure 28. TPS73601 Line Transient, Adjustable Version

7 Detailed Description

7.1 Overview

The TPS736xx-Q1 belongs to a family of new-generation LDO regulators that use an NMOS pass transistor to achieve ultra-low dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS736xx-Q1 ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and overcurrent protection, including foldback current limit.

7.2 Functional Block Diagrams

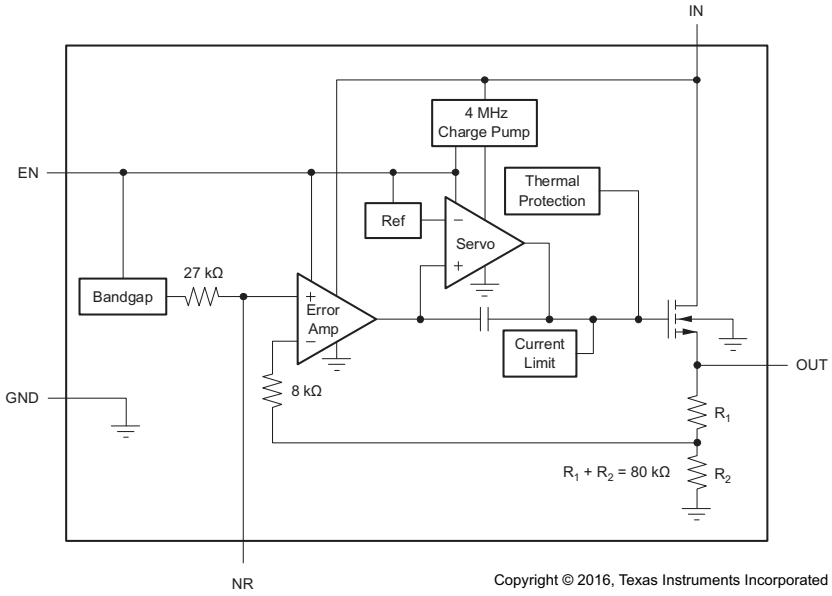
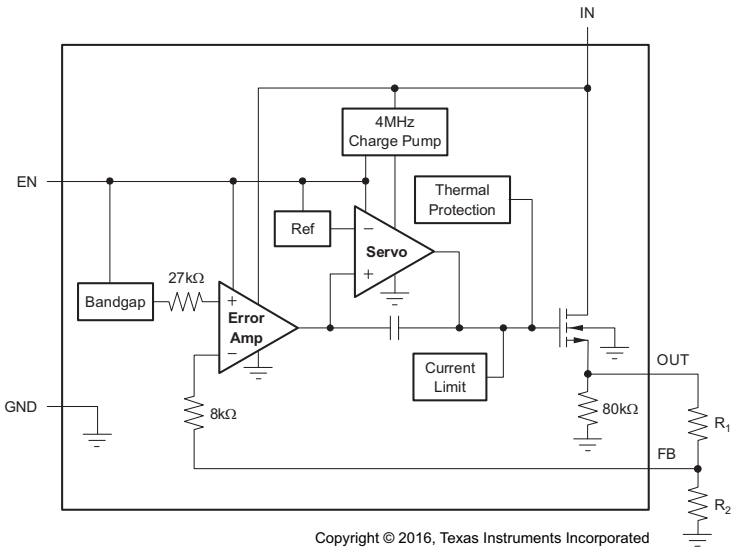


Figure 29. Fixed Voltage Version



See Table 1 for standard resistor values.

Figure 30. Adjustable Voltage Version

Table 1. Standard 1% Resistor Values for Common Output Voltages

V_{OUT}(1)	R_1	R_2
1.2 V	Short	Open
1.5 V	23.2 kΩ	95.3 kΩ
1.8 V	28 kΩ	56.2 kΩ
2.5 V	39.2 kΩ	36.5 kΩ
2.8 V	44.2 kΩ	33.2 kΩ
3 V	46.4 kΩ	30.9 kΩ
3.3 V	52.3 kΩ	30.1 kΩ

(1) V_{OUT} = (R1 + R2) / R2 × 1.204; R1 || R2 ≅ 19 kΩ for best accuracy.

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS736xx-Q1 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V (see Figure 10). Approximately –0.2 V of V_{OUT} results in a current limit of 0 mA. Therefore, if OUT is forced below –0.2 V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS736xx-Q1 must be enabled first.

7.3.2 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value of 1 µF) from the OUT pin to ground reduces undershoot magnitude but increase its duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin also improves the transient response.

The TPS736xx-Q1 does not have active pulldown when the output is overvoltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal and external load resistance. The rate of decay is given by Equation 1 or Equation 2, determined by the version.

Fixed voltage version

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \,||\, R_{LOAD}} \quad (1)$$

Adjustable voltage version

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \,||\, (R_1 + R_2) \,||\, R_{LOAD}} \quad (2)$$

7.3.3 Reverse Current

The NMOS pass element of the TPS736xx-Q1 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. The reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There is additional current flowing into the OUT pin due to the 80-kΩ internal resistor divider to ground (see Figure 29 and Figure 30).

For the TPS73601, reverse current may flow when V_{FB} is more than 1 V above V_{IN}.

Feature Description (continued)

7.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection must trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS736xx-Q1 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TPS736xx-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5 V (maximum) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see Figure 21).

When shutdown capability is not required, EN can be connected to V_{IN}. However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power-up.

Current limit foldback can prevent device start-up under some conditions. See the *Internal Current Limit* section for more information.

7.4.2 Dropout Voltage

The TPS736xx-Q1 uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the NMOS pass element.

For large step changes in load current, the TPS736xx-Q1 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of V_{IN} – V_{OUT} above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to DC dropout levels], the TPS736xx-Q1 can take a couple of hundred microseconds to return to the specified regulation accuracy.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 34. Sample resistor values for common output voltages are shown in Figure 30.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19 kΩ. This 19 kΩ, in addition to the internal 8-kΩ resistor, presents the same impedance to the error amp as the 27-kΩ bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

8.2 Typical Applications

8.2.1 Typical Application Circuit for Fixed-Voltage Versions

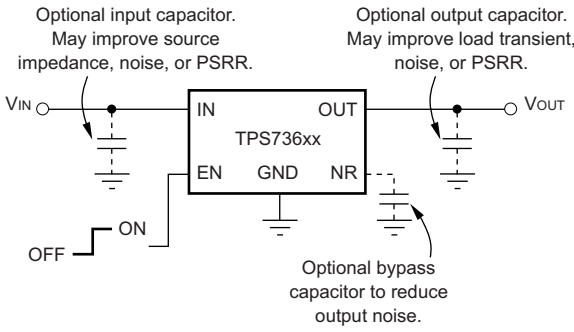


Figure 31. Typical Application Circuit for Fixed-Voltage Versions

8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters (Fixed-Voltage Version)

PARAMETER	EXAMPLE VALUE
Input voltage	5 V, ±3%
Output voltage	3.3 V, ±1%
Output current	500 mA (maximum), 20 mA (minimum)
RMS noise, 10 Hz to 100 kHz	< 30 μV_{RMS}
Ambient temperature	55°C (maximum)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Input And Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS736xx-Q1 does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 nΩF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

8.2.1.2.2 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS736xx-Q1 and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by Equation 3.

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \tag{3}$$

Because the value of V_{REF} is 1.2 V, this relationship reduces to Equation 4.

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \tag{4}$$

for the case of no C_{NR}.

An internal 27-kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship in Equation 5:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V) \tag{5}$$

for C_{NR} = 10 nF.

This noise reduction effect is shown in Figure 18 in *Typical Characteristics*.

The TPS73601 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improves load transient performance.

The TPS736xx-Q1 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250-μV of switching noise at approximately 4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

8.2.1.3 Application Curves

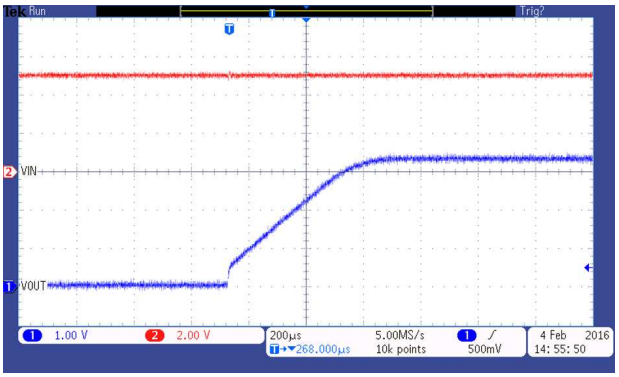


Figure 32. TPS73601 Start-Up

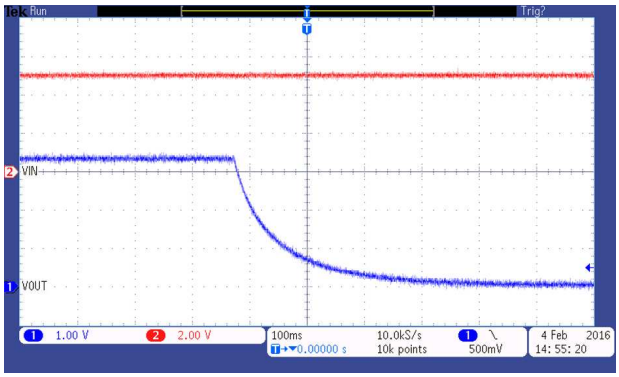


Figure 33. TPS73601 Shutdown

8.2.2 Typical Application Circuit for Adjustable-Voltage Version

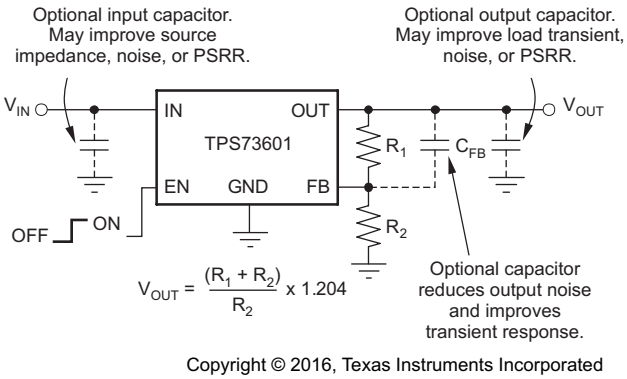


Figure 34. Typical Application Circuit for Adjustable-Voltage Version

8.2.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters (Adjustable-Voltage Version)

PARAMETER	EXAMPLE VALUE
Input voltage	5 V, ±3%, provided by the DC-DC converter switching at 1 MHz
Output voltage	2.5 V, ±1%
Output current	0.4 A (maximum), 10 mA (minimum)
RMS noise, 10 Hz to 100 kHz	< 35 μV_{RMS}
Ambient temperature	55°C (maximum)

9 Power Supply Recommendations

This device is designed to operate with an input supply range of 1.7 V to 5.5 V. If the input supply is noisy, additional input capacitors with low ESR can help improve output noise performance.

10 Layout

10.1 Layout Guidelines

Solder pad footprint recommendations for the TPS736xx-Q1 are presented in *Solder Pad Recommendations for Surface-Mount Devices*, SBFA015.

10.2 Layout Example

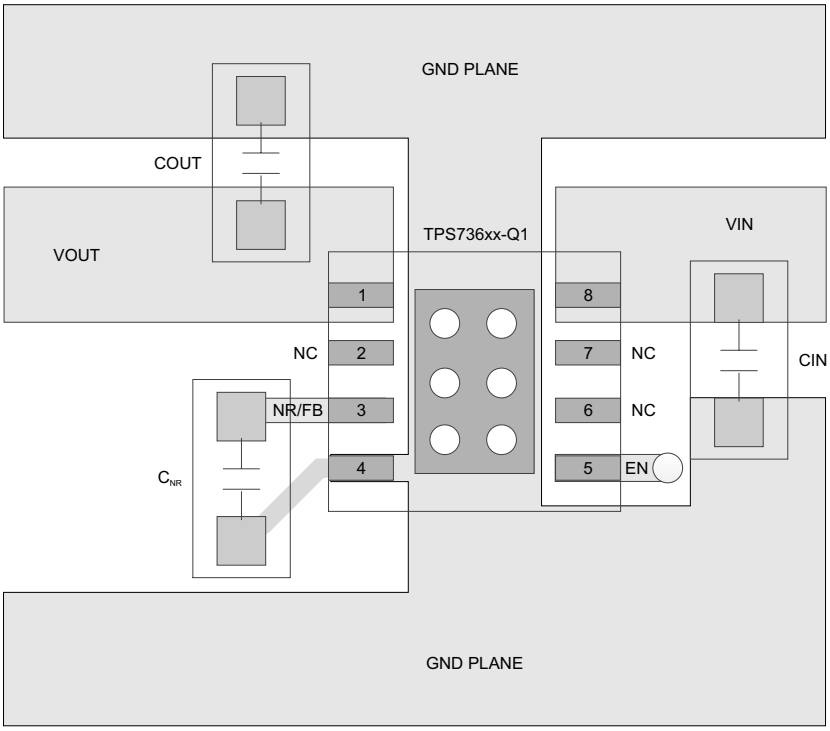


Figure 35. Fixed-Output Voltage Option Layout

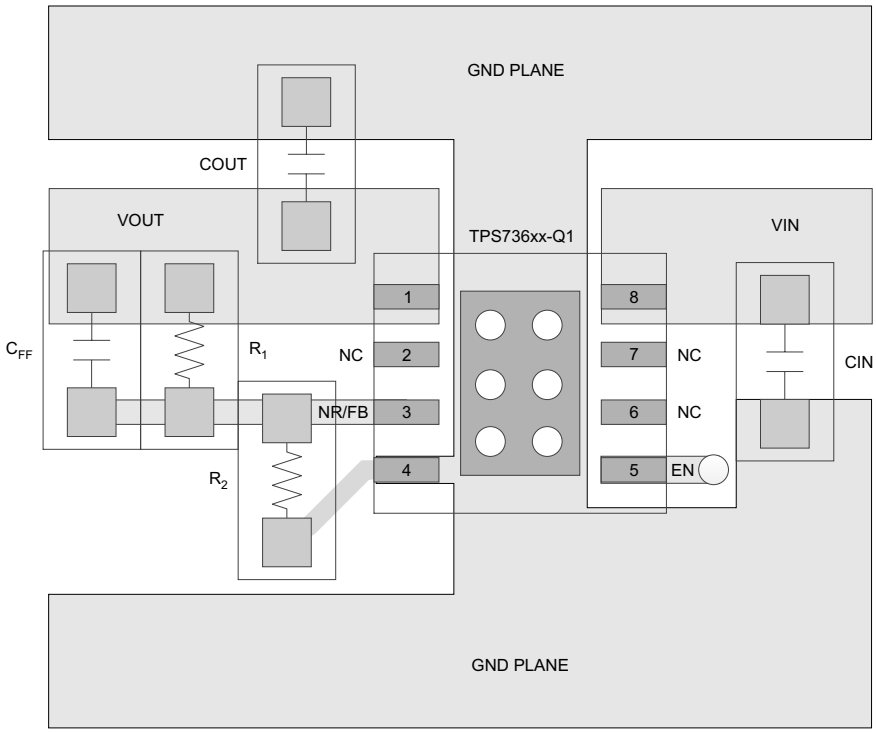


Figure 36. Adjustable-Output Voltage Option Layout

10.3 Thermal Considerations

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improve the heat sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), shown in Equation 6:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

10.4 Power Dissipation

To improve AC performance such as PSRR, output noise, and transient response, TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

11 Device And Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Solder Pad Recommendations for Surface-Mount Devices, SBFA015

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS73601-Q1	Click here	Click here	Click here	Click here	Click here

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73601QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PTWQ	Samples
TPS73618QDCQRQ1	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	73618Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS736-Q1 :

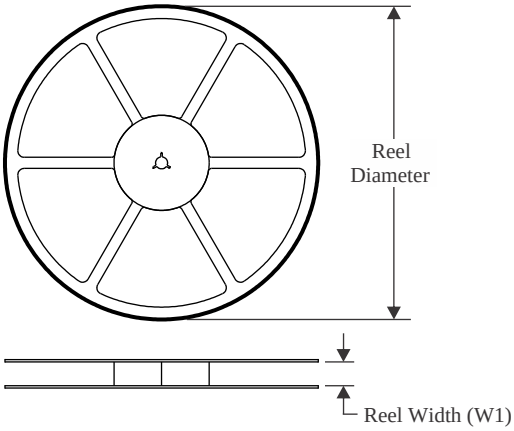
- Catalog: TPS736

NOTE: Qualified Version Definitions:

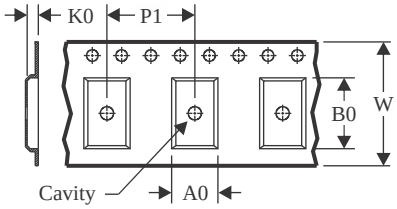
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

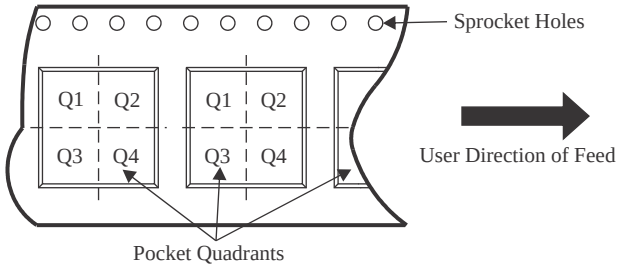


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

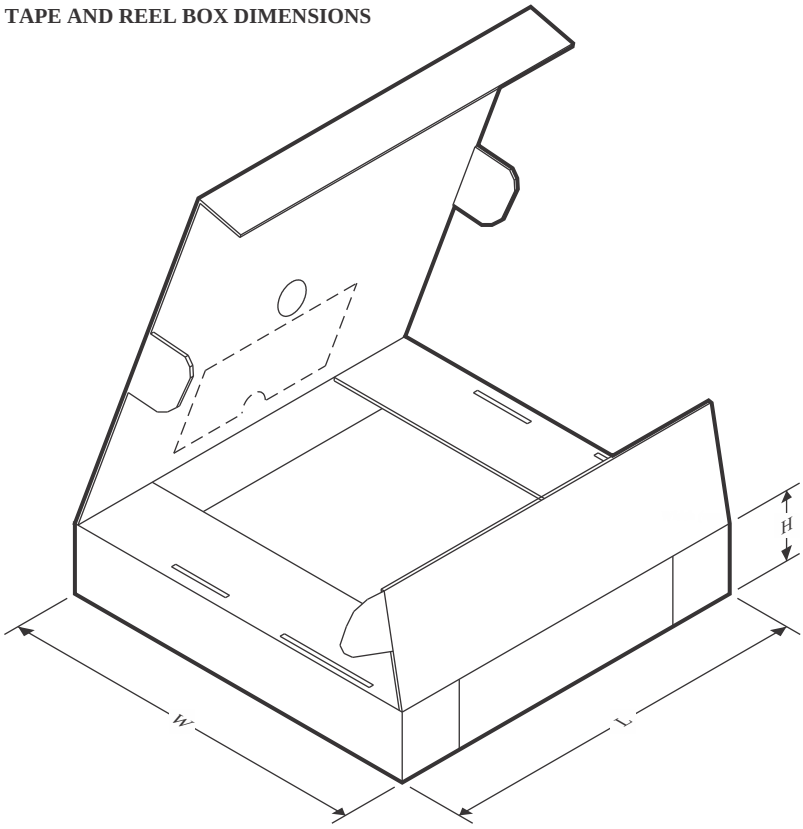
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73601QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73618QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

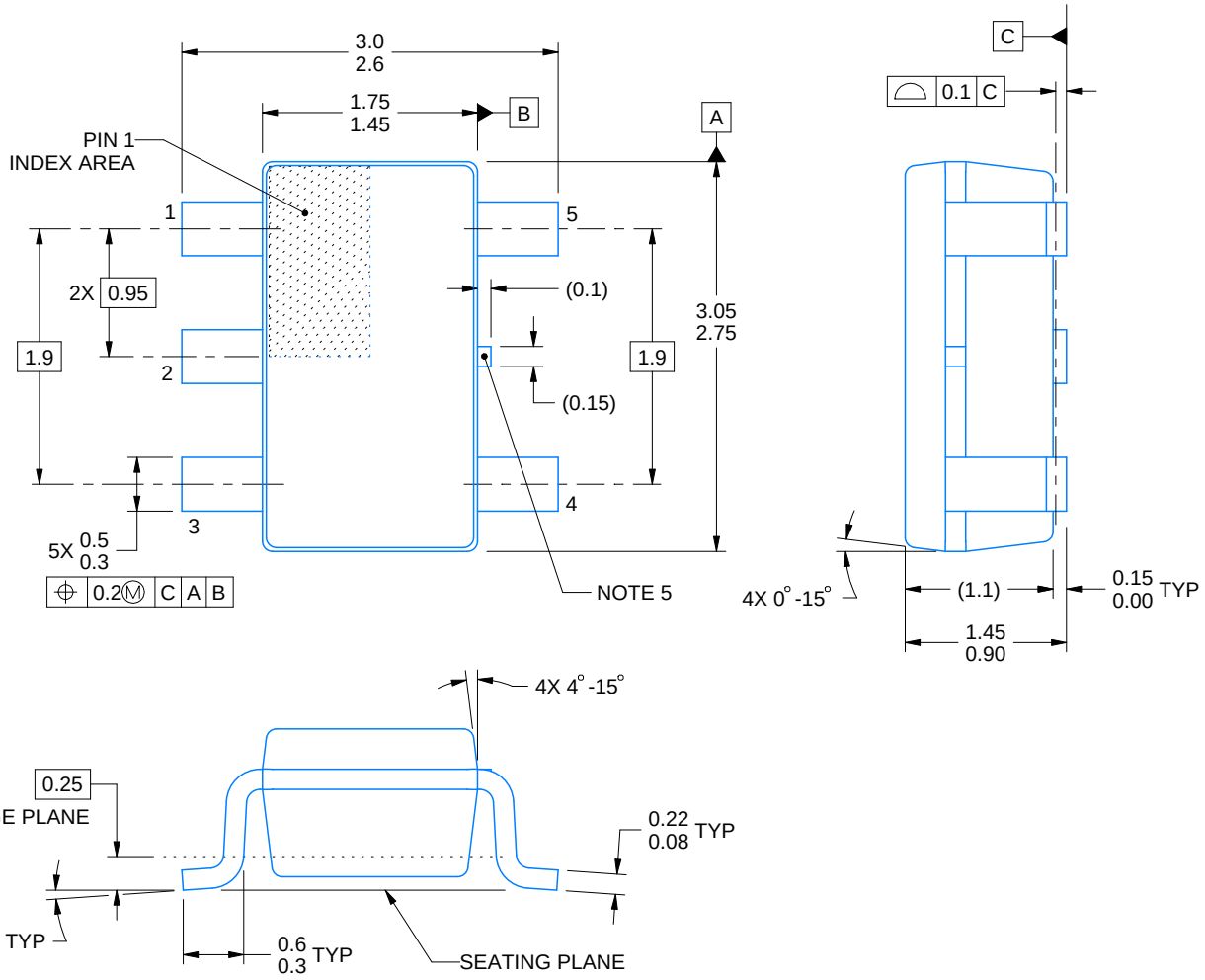
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73601QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73618QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

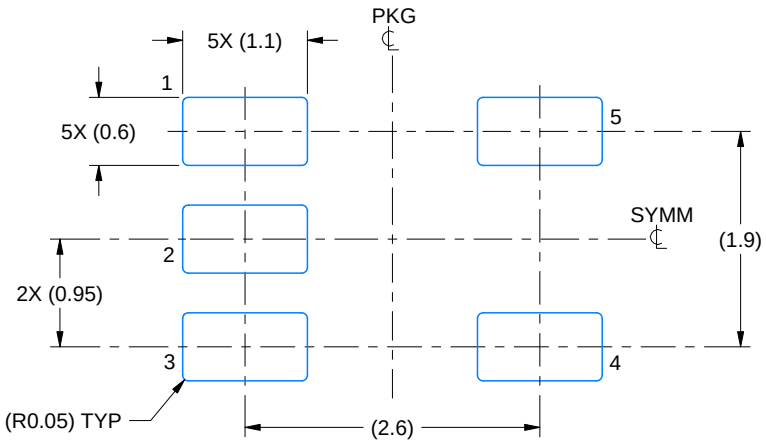
SMALL OUTLINE TRANSISTOR



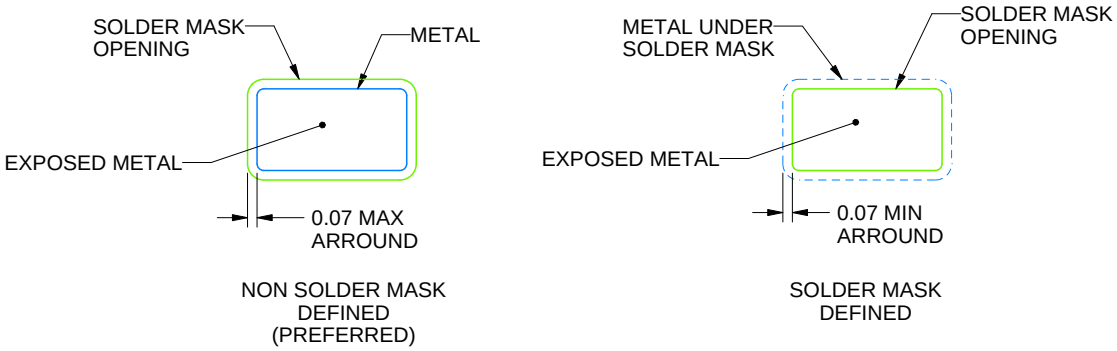
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

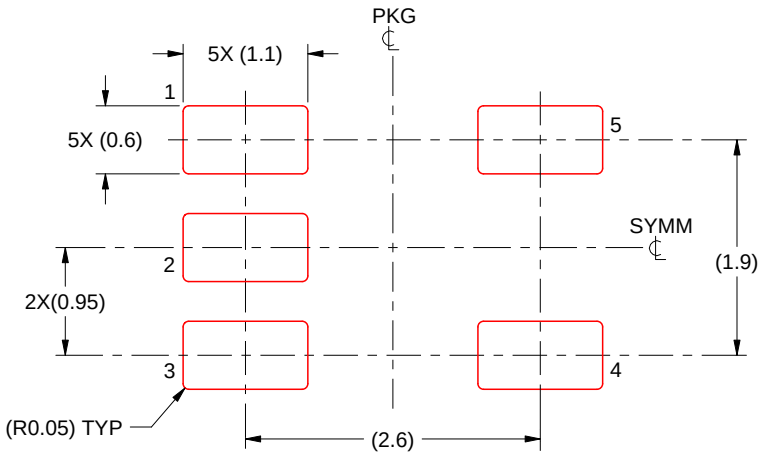


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

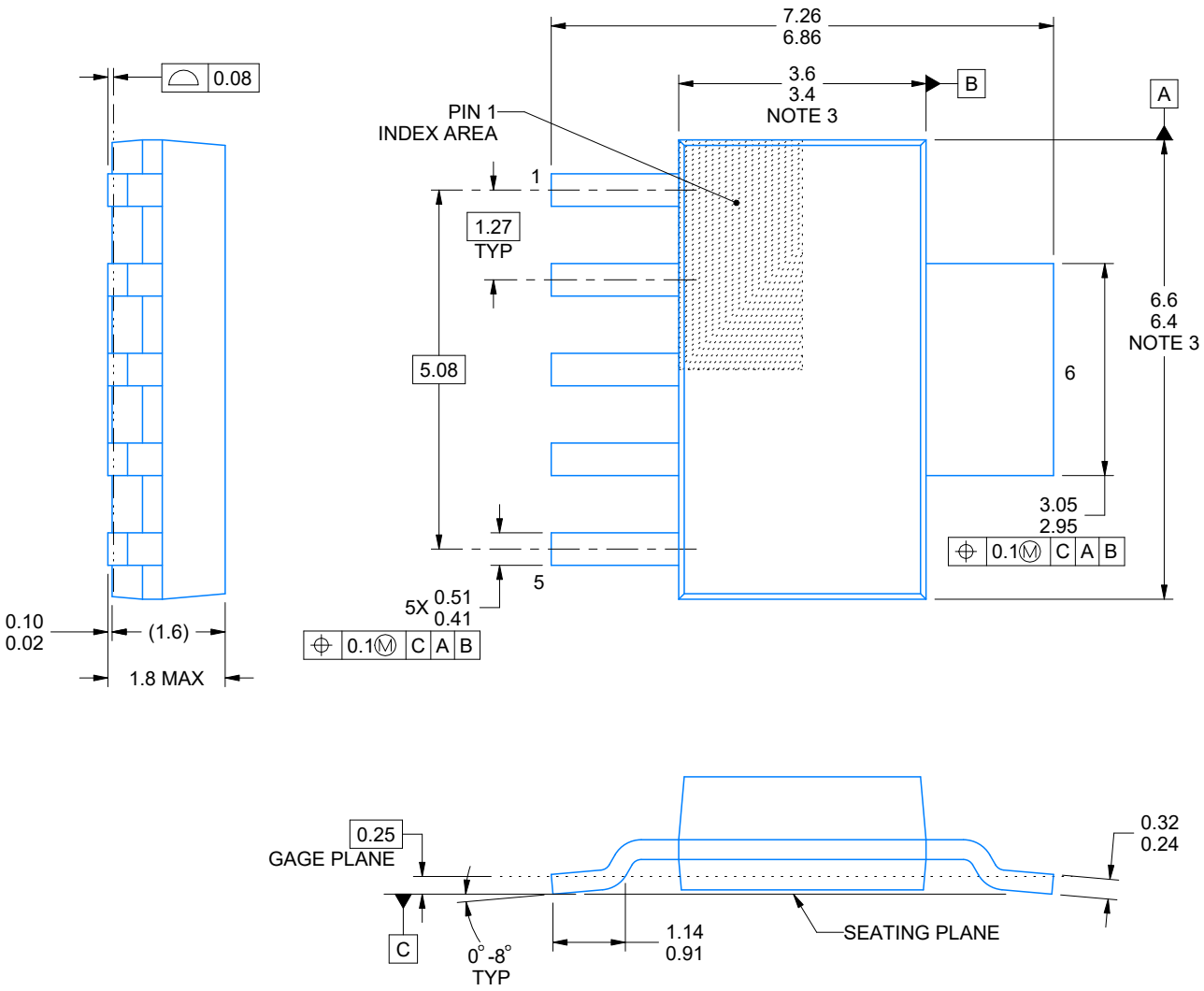
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

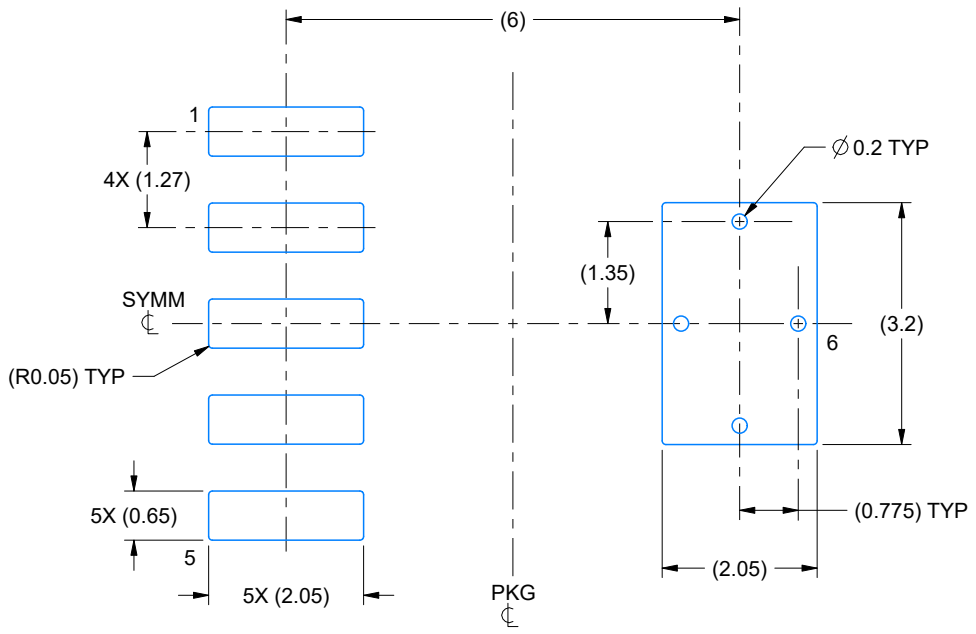
PLASTIC SMALL OUTLINE



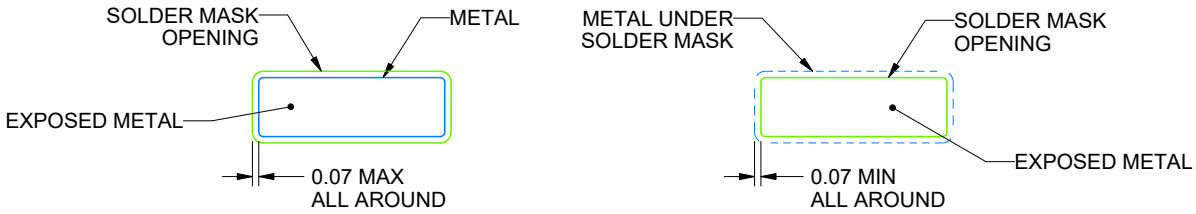
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

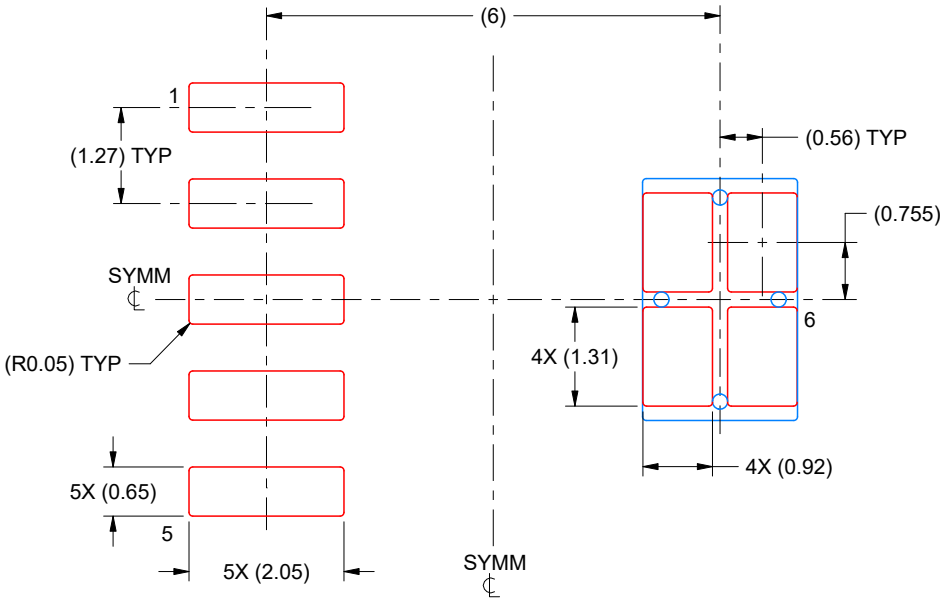


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265