TS5A21366 0.75-Ω 2-channel SPST Analog Switch With 1.8-V Compatible Input Logic

1 Features

- 2-Channel Single-Pole Single-Throw (SPST) Switch
- 1.65-V to 5.5-V Power Supply (V_{CC})
- Isolation in Power-Down Mode, V_{CC} = 0
- Low ON-State Resistance (0.75 Ω Typical)
- Excellent ON-State Resistance Matching
- Low Charge Injection
- Low Total Harmonic Distortion (THD+N)
- High Bandwidth (260 MHz)
- 1.8-V Compatible Control Input Threshold Independent of V_{CC}
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Cell Phones
- PDAs
- Portable Instrumentation
- Audio and Video Signal Routing
- Portable Media Players
- Communication Circuits
- Computer Peripherals

3 Description

The TS5A21366 is a bidirectional, 2-channel, single-pole single-throw (SPST) analog switch that is designed to operate from 1.65-V to 5.5-V supply voltages. The device offers a low ON-state resistance and an excellent channel-to-channel ON-state resistance matching. The device has excellent total harmonic distortion (THD+N) performance and consumes very low power.

The control pin can be connected to a low voltage GPIO allowing it to be controlled by 1.8-V signals.

These features make this device ideal for portable audio applications.

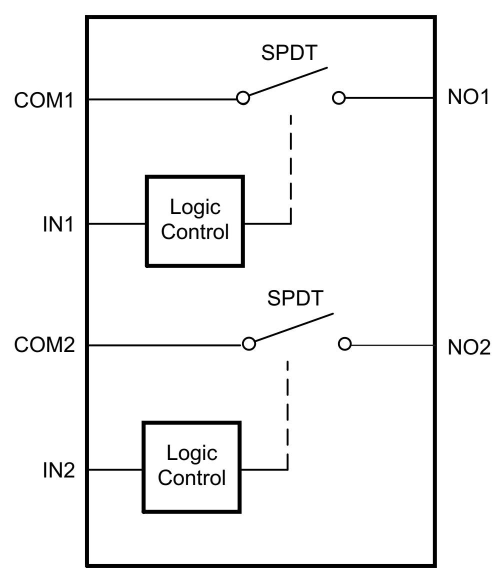
The TS5A21366 is available in a small, space-saving 8-pin DCU or RSE package, and is characterized for operation over the free-air temperature range of –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TS5A21366	VSSOP (8)	2.30 mm × 2.00 mm
	UQFN (8)	1.50 mm × 1.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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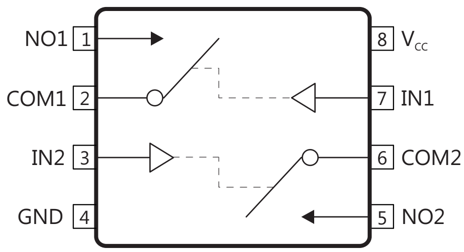
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

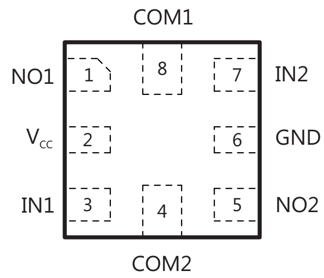
Changes from Revision A (October 2009) to Revision B	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1
• Changed V_+ to V_{CC} in the pinout drawings	3
• Deleted V_{CC}, V_{NO} row from *Electrical Characteristics for 5-V Supply*	5
• Deleted V_{CC}, V_{NO} row from *Electrical Characteristics for 3.3-V Supply*	7
• Deleted V_{CC}, V_{NO} row from *Electrical Characteristics for 2.5-V Supply*	9
• Deleted V_{CC}, V_{NO} row from *Electrical Characteristics for 1.8-V Supply*	11

5 Pin Configuration and Functions

DCU Package
8-Pin VSSOP
Top View



RSE Package
8-Pin UQFN
Top View



Pin Functions

PIN			DESCRIPTION
NAME	VSSOP	UQFN	
NO1	1	1	Switch 1, normally open
COM1	2	8	Switch 1, common
IN2	3	7	Switch 2, digital control pin to connect COM to NO LOW = High impedance signal path from NO pin to COM pin HIGH = NO pin connected to COM pin
GND	4	6	Digital ground
NO2	5	5	Switch 2, normally open
COM2	6	4	Switch 2, common
IN1	7	3	Switch 1, digital control pin to connect COM to NO LOW = High impedance signal path from NO pin to COM pin HIGH = NO pin connected to COM pin
V_{CC}	8	2	Power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

			MIN	MAX	UNIT
V_{CC}	Supply voltage[3]		–0.5	6.5	V
V_{NO} V_{COM}	Analog voltage[3][4][5]		–0.5	V_{CC} + 0.5	V
I_K	Analog port diode current	V_{NO}, V_{COM} < 0	–50		mA
I_{NO} I_{COM}	ON-state switch current	V_{NO}, V_{COM} = 0 to V_{CC}	–200	200	mA
	ON-state peak switch current[6]		–400	400	
V_I	Digital input voltage[3][4]		–0.5	6.5	V
I_{IK}	Digital input clamp current	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100	100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration <10% duty cycle

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage[1]	1.65	5.5	V
V_{NO} V_{COM}	Analog signal voltage	0	V_{CC}	V
V_{IN}	Control input voltage	0	5.5	V
T_A	Ambient temperature	–40	85	°C

(1) V_{CC} needs to be supplied prior to the control input, see *1.8-V Compatible Control Input Threshold Independent of V_{CC}*.

6.4 Thermal Information

THERMAL METRIC[1]		TS5A21366		UNIT
		DCU (VSSOP)	RSE (UQFN)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	211.3	168	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	83.8	71.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90.1	80.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.2	9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Thermal Information (continued)

THERMAL METRIC[1]		TS5A21366 DCU (VSSOP) 8 PINS	TS5A21366 RSE (UQFN) 8 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	89.6	80.3	°C/W

6.5 Electrical Characteristics for 5-V Supply

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
r_{ON}	ON-state resistance	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	4.5 V		0.75	1	Ω
				Full				1.4	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	4.5 V		0.04	0.1	Ω
				Full				0.1	
$r_{on(flat)}$	ON-state resistance flatness	V_{NO} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	4.5 V		0.15	0.25	Ω
				Full				0.25	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 4.5 V, or V_{NO} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 16	25°C	5.5 V	–10	1.4	10	nA
						–235		235	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,		Full	0 V	–5	0.06	5	µA
						–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{COM} = 1 V, V_{NO} = 4.5 V, or V_{COM} = 4.5 V, V_{NO} = 1 V,	Switch OFF, See Figure 16	25°C	5.5 V	–10	1.4	10	nA
				Full		–235		235	
$I_{COM(PWROFF)}$		V_{NO} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,		25°C	0 V	–5	0.06	5	µA
				Full		–10		10	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	5.5 V	–5	1.33	5	nA
				Full		–50		50	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 4.5 V, V_{NO} = Open,	Switch ON, See Figure 17	25°C	5.5 V	–5	1.33	5	nA
				Full		–50		50	
DIGITAL CONTROL INPUTS (IN1, IN2)[2]									
V_{IH}	Input logic high			Full	5.5 V	1.05		5.5	V
V_{IL}	Input logic low			Full	5.5 V	0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 1.95 V or GND		Full	5.5 V	–0.6		0.6	µA
r_{IN}	Input resistance	V_I = 1.95 V		Full	5.5 V		6		MΩ
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L= 35 pF, See Figure 19	25°C	5 V	39	49	72	ns
				Full	4.5 V to 5.5 V	28		97	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

Electrical Characteristics for 5-V Supply (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	5 V	168	243	318	ns
				Full	4.5 V 5.5 V	178		323	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	5 V		1.3		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 18	25°C	5 V		19		pF
$C_{COM(OFF)}$	COM OFF capacitance	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 18	25°C	5 V		17		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_{CC} or GND, Switch ON,	See Figure 18	25°C	5 V		33		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 18	25°C	5 V		33		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND,	See Figure 18	25°C	5 V		2.5		pF
PSRR	Power supply rejection ratio	f = 10 kHz, V_{COM} = 1 Vrms, R_L = 50 Ω,	C_L = 15 pF, See Figure 25	25°C	5 V		–84		dB
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	5 V		260		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	5 V		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	5 V		–98		dB
THD+N	Total harmonic distortion	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	5 V		0.002%		
SUPPLY									
I_{CC}	Positive supply current	V_I = 1.95 V or GND	Switch ON or OFF	25°C	5.5 V		7.6	9	µA
				Full				10	

6.6 Electrical Characteristics for 3.3-V Supply

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
r_{on}	ON-state resistance	V_{NO} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	3 V		1.1	1.5	Ω
				Full				1.8	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 2 V, 0.8 V I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	3 V		0.045	0.1	Ω
				Full				0.1	
$r_{on(flat)}$	ON-state resistance flatness	V_{NO} = 2 V, 0.8 V, I_{COM} = –100 mA,	Switch ON, See Figure 15	25°C	3 V		0.15	0.25	Ω
				Full				0.25	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 1 V, V_{COM} = 3 V, 1 V, or V_{NO} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 16	25°C	3.6 V	–5	0.9	5	nA
						–160		160	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		Full	0 V	–5	0.03	5	µA
						–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{NO} = 3 V, V_{COM} = 1 V, or V_{NO} = 1 V, V_{COM} = 3 V,	Switch OFF, See Figure 16	25°C	3.6 V	–5	0.9	5	nA
				Full		–160		160	
$I_{COM(PWROFF)}$		V_{NO} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–5	0.03	5	µA
				Full		–10		10	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 1 V, V_{COM} = Open, or V_{NO} = 3 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	3.6 V	–2	1	2	nA
				Full		–20		20	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 1 V, V_{NO} = Open, or V_{COM} = 3 V, V_{NO} = Open,	See Figure 17	25°C	3.6 V	–2	1	2	nA
				Full		–20		20	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
V_{IH}	Input logic high			Full	3.6 V	1.05		5.5	V
V_{IL}	Input logic low			Full	3.6 V	0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 1.95 V or GND		Full	3.6 V	–0.6		0.6	µA
r_{IN}	Input resistance	V_I = 1.95 V		Full	3.6 V		6		MΩ
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L= 35 pF, See Figure 19	25°C	3.3 V	66	83	133	ns
				Full	3 V to 3.6 V	43		178	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	3.3 V	138	247	306	ns
				Full	3 V to 3.6 V	204		329	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	3.3 V		1.3		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 18	25°C	3.3 V		19		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

Electrical Characteristics for 3.3-V Supply (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)[(1)]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$C_{COM(OFF)}$	COM OFF capacitance	V_{COM} = V_{CC} or GND, Switch OFF,	See Figure 18	25°C	3.3 V		17		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_{CC} or GND, Switch ON,	See Figure 18	25°C	3.3 V		30		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 18	25°C	3.3 V		30		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND,	See Figure 18	25°C	3.3 V		2.5		pF
PSRR	Power supply rejection ratio	f = 10 kHz, V_{COM} = 1 Vrms, R_L = 50 Ω,	C_L = 15 pF, See Figure 25	25°C	3.3 V		–84		dB
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	3.3 V		260		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	3.3 V		–62		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	3.3 V		–99		dB
THD+N	Total harmonic distortion	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	3.3 V		0.004%		
SUPPLY									
I_{CC}	Positive supply current	V_I = 1.95 V or GND	Switch ON or OFF	25°C	3.6 V		6.8	9	µA
				Full				10	

6.7 Electrical Characteristics for 2.5-V Supply

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
r_{on}	ON-state resistance	V_{NO} = 1.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 15	25°C	2.3 V		1.2	2.1	Ω
				Full				2.7	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 15	25°C	2.3 V		0.045	0.15	Ω
				Full				0.15	
$r_{on(flat)}$	ON-state resistance flatness	V_{NO} = 1.8 V, 0.8 V, I_{COM} = –8 mA,	Switch ON, See Figure 15	25°C	2.3 V		0.4	0.6	Ω
				Full				0.6	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 0.5 V, V_{COM} = 2.3 V, or V_{NO} = 2.3 V, V_{COM} = 0.5 V,	Switch OFF, See Figure 16	25°C	2.7 V	–8	0.7	8	nA
						–136		136	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,		Full	0 V	–5	0.02	5	µA
						–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{NO} = 2.3 V, V_{COM} = 0.5 V, or V_{NO} = 0.5 V, V_{COM} = 2.3 V,	Switch OFF, See Figure 16	25°C	2.7 V	–8	0.7	8	nA
				Full		–136		136	
$I_{COM(PWROFF)}$		V_{NO} = 0 to 2.7 V, V_{COM} = 2.7 V to 0,		25°C	0 V	–5	0.02	5	µA
				Full		–10		10	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 0.5 V, V_{COM} = Open, or V_{NO} = 2.3 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	2.7 V	–2	0.3	2	nA
				Full		–15		15	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.5 V, V_{NO} = Open, or V_{COM} = 2.3 V, V_{NO} = Open,	Switch ON, See Figure 17	25°C	2.7 V	–2	0.3	2	nA
				Full		–15		15	
DIGITAL CONTROL INPUTS (IN1, IN2)(2)									
V_{IH}	Input logic high			Full	2.7 V	1.05		5.5	V
V_{IL}	Input logic low			Full	2.7 V	0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 1.95 V or GND		Full	2.7 V	–0.6		0.6	µA
r_{IN}	Input resistance	V_I = 1.95 V		Full	2.7 V		6		MΩ
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L= 35 pF, See Figure 19	25°C	2.5 V	101	137	222	ns
				Full	2.3 V to 2.7 V	68		288	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	2.5 V	148	264	333	ns
				Full	2.3 V to 2.7 V	197		367	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	2.5 V		1.3		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 18	25°C	2.5 V		19		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

Electrical Characteristics for 2.5-V Supply (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$C_{COM(OFF)}$	COM OFF capacitance	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 18	25°C	2.5 V		17		pF
$C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_{CC} or GND, Switch ON,	See Figure 18	25°C	2.5 V		27.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 18	25°C	2.5 V		27.5		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND,	See Figure 18	25°C	2.5 V		2.5		pF
PSRR	Power supply rejection ratio	f = 10 kHz, V_{COM} = 1 Vrms, R_L = 50 Ω,	C_L = 15 pF, See Figure 25	25°C	2.5 V		–84		dB
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	2.5 V		260		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	2.5 V		–61		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	2.5 V		–99		dB
THD+N	Total harmonic distortion	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	2.5 V		0.011%		
SUPPLY									
I_{CC}	Positive supply current	V_I = 1.95 V or GND	Switch ON or OFF	25°C	2.7 V		6.6	9	μA
				Full				10	

6.8 Electrical Characteristics for 1.8-V Supply

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
ANALOG SWITCH									
r_{on}	ON-state resistance	V_{NO} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 15	25°C	1.65 V		1.6	4	Ω
				Full				5	
Δr_{on}	ON-state resistance match between channels	V_{NO} = 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 15	25°C	1.65 V		0.045	0.2	Ω
				Full				0.2	
$r_{on(flat)}$	ON-state resistance flatness	V_{NO} = 0.6 V, 1.5 V, I_{COM} = –2 mA,	Switch ON, See Figure 15	25°C	1.65 V		1.7	2.8	Ω
				Full				3	
$I_{NO(OFF)}$	NO OFF leakage current	V_{NO} = 0.3 V, V_{COM} = 1.65 V, or V_{NO} = 1.65 V, V_{COM} = 0.3 V,	Switch OFF, See Figure 16	25°C	1.95 V	–10	0.5	10	nA
						–30		30	
$I_{NO(PWROFF)}$		V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,		Full	0 V	–5	0.02	5	µA
						–10		10	
$I_{COM(OFF)}$	COM OFF leakage current	V_{NO} = 1.65 V, V_{COM} = 0.3 V, or V_{NO} = 0.3 V, V_{COM} = 1.65 V,	Switch OFF, See Figure 16	25°C	1.95 V	–10	0.5	10	nA
				Full		–30		30	
$I_{COM(PWROFF)}$		V_{NO} = 0 to 1.95 V, V_{COM} = 1.95 V to 0,		25°C	0 V	–5	0.02	5	µA
				Full		–10		10	
$I_{NO(ON)}$	NO ON leakage current	V_{NO} = 0.3 V, V_{COM} = Open, or V_{NO} = 1.65 V, V_{COM} = Open,	Switch ON, See Figure 17	25°C	1.95 V	–2	0.2	2	nA
				Full		–15		15	
$I_{COM(ON)}$	COM ON leakage current	V_{COM} = 0.3 V, V_{NO} = Open, or V_{COM} = 1.65 V, V_{NO} = Open,	Switch ON, See Figure 17	25°C	1.95 V	–2	0.2	2	nA
				Full		–15		15	
DIGITAL CONTROL INPUTS (IN1, IN2)[2]									
V_{IH}	Input logic high			Full	1.95 V	1.05		5.5	V
V_{IL}	Input logic low			Full	1.95 V	0		0.6	V
I_{IH}, I_{IL}	Input leakage current	V_I = 1.95 V or GND		Full	1.95 V	–0.6		0.6	µA
r_{IN}	Input resistance	V_I = 1.95 V		Full	1.95 V		6		MΩ
DYNAMIC									
t_{ON}	Turnon time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L= 35 pF, See Figure 19	25°C	1.8 V	198	297	448	ns
				Full	1.65 V to 1.95 V	136		620	
t_{OFF}	Turnoff time	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 19	25°C	1.8 V	225	308	430	ns
				Full	1.65 V to 1.95 V	204		514	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 23	25°C	1.8 V		1.4		pC
$C_{NO(OFF)}$	NO OFF capacitance	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 18	25°C	1.8 V		19		pF

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, (SCBA004).

Electrical Characteristics for 1.8-V Supply (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
$C_{COM(OFF)}$	COM OFF capacitance	V_{NO} = V_{CC} or GND, Switch OFF,	See Figure 18	25°C	1.8 V		17		pF
$C_{NC(ON)}$, $C_{NO(ON)}$	NO ON capacitance	V_{NO} = V_{CC} or GND, Switch ON,	See Figure 18	25°C	1.8 V		27.5		pF
$C_{COM(ON)}$	COM ON capacitance	V_{COM} = V_{CC} or GND, Switch ON,	See Figure 18	25°C	1.8 V		27.5		pF
C_I	Digital input capacitance	V_I = V_{CC} or GND,	See Figure 18	25°C	1.8 V		2.5		pF
PSRR	Power supply rejection ratio	f = 10 kHz, V_{COM} = 1 Vrms, R_L = 50 Ω,	C_L = 15 pF, See Figure 25	25°C	1.8 V		–78		dB
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See Figure 20	25°C	1.8 V		260		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 21	25°C	1.8 V		–59		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	Switch ON, See Figure 22	25°C	1.8 V		–101		dB
THD+N	Total harmonic distortion	R_L = 600 Ω, C_L = 15 pF,	f = 20 Hz to 20 kHz, See Figure 24	25°C	1.8 V		0.001%		
SUPPLY									
I_{CC}	Positive supply current	V_I = 1.95 V or GND	Switch ON or OFF	25°C	1.95 V		3.6	9	µA
				Full				10	

6.9 Typical Characteristics

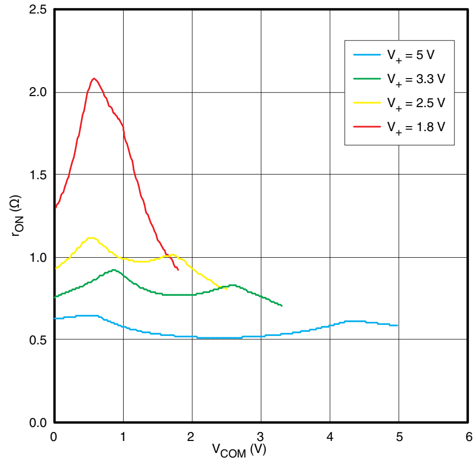
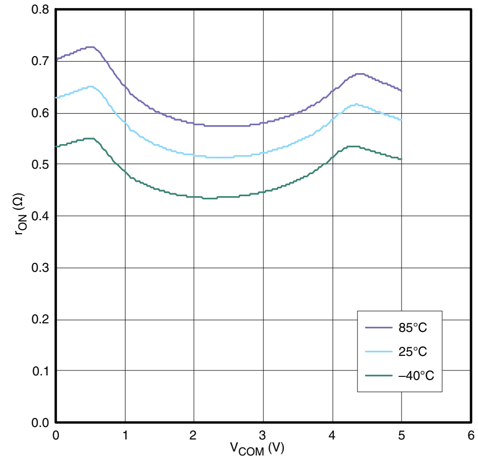
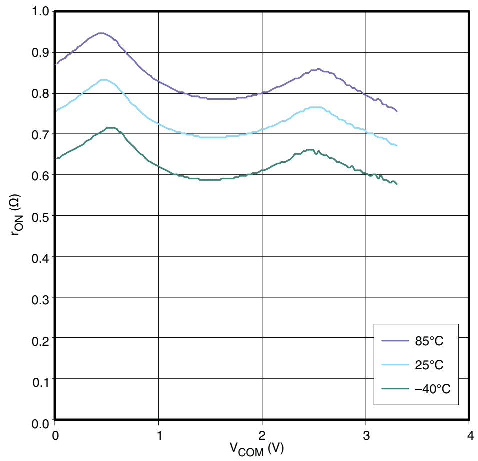


Figure 1. r_{ON} vs V_{COM}



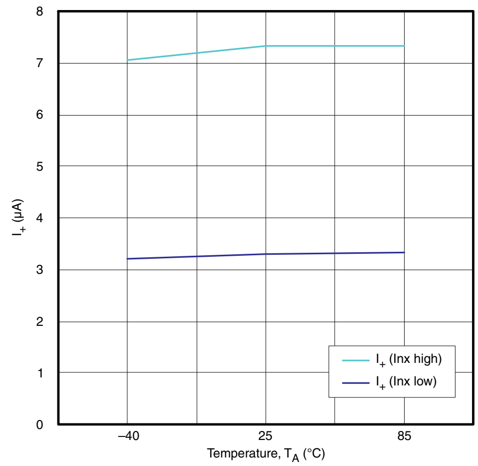
V_{CC} = 5 V

Figure 2. r_{ON} vs V_{COM}



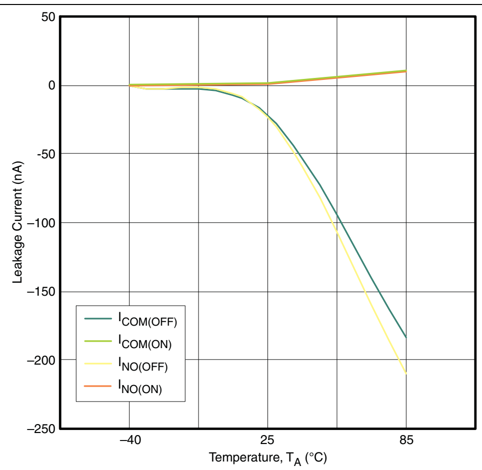
V_{CC} = 3.3 V

Figure 3. r_{ON} vs V_{COM}



V_{CC} = 5 V

Figure 4. Power Supply Current vs Temperature



V_{CC} = 5.5 V

Figure 5. Leakage Current vs Temperature

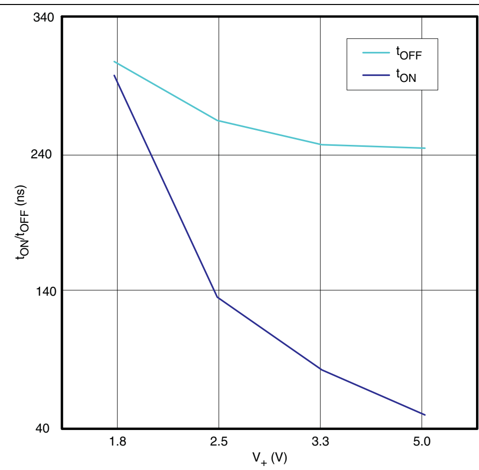
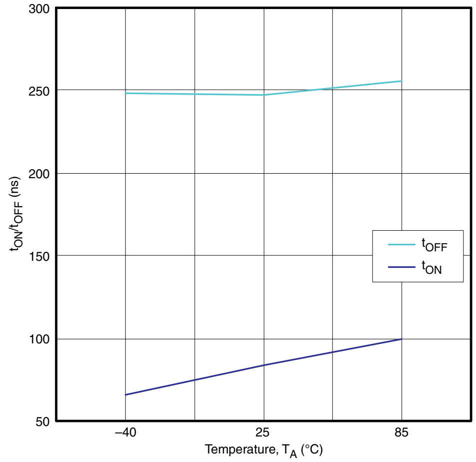


Figure 6. t_{ON}/t_{OFF} vs Supply Voltage

Typical Characteristics (continued)



V_{CC} = 3.3 V

Figure 7. t_{ON}/t_{OFF} vs Temperature

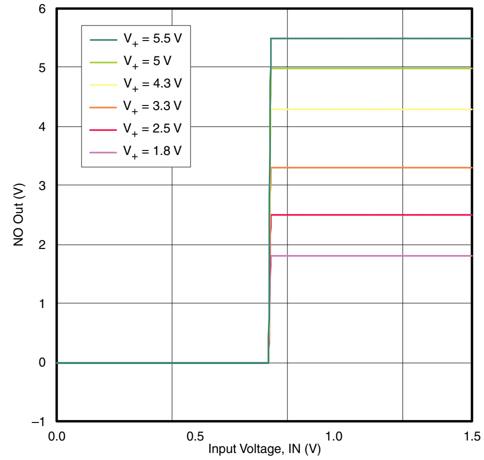


Figure 8. Input Voltage Thresholds

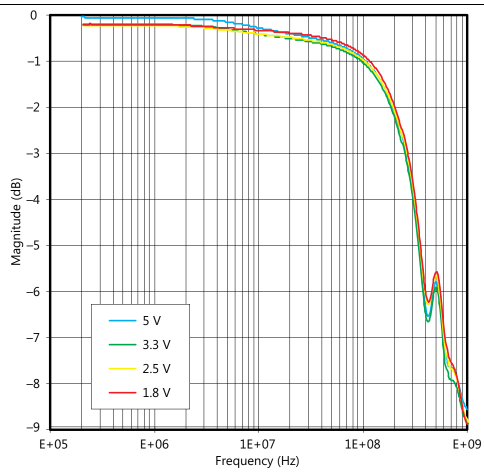


Figure 9. Insertion Loss

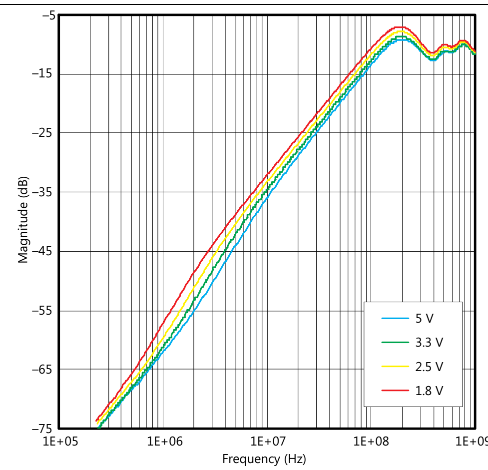


Figure 10. OFF Isolation

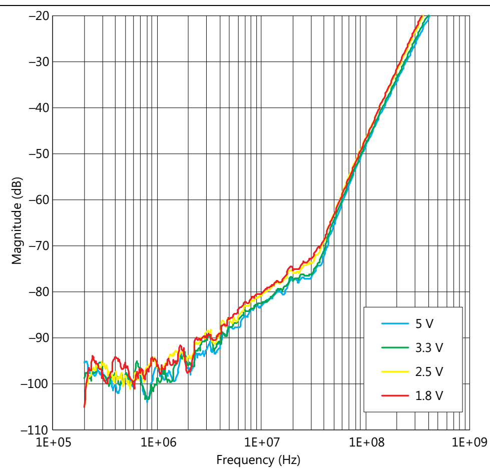


Figure 11. Crosstalk

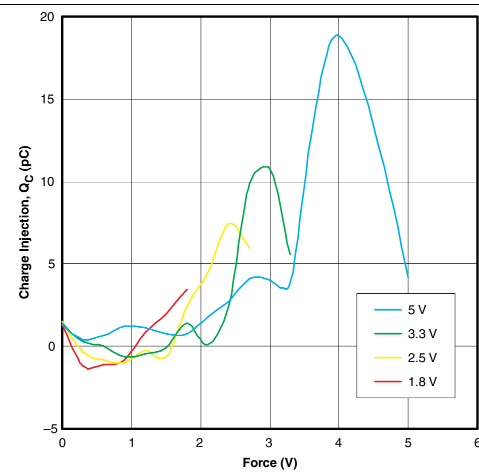


Figure 12. Charge Injection (Q_C) vs Bias Voltage

Typical Characteristics (continued)

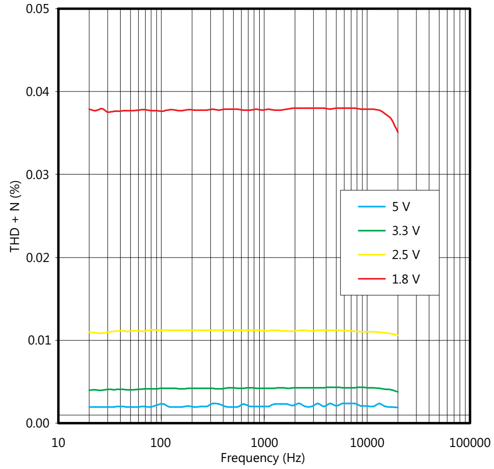


Figure 13. THD+N (%) vs Frequency

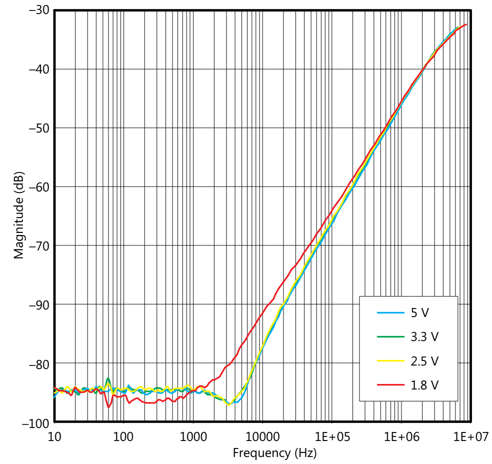


Figure 14. Power Supply Rejection Ratio (PSRR)

7 Parameter Measurement Information

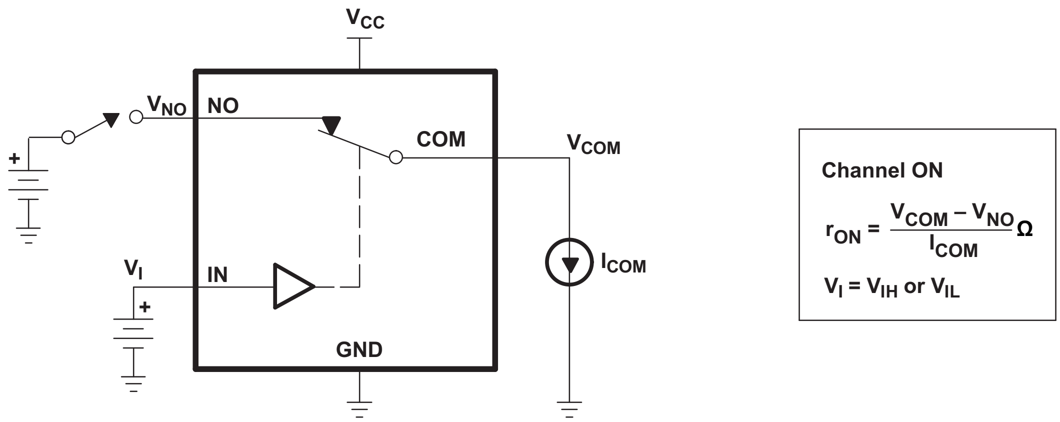


Figure 15. ON-State Resistance (r_{ON})

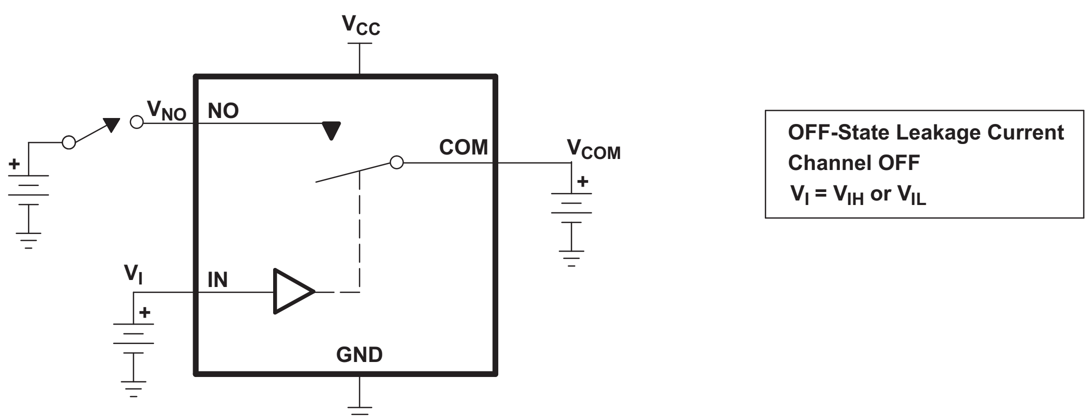


Figure 16. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NO(OFF)}$, $I_{COM(PWROFF)}$, $I_{NOC(PWR(FF)}$)

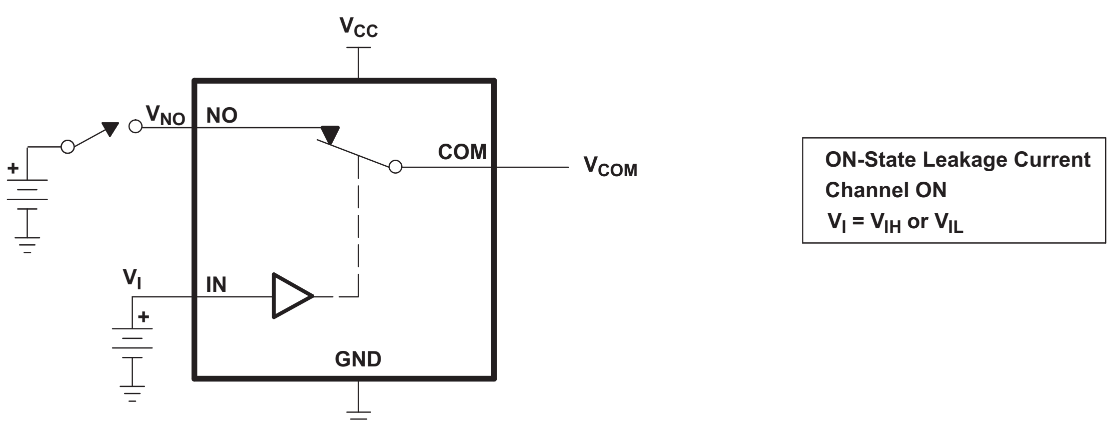


Figure 17. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NO(ON)}$)

Parameter Measurement Information (continued)

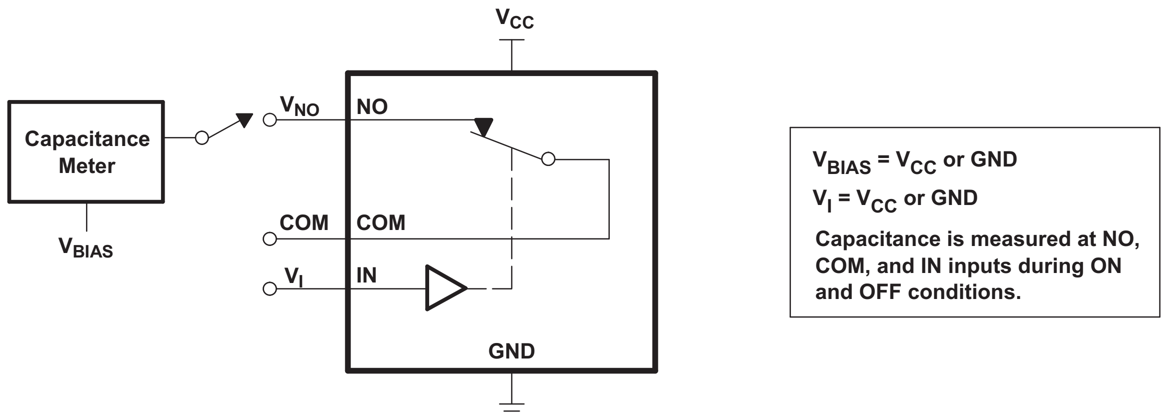
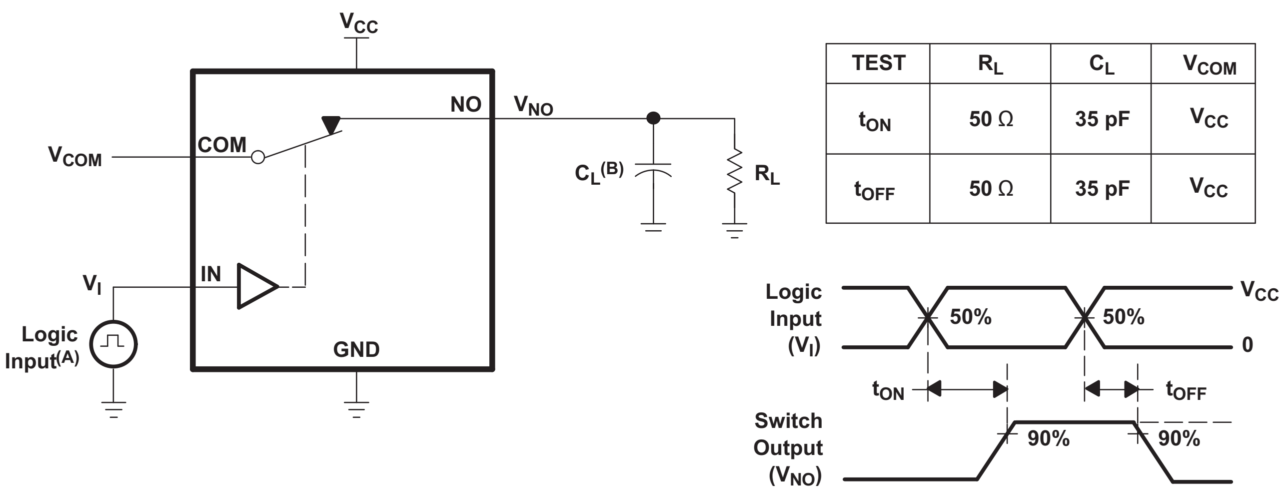


Figure 18. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NO(OFF)}$, $C_{NO(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{CC}
t_{OFF}	50 Ω	35 pF	V_{CC}

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 5 ns, t_f ≤ 5 ns.

B. C_L includes probe and jig capacitance.

Figure 19. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

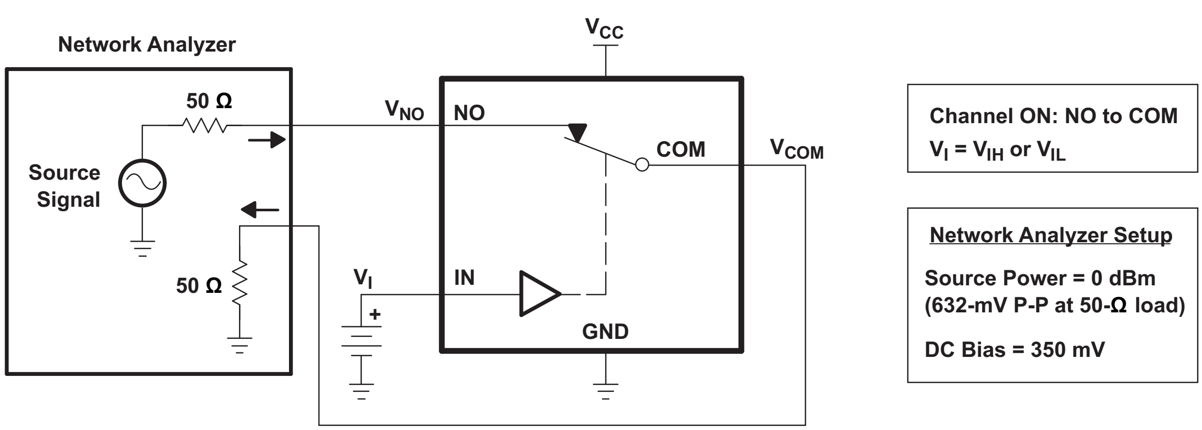


Figure 20. Bandwidth (BW)

Parameter Measurement Information (continued)

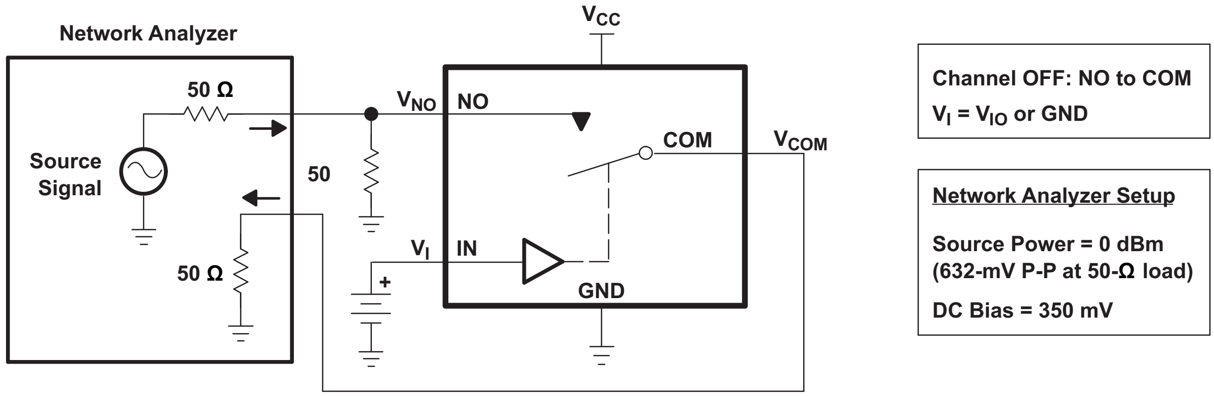


Figure 21. OFF Isolation (O_{ISO})

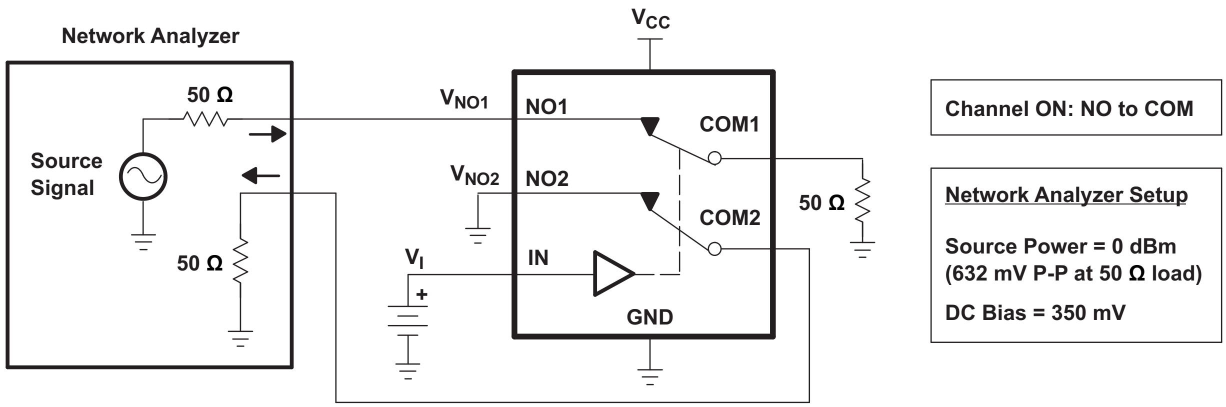
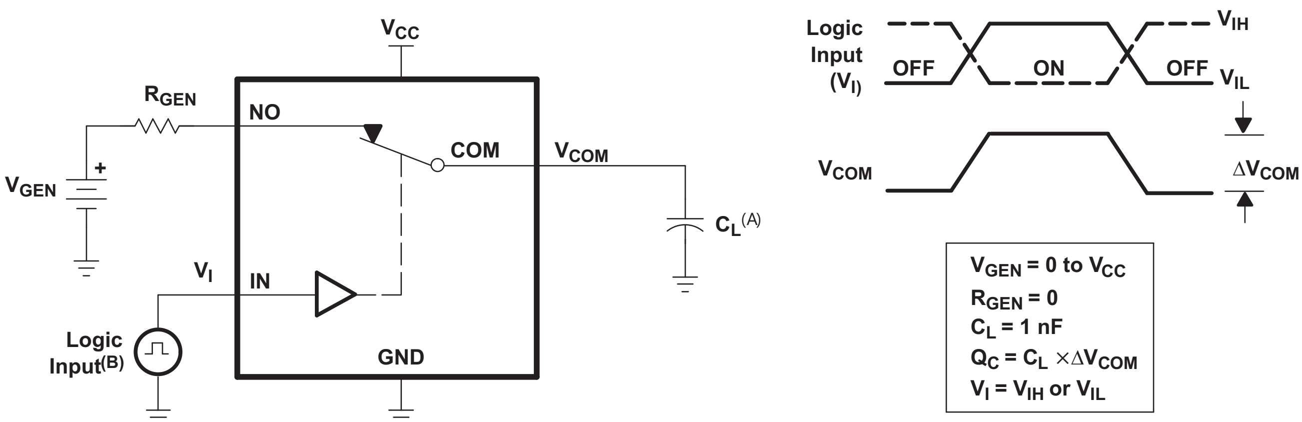


Figure 22. Crosstalk (X_{TALK})

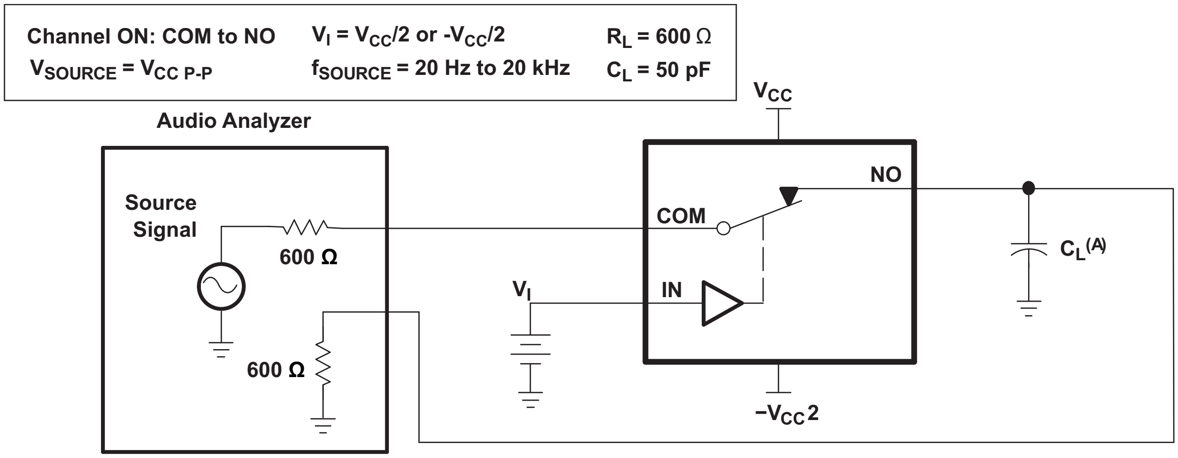


A. C_L includes probe and jig capacitance.

B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 5 ns, t_f ≤ 5 ns.

Figure 23. Charge Injection (Q_C)

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

Figure 24. Total Harmonic Distortion (THD+N)

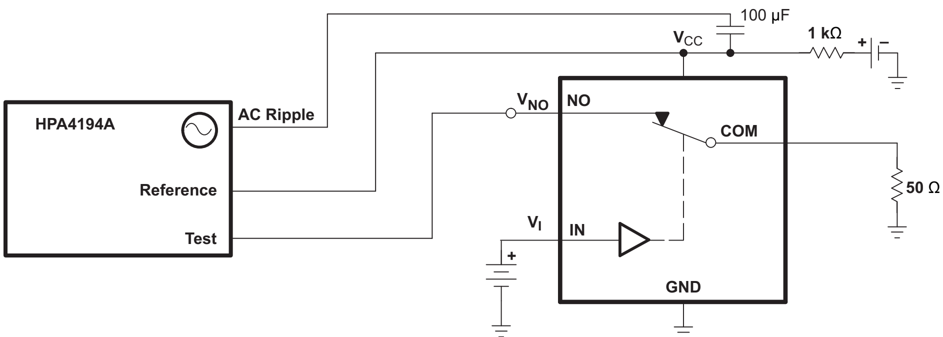


Figure 25. Power Supply Rejection Ratio (PSRR)

Parameter Measurement Information (continued)

Table 1. Parameter Description

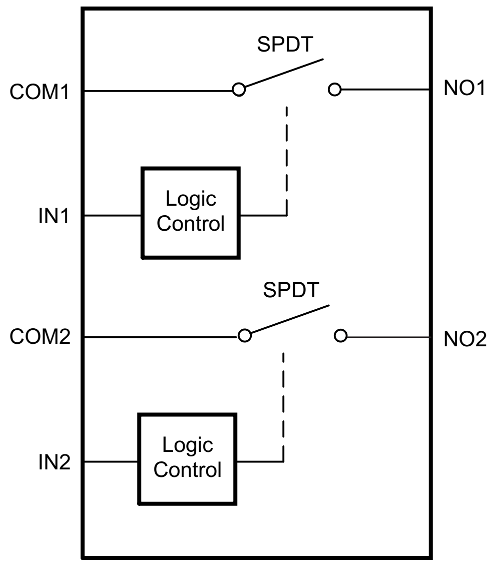
SYMBOL	DESCRIPTION
V_{COM}	Voltage at COM
V_{NO}	Voltage at NO
r_{on}	Resistance between COM and NO ports when the channel is ON
$r_{on(flat)}$	Difference between the maximum and minimum value of r_{on} in a channel over the specified range of conditions
$I_{NO(OFF)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the OFF state
$I_{NO(ON)}$	Leakage current measured at the NO port, with the corresponding channel (NO to COM) in the ON state and the output (COM) open
$I_{COM(OFF)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the OFF state
$I_{COM(ON)}$	Leakage current measured at the COM port, with the corresponding channel (COM to NO) in the ON state and the output (NO) open
V_{IH}	Minimum input voltage for logic high for the control input (IN)
V_{IL}	Maximum input voltage for logic low for the control input (IN)
V_I	Voltage at the control input (IN)
I_{IH}, I_{IL}	Leakage current measured at the control input (IN)
t_{ON}	Turnon time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning ON.
t_{OFF}	Turnoff time for the switch. This parameter is measured under the specified range of conditions and by the propagation delay between the digital control (IN) signal and analog output (COM or NO) signal when the switch is turning OFF.
Q_C	Charge injection is a measurement of unwanted signal coupling from the control (IN) input to the analog (NO or COM) output. This is measured in coulomb (C) and measured by the total charge induced due to switching of the control input. Charge injection, $Q_C = C_L \times \Delta V_{COM}$, C_L is the load capacitance and ΔV_{COM} is the change in analog output voltage.
$C_{NO(OFF)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is OFF
$C_{NO(ON)}$	Capacitance at the NO port when the corresponding channel (NO to COM) is ON
$C_{COM(OFF)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is OFF
$C_{COM(ON)}$	Capacitance at the COM port when the corresponding channel (COM to NO) is ON
C_I	Capacitance of control input (IN)
O_{ISO}	OFF isolation of the switch is a measurement of OFF-state switch impedance. This is measured in dB in a specific frequency, with the corresponding channel (NO to COM) in the OFF state.
X_{TALK}	Crosstalk is a measurement of unwanted signal coupling from an ON channel to an OFF channel (NO1 to NO2). This is measured in a specific frequency and in dB.
BW	Bandwidth of the switch. This is the frequency in which the gain of an ON channel is –3 dB below the DC gain.
THD+N	Total harmonic distortion describes the signal distortion caused by the analog switch. This is defined as the ratio of root mean square (RMS) value of the second, third, and higher harmonic to the absolute magnitude of the fundamental harmonic.
I_{CC}	Static power-supply current with the control (IN) pin at V_{CC} or GND
ΔI_{CC}	This is the increase in I_{CC} for each control (IN) input that is at the specified voltage, rather than at V_{CC} or GND.

8 Detailed Description

8.1 Overview

The TS5A21366 is a bidirectional, 2-channel, single-pole single-throw (SPST) analog switch that is designed to operate from 1.65-V to 5.5-V supply voltages. This device has 1.8-V compatible input control logic thresholds that are independent of the supply voltage.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 1.8-V Compatible Control Input Threshold Independent of V_{CC}

TS5A21366 integrates special control inputs with low threshold allowing the device to be controlled by 1.8-V signals. The thresholds are fixed and independent of the supply value (V_{CC}). The low threshold (V_{IH}, V_{IL}) of the control inputs (IN1, IN2) is achieved by use of an internal bias circuit. To avoid an increased quiescent current (I_{CC}) condition, proper power sequencing must be followed to ensure that the bias circuitry is powered up prior to applying voltage on the I/Os. The proper sequence is for the V_{CC} pin to be brought up to V_{CC} before the control inputs (IN1, IN2) are allowed to go to a high level.

8.3.2 Isolation in Power-Down Mode, V_{CC} = 0

The TS5A21366 signal paths are high impedance (Hi-Z) when V_{CC} = 0. This feature ensures the signal path is isolated when not in use to avoid interfering with other signals in the system.

8.4 Device Functional Modes

The TS5A21366 device has two functional modes. In one mode, the NO pin is connected to COM pin and a signal passes through the switch. The other mode the NO and COM pins placed in a high impedance state (Hi-Z) and a signal does not pass through the switch.

Table 2. Function Table

IN	NO TO COM, COM TO NO
L	OFF
H	ON

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

2-channel SPST analog switches are used to provide bus isolation in the system by turning on and off a signal path. The TS5A21366 is selected for applications needing to isolate analog signals where signal integrity is most important because of the switches' low on-state resistance and low on-state leakage performance. An example of this type of application is an analog signal from a sensor into an ADC.

9.2 Typical Application

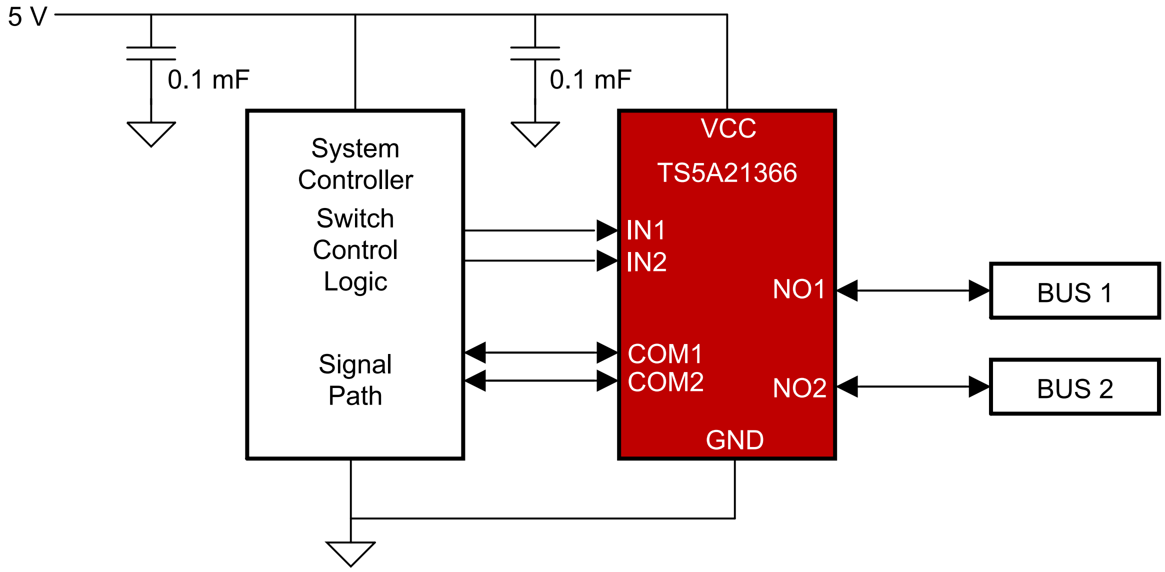


Figure 26. Typical Application Schematic

9.2.1 Design Requirements

- The TS5A23166 can be properly operated without any external components.
- Unused pins COM or NO may be left floating.
- Digital control pins IN must be pulled up to V_{CC} or down to GND to avoid undesired switch positions that could result from the floating pin.

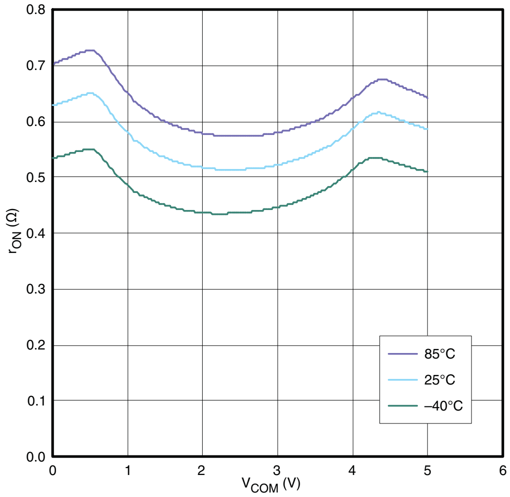
9.2.2 Detailed Design Procedure

Ensure that all of the signals passing through the switch are within the specified ranges in the *Recommended Operating Conditions* to ensure proper performance.

To avoid an increased quiescent current (I_{CC}) condition, proper power sequencing must be followed to ensure that the bias circuitry is powered up prior to applying voltage on the I/Os. The proper sequence is for the V_{CC} pin to be brought up to V_{CC} before the control inputs (IN1, IN2) are allowed to go to a high level.

Typical Application (continued)

9.2.3 Application Curve



V_{CC} = 5 V

Figure 27. r_{ON} vs V_{COM}

10 Power Supply Recommendations

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the VCC supply to other components. A 0.1-µF capacitor, connected from VCC to GND, is adequate for most applications

To avoid an increased quiescent current (I_{CC}) condition, proper power sequencing must be followed to ensure that the bias circuitry is powered up prior to applying voltage on the I/Os. The proper sequence is for the V_{CC} pin to be brought up to V_{CC} before the control inputs (IN1, IN2) are allowed to go to a high level.

11 Layout

11.1 Layout Guidelines

High-speed switches require proper layout and design procedures for optimum performance. Reduce stray inductance and capacitance by keeping traces short and wide. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

11.2 Layout Example

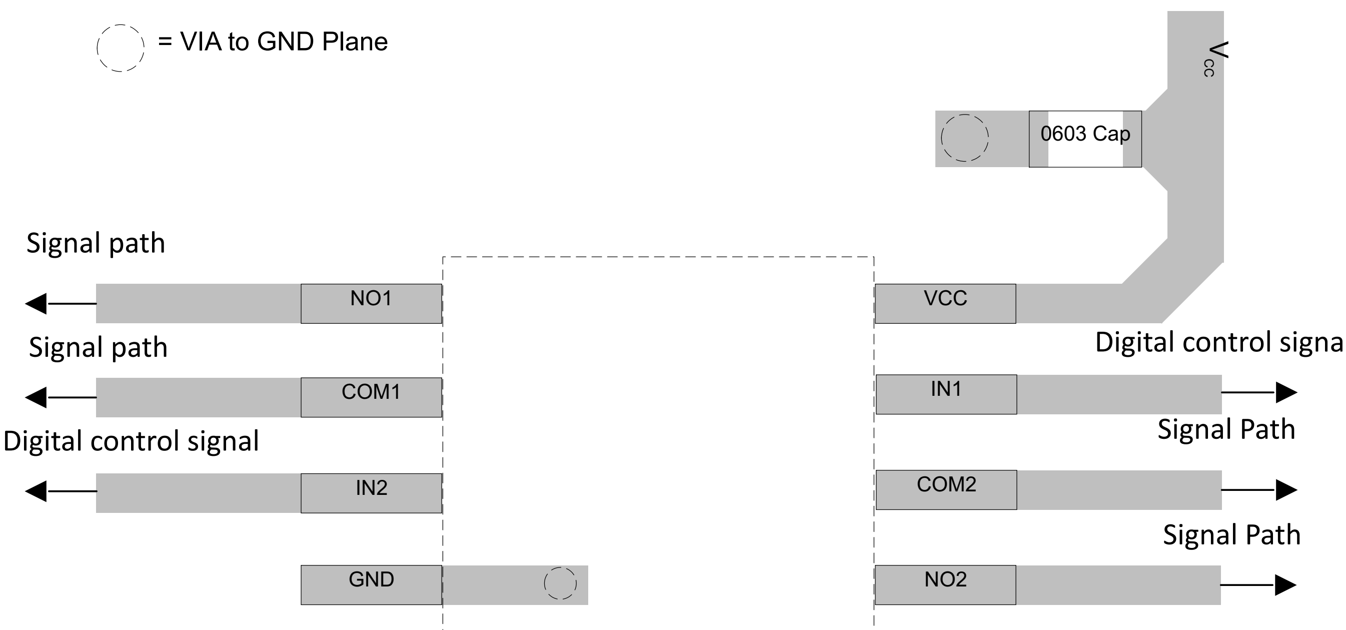


Figure 28. TS5A21366 Layout Example

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A21366DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(BS, JBSR) JZ	Samples
TS5A21366RSER	ACTIVE	UQFN	RSE	8	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	4F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

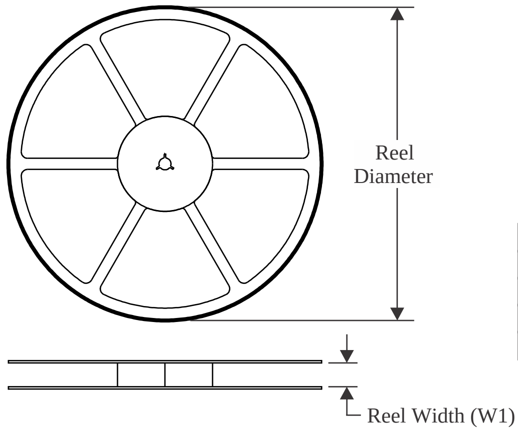
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

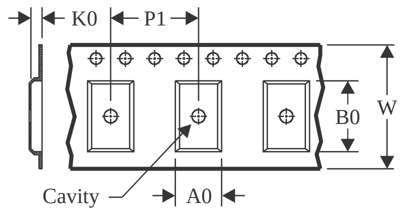
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

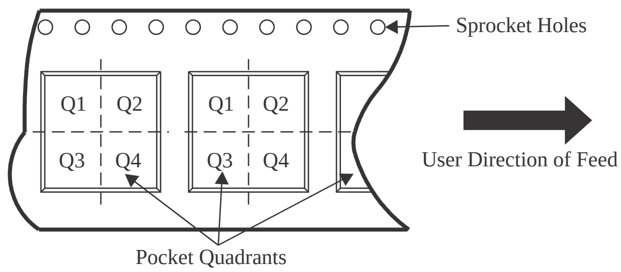


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

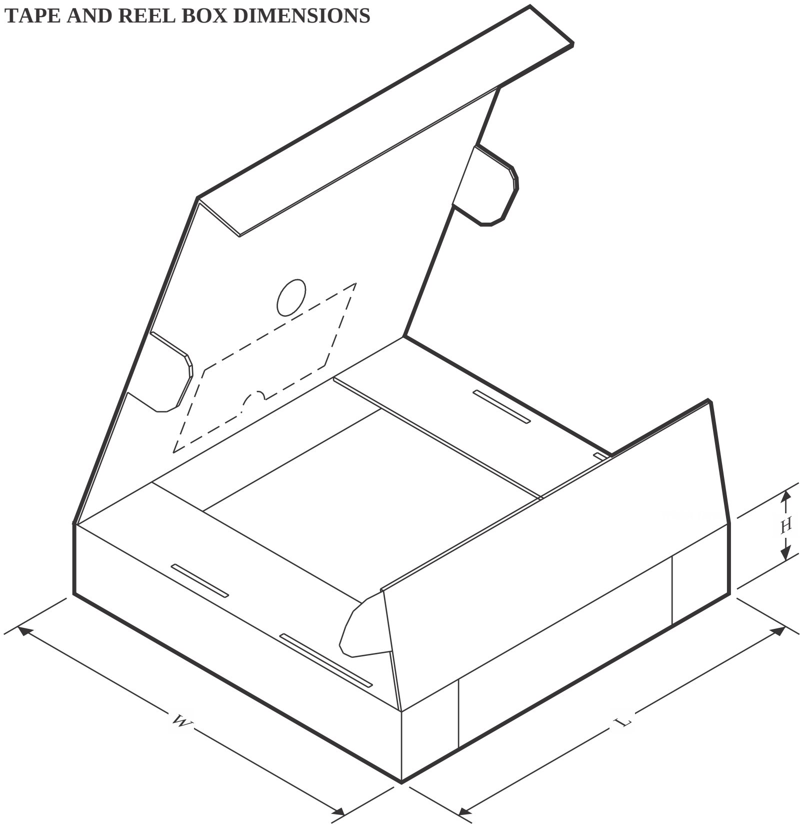
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

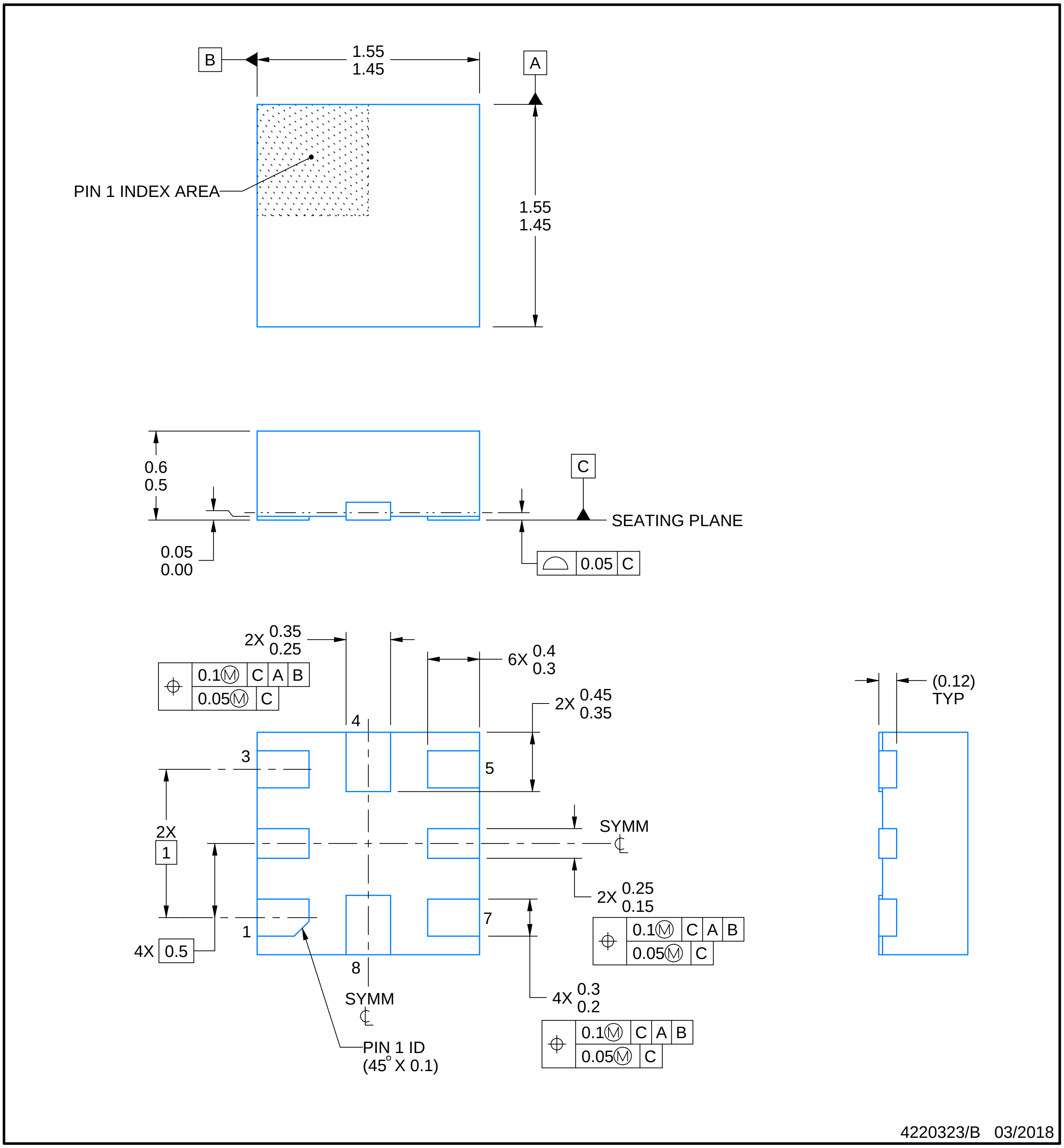
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A21366DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
TS5A21366RSER	UQFN	RSE	8	3000	180.0	8.4	1.7	1.7	0.7	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



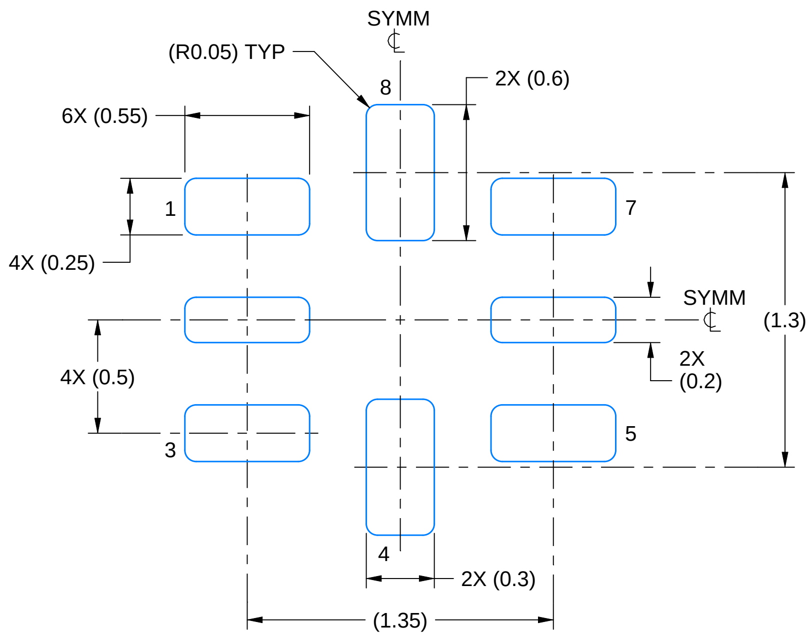
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A21366DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
TS5A21366RSER	UQFN	RSE	8	3000	202.0	201.0	28.0

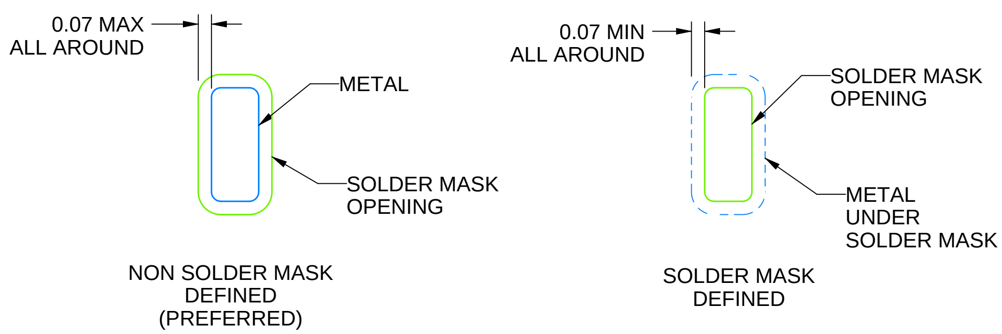


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

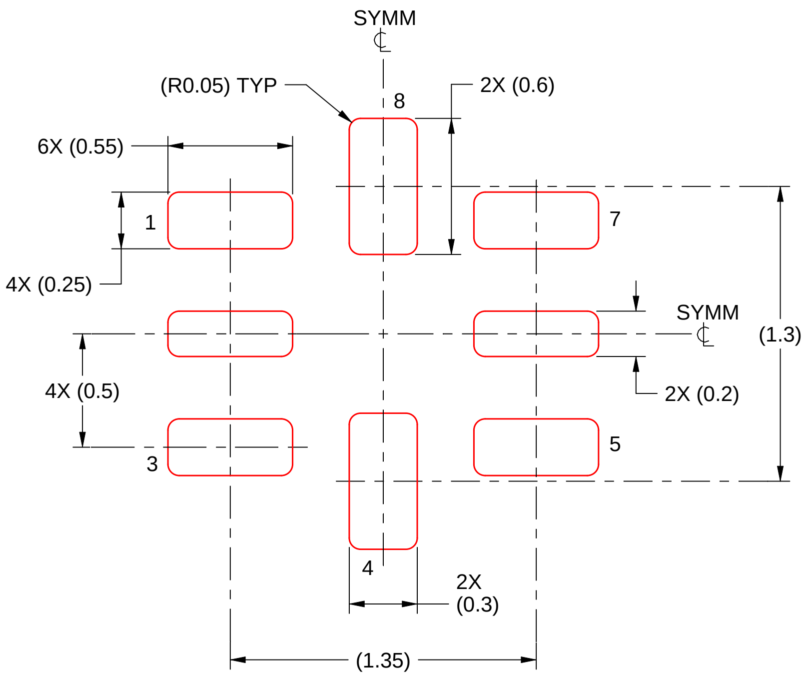


SOLDER MASK DETAILS
NOT TO SCALE

4220323/B 03/2018

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICKNESS
SCALE: 30X

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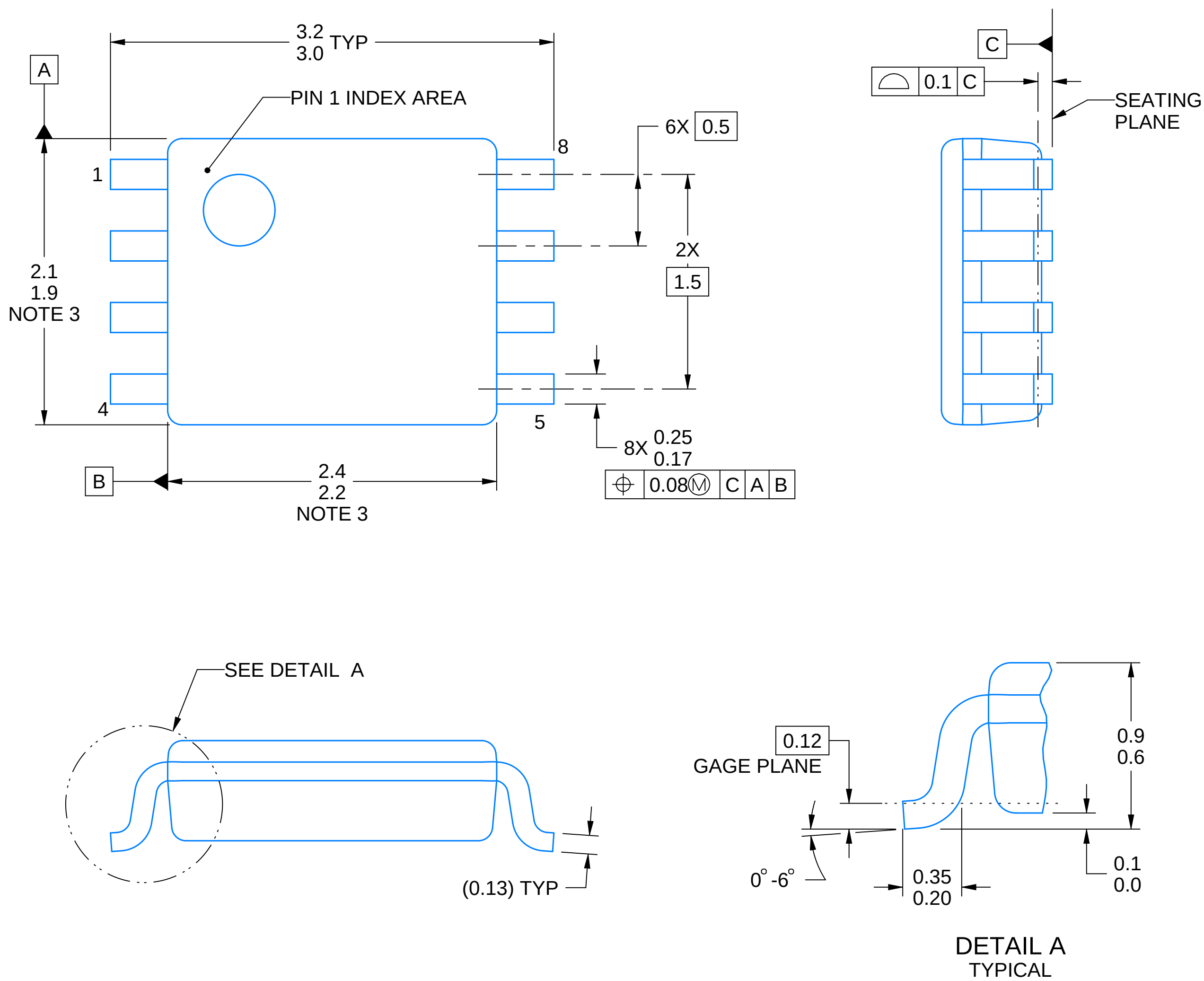
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



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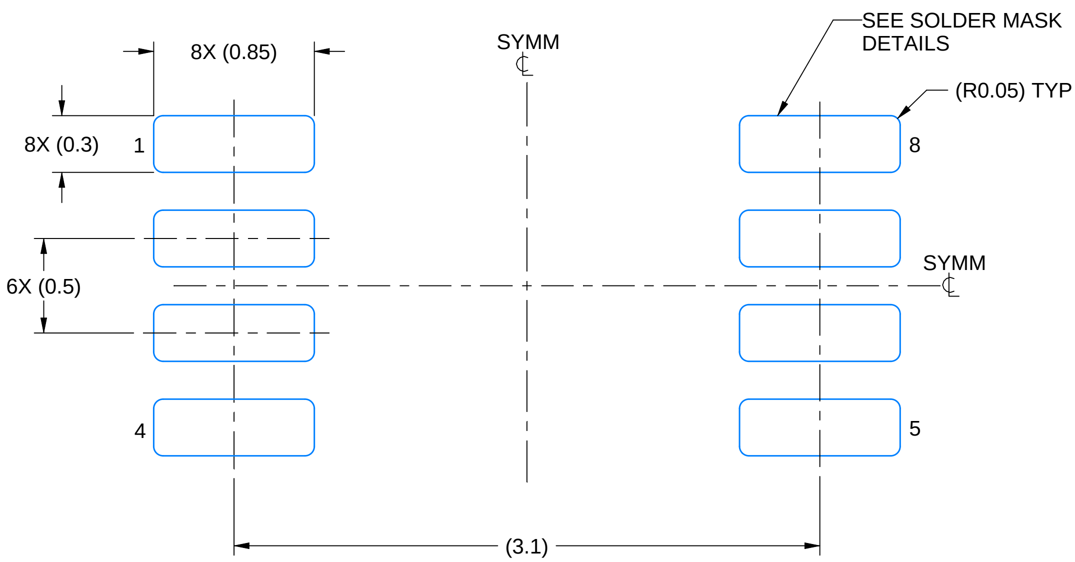
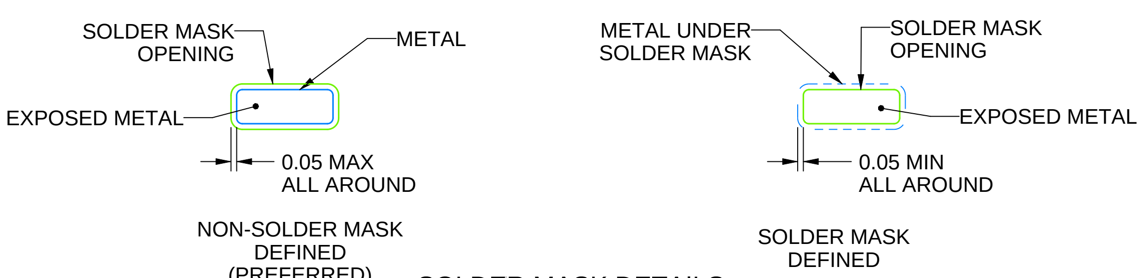
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



SOLDER MASK DETAILS

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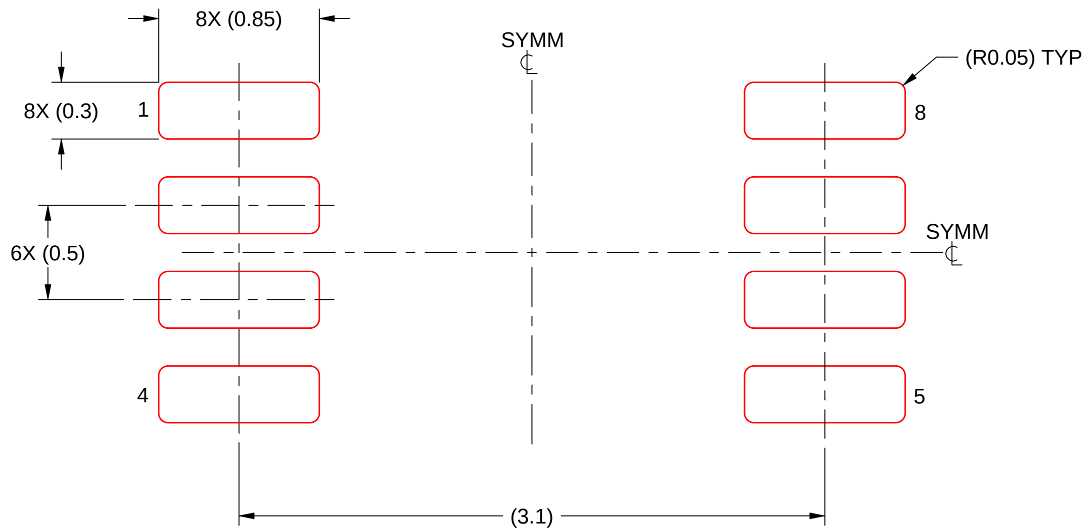
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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