USB 2.0 High-Speed (480 Mbps) and Audio Switches with Negative Signal Capability and 1.8-V Logic Compatibility

Check for Samples: TS5USBA224

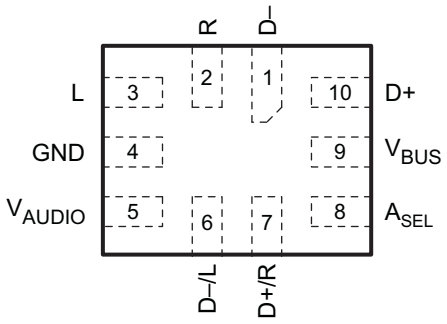
FEATURES

- **High-Speed USB Switch:**
  - **4 Ω R_{DSON} Typical**
  - **12.5 pF C_{ON} Typical**
  - **650-MHz Bandwidth (–3 dB)**
- **Audio Switch:**
  - **3 Ω R_{DSON} Typical**
  - **Negative Rail Capability**
  - **Low THD: <0.05%**
  - **Internal Shunt Resistors for Click-and-Pop Reduction**
  - **Powered From V_{AUDIO} (2.7V to 5.5V)**
- **1.8-V Compatible Control Input (A_{SEL} and V_{BUS}) Threshold**
- **I_{OFF} Supports Partial Powerdown Mode**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
  - **200-V Machine Model (A115-A)**

APPLICATIONS

- **Cellular Phones**
- **Personal Digital Assistants (PDAs)**
- **Portable Instrumentation**
- **Digital Still Cameras**
- **Portable Navigation Devices**

RSW PACKAGE
(TOP VIEW)



DESCRIPTION

The TS5USBA224 is a double-pole, double throw (DPDT) multiplexer that includes a low-distortion audio switch and a USB 2.0 High-Speed (480Mbps) switch in the same package. This configuration allows the system designer to use a common connector for audio and USB data. The audio switch is designed to allow audio signals to swing below ground which makes this common connector configuration possible.

The TS5USBA224 is powered up using V_{AUDIO}. When A_{SEL}=High, the audio path is selected regardless of the logic level at V_{BUS}. If A_{SEL}=Low and V_{BUS}=High, the USB path is selected. Otherwise if A_{SEL}=Low and V_{BUS}=Low, the audio path is selected.

The TS5USBA224 also features shunt resistors on the audio path to reduce clicks and pops that may be heard when the audio switches are selected.

ORDERING INFORMATION

T_A	PACKAGE(1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QFN 0.4-MM PITCH – RSW (Pb-Free)	Tape and reel	TS5USBA224RSWR	A5R

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SUMMARY OF TYPICAL CHARACTERISTICS

	USB PATH	AUDIO PATH
Number of switches	2	2
ON-state resistance (r_{on})	4 Ω	3 Ω
ON-state resistance match (Δr_{on})	< 0.3 Ω	< 0.3 Ω
ON-state resistance flatness ($r_{on(flat)}$)	N/A	1.5 Ω
Turn-on/turn-off time (t_{ON}/t_{OFF})	< 2 µs	< 4 µs
Bandwidth (BW)	650 MHz	N/A
OFF isolation (O_{ISO})	–22 dB	–83 dB
Crosstalk (X_{TALK})	–31 dB	–83 dB
Total harmonic distortion (THD)	N/A	0.05%

PIN DESCRIPTION TABLE

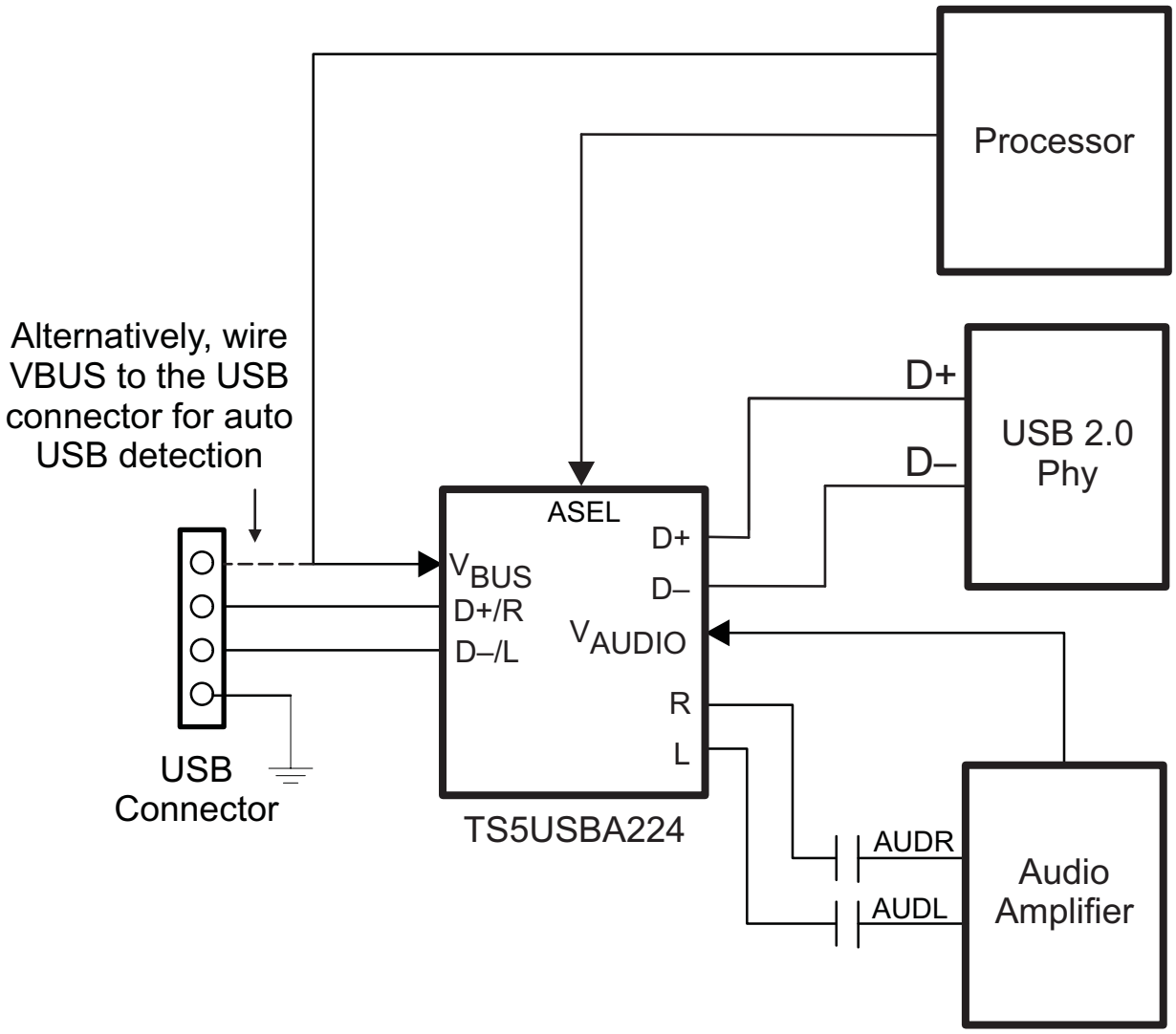
PIN			DESCRIPTION
NO.	NAME	TYPE	
1	D–	I/O	USB Data (Differential –)
2	R	I/O	Right Channel Audio
3	L	I/O	Left Channel Audio
4	GND	Ground	Ground
5	V_{AUDIO}	Power	Supply Voltage
6	D–/L	I/O	USB/Audio Common Connector
7	D+/R	I/O	USB/Audio Common Connector
8	A_{SEL}	Input	Control Input for Audio Path
9	V_{BUS}	Input	Control Input for USB Path
10	D+	I/O	USB Data (Differential +)

FUNCTION TABLE

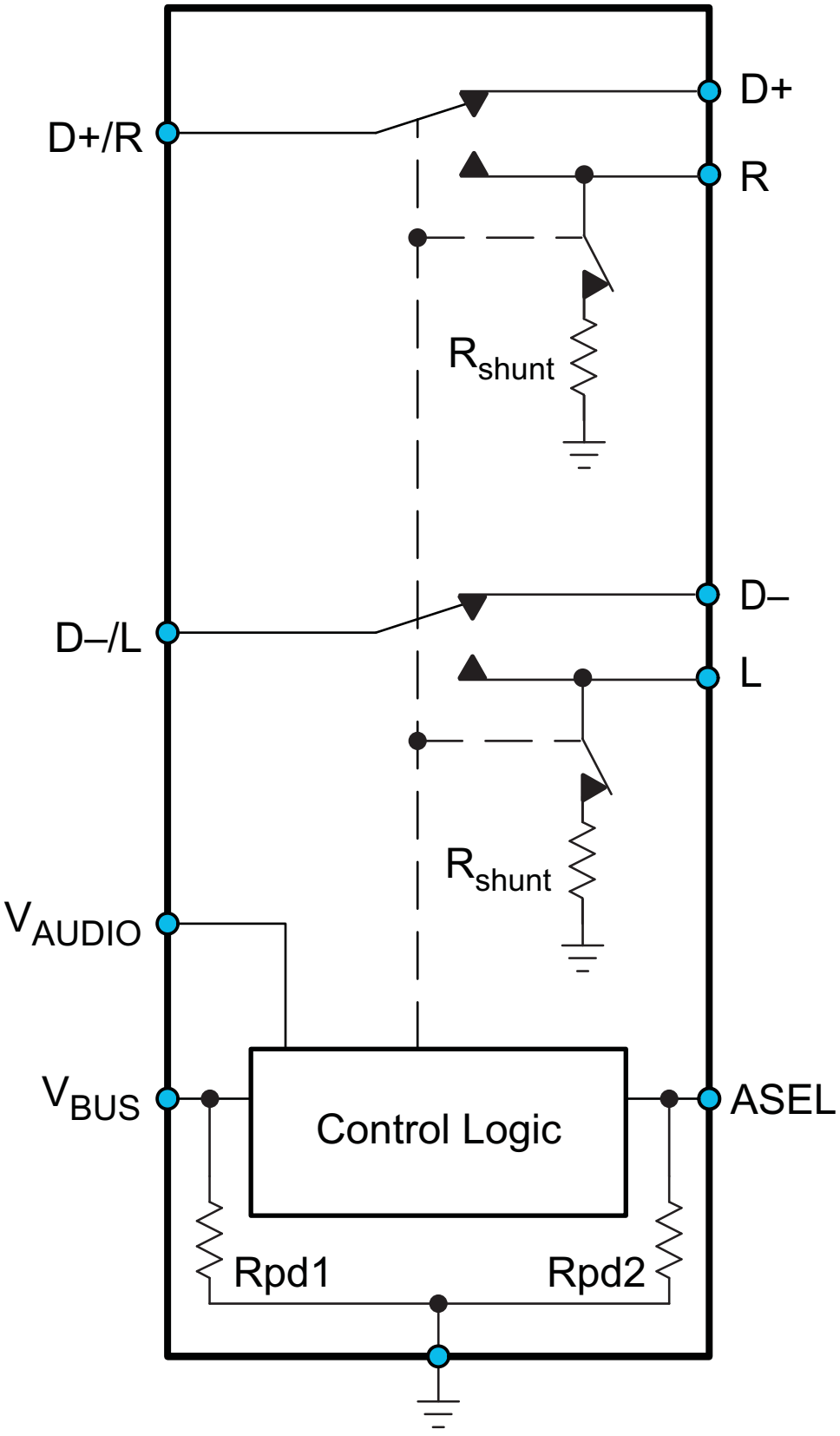
A_{SEL}	V_{AUDIO}	V_{BUS}	L,R	D+, D–
L	L	L	OFF	OFF
L	L	H	OFF	OFF
L	H	L	ON	OFF
L	H	H	OFF(1)	ON
H	L	L	OFF	OFF
H	L	H	OFF	OFF
H	H	L	ON	OFF
H	H	H	ON	OFF

(1) 100Ω shunt resistors are enabled in this state.

TYPICAL APPLICATION BLOCK DIAGRAM



SWITCH BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{AUDIO}	Supply voltage range(3)		–0.5	6.5	V
V_{D+} $V_{D–}$	Analog voltage Range(3)		–0.5	6.5	V
V_R V_L			V_{AUDIO} – 6.5	V_{AUDIO} + 0.5	V
I_K	Analog port diode current	V_{D+}, $V_{D–}$ < 0	–50		mA
I_{D+}, $I_{D–}$ I_R, I_L	ON-state switch current	V_{D+}, $V_{D–}$ = 0 to V_{AUDIO}, V_R, V_L $V_{D+/R}$, $V_{D–/L}$ = V_{AUDIO} – 5.5 V to V_{AUDIO}	–100	100	mA
$I_{D+/R}$ $I_{D–/L}$	ON-state peak switch current(4)		–200	200	
V_I	Digital input voltage range		–0.5	6.5	V
I_{IK}	Digital logic input clamp current(3)	V_I < 0		–50	mA
I_{AUDIO}	Continuous current through V_{AUDIO}			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Pulse at 1-ms duration <10% duty cycle.

PACKAGE THERMAL IMPEDANCE(1)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
θ_{JA}	Package thermal impedance	RSW package	175	°C/W

(1) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS

T_A = –40°C to 85°C, typical values are at V_{AUDIO} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
USB SWITCH							
V_{D+},$V_{D–}$	Analog voltage range			0		5.5	V
r_{on}	ON-state resistance	V_{AUDIO} = 3 V, V_{BUS} = 5 V, V_{ASEL} = 0 V, $V_{D+/D–}$ = 0 V, 0.4 V, I_{ON} = –8 mA	Switch ON		4	7	Ω
Δr_{on}	ON-state resistance match between channels	V_{AUDIO} = 3 V, V_{BUS} = 5 V, V_{ASEL} = 0 V, $V_{D+/D–}$ = 0 V, 0.4 V, I_{ON} = –8 mA	Switch ON			0.3	Ω
$I_{D+(OFF)}$ $I_{D–(OFF)}$	D+ ,D- OFF leakage current	V_{AUDIO} = 3.6 V, V_{BUS} = 0 V, V_{ASEL} = 3.6 V, V_{D+} ,$V_{D–}$ = 0.3 V, $V_{D+/R}$,$V_{D–/L}$ = 0.3 V	Switch OFF			±50	nA
$I_{D+(ON)}$ $I_{D–(ON)}$	D+ ,D– ON leakage current	V_{AUDIO} = 3.6 V, V_{BUS} = 5 V, V_{ASEL} = 0 V, V_{D+} ,$V_{D–}$ = 0.3 V, $V_{D+/R}$ = Open	Switch ON			±50	nA
AUDIO SWITCH							
V_R,V_L	Analog voltage range			V_{AUDIO} – 5.5		V_{AUDIO}	V
r_{on}	ON-state resistance	V_{AUDIO} = 3 V, V_{BUS} = 0 V, V_{ASEL} = 3 V, $V_{L/R}$ = –2 V, 0 V, 0.7 V, I_{ON} = –26 mA	Switch ON		3	5	Ω
Δr_{on}	ON-state resistance match between channels	V_{AUDIO} = 3 V, V_{BUS} = 0 V, V_{ASEL} = 3 V, $V_{L/R}$ = 0.7 V, I_{ON} = –26 mA	Switch ON			0.3	Ω
$r_{on\ (flat)}$	ON-state resistance flatness	V_{AUDIO} = 3 V, V_{BUS} = 0 V, V_{ASEL} = 3 V, $V_{L/R}$ = –2 V, 0 V, 0.7 V, I_{ON} = –26 mA	Switch ON		1.5	2.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

T_A = –40°C to 85°C, typical values are at V_{AUDIO} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
r_{SHUNT}	Shunt resistance	V_{AUDIO} = 3 V, V_{BUS} = 5 V, V_{ASEL} = 0 V, $V_{L/R}$ = 0.7 V, I_{OSHUNT} = 10 mA	Switch OFF		100	200	Ω
$I_{L(OFF)}$ $I_{R(OFF)}$	L , R OFF leakage current	V_{AUDIO} = 3.6 V, V_{BUS} = 5 V, V_{ASEL} = 0 V, V_R, V_L = 0.3 V, V_{AUDIO}–0.3 V, $V_{D+/R}$, $V_{D–/L}$ = 0.3 V, V_{AUDIO}–0.3V	Switch OFF			±50	nA
$I_{L(ON)}$ $I_{R(ON)}$	L , R ON leakage current	V_{AUDIO} = 3.6 V, V_{BUS} = 0 V, V_{ASEL} = 3.6 V,D+/R, D–L = 0.3 V, V_R, V_L = 0.3 V, V_{AUDIO}–0.3 V, V_{AUDIO}–0.3V $V_{D+/R}$, $V_{D–/L}$ =Open	Switch ON			±50	nA
DIGITAL CONTROL INPUTS (A_{SEL}, V_{BUS})							
V_{IH}	Input logic high	V_{AUDIO} = 2.7V to 5.5V		1.2			V
V_{IL}	Input logic low	V_{AUDIO} = 2.7V to 5.5V				0.5	V
I_{IN}	Input leakage current	V_{AUDIO} = 3.6V	VIN = 3.6V			±10	µA
			VIN = 0V			±1	
r_{PD1}	Internal pulldown resistance				3		MΩ
r_{PD2}	Internal pulldown resistance				5		MΩ

DYNAMIC CHARACTERISTICS

T_A = –40°C to 85°C, typical values are at V_{AUDIO} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
USB SWITCH							
t_{ON}	Turn-on time	V_{AUDIO} = 3 V, V_{BUS} = 0 V to 5 V, V_{ASEL} = 0 V, $V_{D+/R,\ D-/L}$ = 1 V, Figure 10			2		µs
t_{OFF}	Turn-off time	V_{AUDIO} = 3 V, V_{BUS} = 5 V to 0 V, V_{ASEL} = 0 V, $V_{D+/R,\ D-/L}$ = 1 V, Figure 10			1		µs
$t_{SK(O)}$	Channel-to-channel skew	f = 240 MHz, Figure 11			35		ps
$t_{SK(P)}$	Skew of opposite transitions of same output	f = t 240 MHz, Figure 11			25		ps
$C_{D+(OFF)}$ $C_{D-(OFF)}$	D+, D-OFF capacitance	V_{AUDIO} = 3 V, V_{BUS} = 0 V, A_{SEL} = 3 V, f = 240 MHz	Switch OFF		2.8		pF
$C_{D+(ON)}$ $C_{D-(ON)}$	D+, D– ON capacitance	V_{AUDIO} = 3 V, V_{BUS} = 5 V, A_{SEL} = 0 V, f = 240 MHz	Switch ON		12.5		pF
C_I	Digital input capacitance	V_{AUDIO} = 3 V, V_{BUS} = 0 V, A_{SEL} = 0 V, f = 1 MHz			2.2		pF
BW	Bandwidth	V_{AUDIO} = 3 V, V_{BUS} = 5 V, V_{ASEL} = 0 V, Figure 12	Switch ON		650		MHz
O_{ISO}	OFF Isolation	V_{AUDIO} = 3 V, V_{BUS} = 0 V, V_{ASEL} = 3 V, R_L = 50 Ω, f = 240 MHz, Figure 14	Switch OFF		–22		dB
X_{TALK}	Crosstalk	V_{AUDIO} = 3 V, V_{BUS} = 5 V, V_{ASEL} = 0 V, R_L = 50 Ω, f = 240 MHz, Figure 13	Switch ON		–31		dB
AUDIO SWITCH							
t_{ON}	Turn-on time	V_{AUDIO} = 3 V, V_{BUS} = 0 V or 5 V, V_{ASEL} = 0 V to 3 V, $V_{D+/R,D-/L}$ = 1 V, Figure 10			4		µs
t_{OFF}	Turn-off time	V_{AUDIO} = 3 V, V_{BUS} = 0 V, V_{ASEL} = 3 V to 0 V, $V_{D+/R,D-/L}$ = 1 V, Figure 10			1		µs
$C_{L(OFF)}$ $C_{R(OFF)}$	L , R OFF capacitance	V_{AUDIO} = 3 V, V_{BUS} = 5 V, V_{ASEL} = 0 V, f = 20 kHz	Switch OFF		4.5		pF
$C_{L(ON)}$ $C_{R(ON)}$	L, R ON capacitance	V_{AUDIO} = 3 V, V_{BUS} = 0 V, V_{ASEL} = 3 V, f = 20 kHz	Switch ON		15		pF
O_{ISO}	OFF Isolation	V_{AUDIO} = 3 V, V_{BUS} = 5 V, V_{ASEL} = 0 V, R_L = 50 Ω, f = 20 kHz, Figure 14	Switch OFF		–83		dB
X_{TALK}	Crosstalk	V_{AUDIO} = 3 V, V_{BUS} = 0 V, V_{ASEL} = 3 V, R_L = 50 Ω, f = 20 kHz, Figure 13	Switch ON		–83		dB
THD	Total harmonic distortion	V_{AUDIO} = 3 V, V_{BUS} = 0 V, V_{ASEL} = 3 V, f = 20 Hz to 20 kHz, R_L = 600 Ω, V_{IN} = 2 Vpp			0.05		%
SUPPLY							
V_{AUDIO}	Power supply voltage			2.7		5.5	V
I_{AUDIO}	Positive supply current	V_{AUDIO} = 3.6 V, V_{BUS} = 0 or 5 V, V_{ASEL} = 0 to 3.6 V, I_{OUT} = 0			6	10	µA
I_{OFF}	Power off leakage current	V_{AUDIO} = 0 V, $V_{D+/R,\ D-/L,\ D+,\ D-,\ L,\ R}$ = 0 to 5.5 V				±10	µA

TYPICAL CHARACTERISTICS

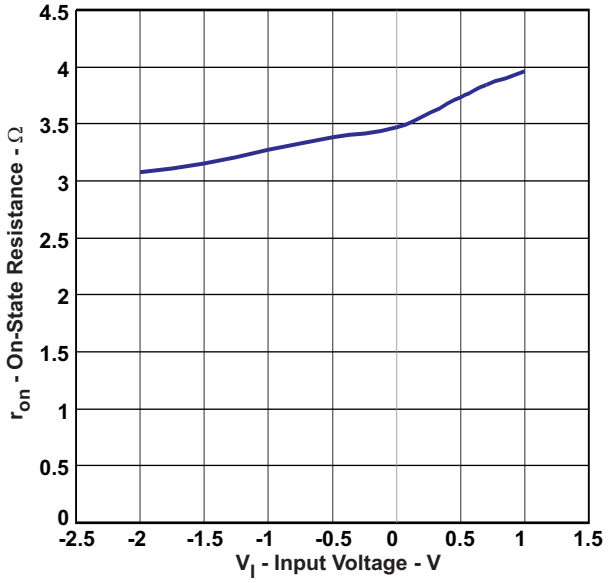


Figure 1. ON Resistance vs V_I for Audio Switch

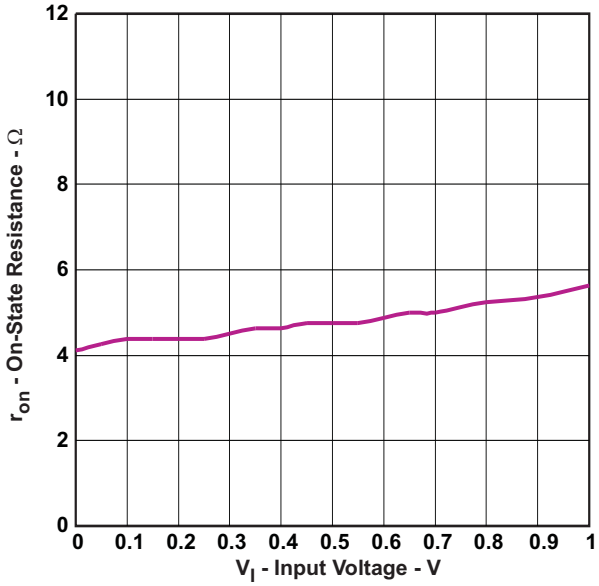


Figure 2. ON Resistance vs V_I for USB Switch

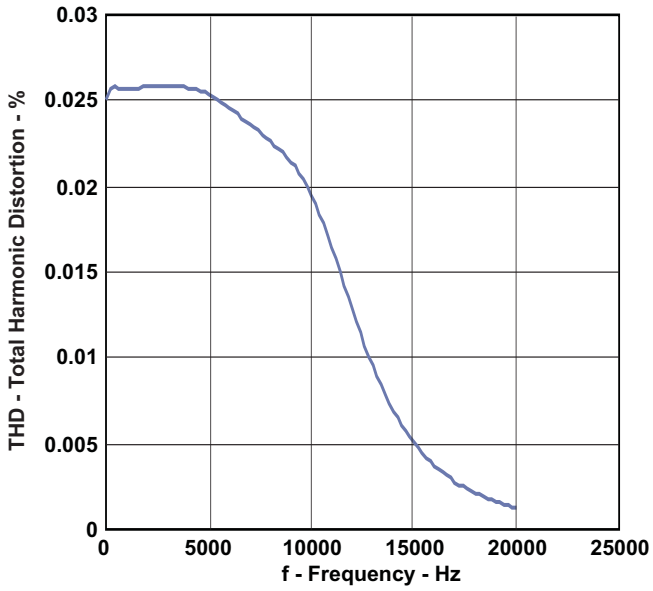


Figure 3. THD vs Frequency for Audio Switch

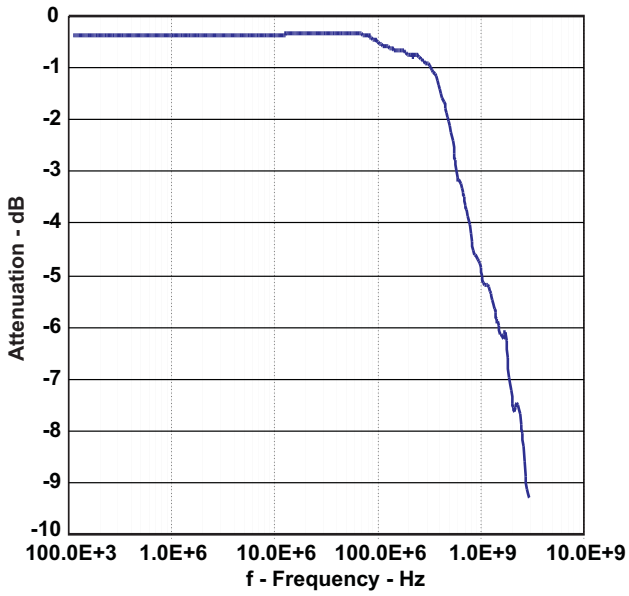


Figure 4. Gain vs Frequency for USB Switch

TYPICAL CHARACTERISTICS (continued)

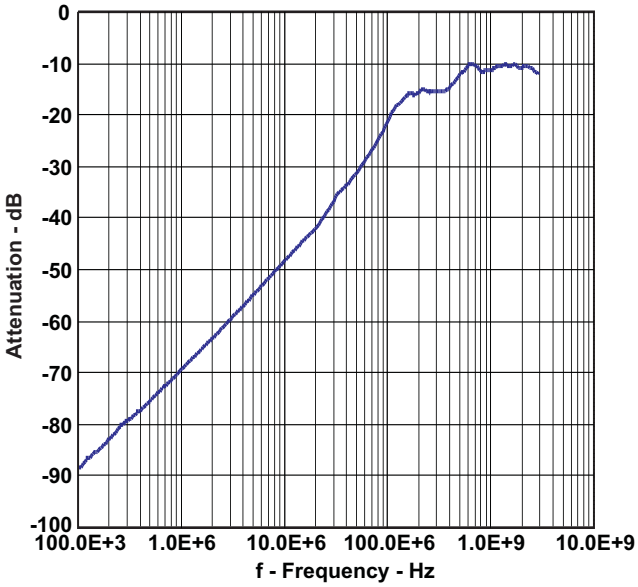


Figure 5. Off Isolation vs Frequency for Audio Switch

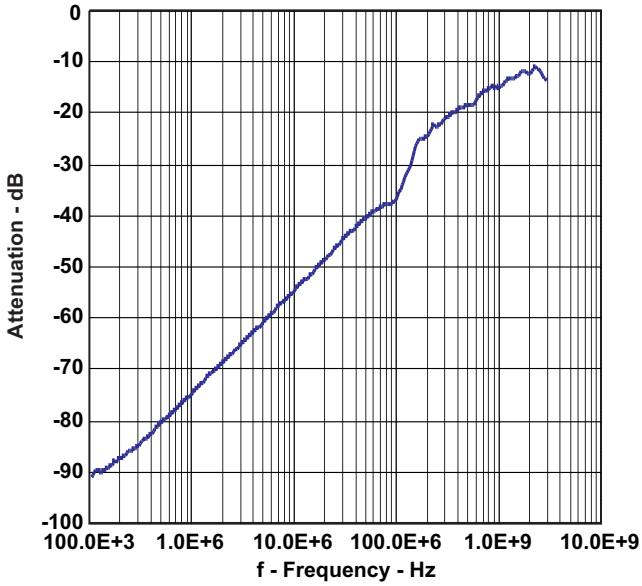


Figure 6. Off Isolation vs Frequency for USB Switch

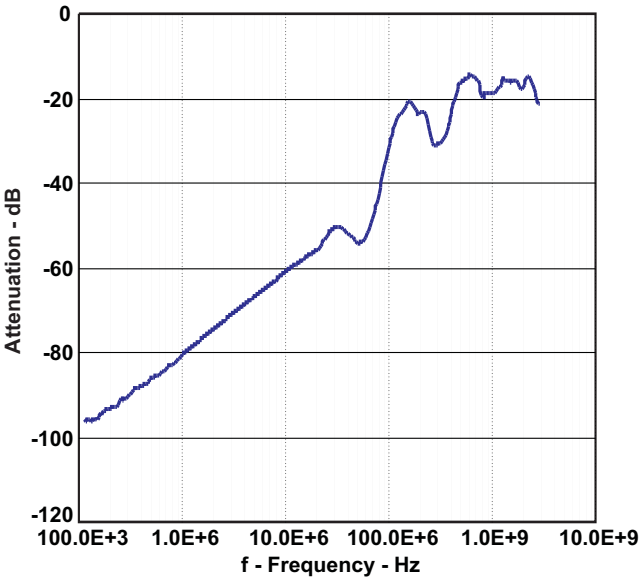


Figure 7. Cross Talk vs Frequency for Audio Switch

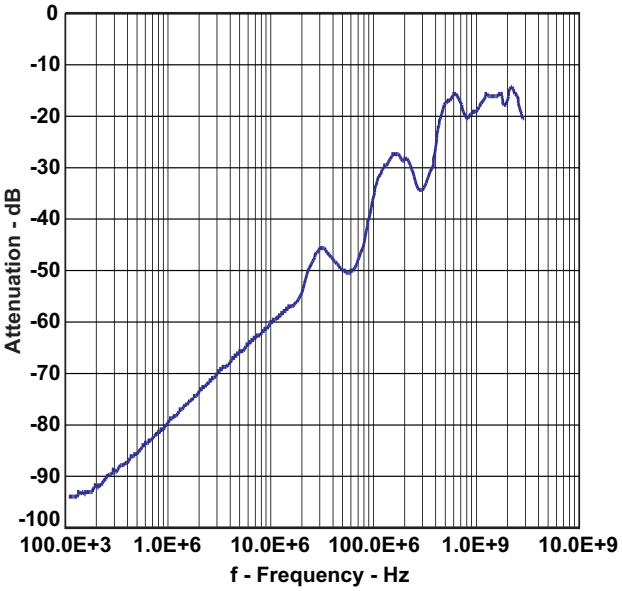


Figure 8. Cross Talk vs Frequency for USB Switch

TYPICAL CHARACTERISTICS (continued)

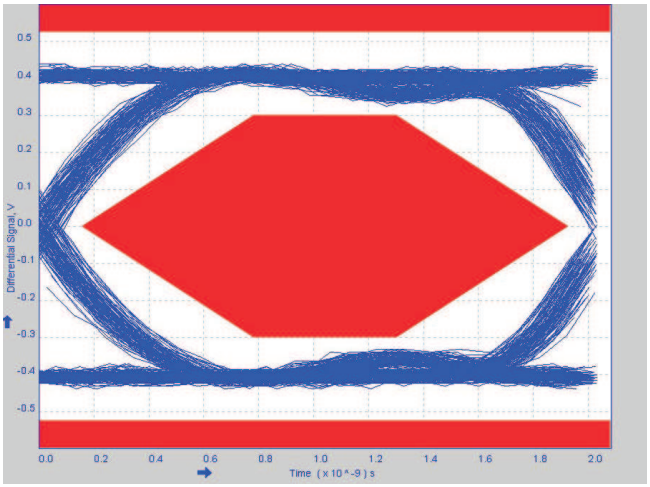
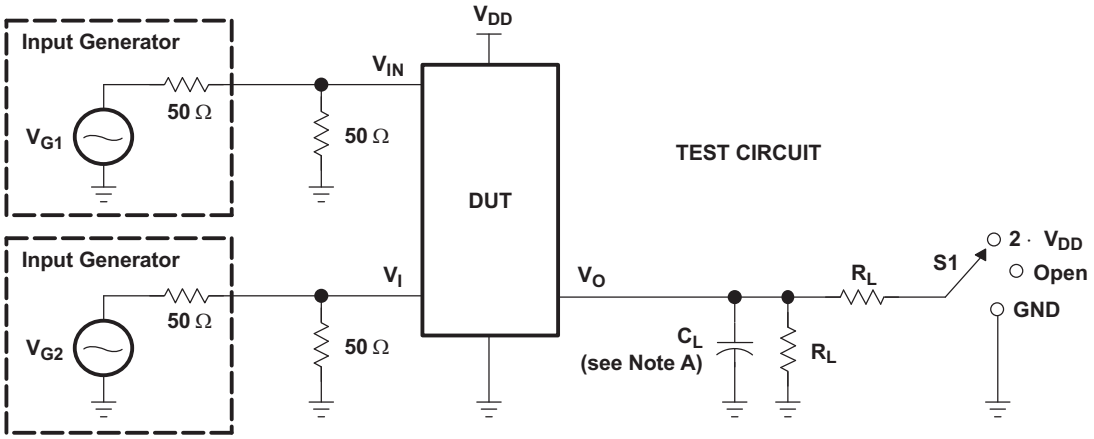
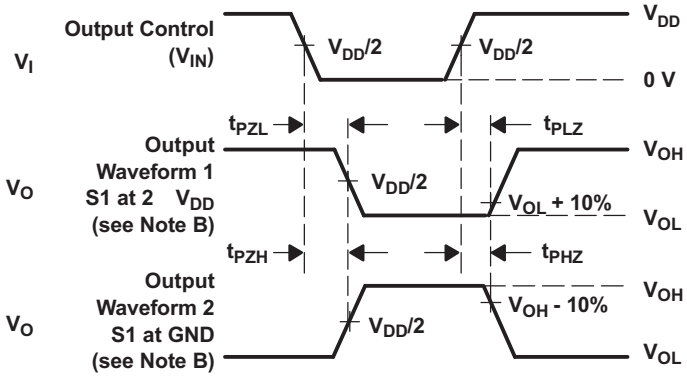


Figure 9. USB 2.0 Eye Pattern for USB Switch

PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



TEST	V_{AUDIO} (V_{DD})	S1	R_L	V_{in}	C_L	V_Δ
t_{PLZ}/t_{PZL}	3.3 V	2 · V_{DD}	200 Ω	GND	10 pF	0.3 V
t_{PHZ}/t_{PZH}	3.3 V	GND	200 Ω	V_{DD}	10 pF	0.3 V

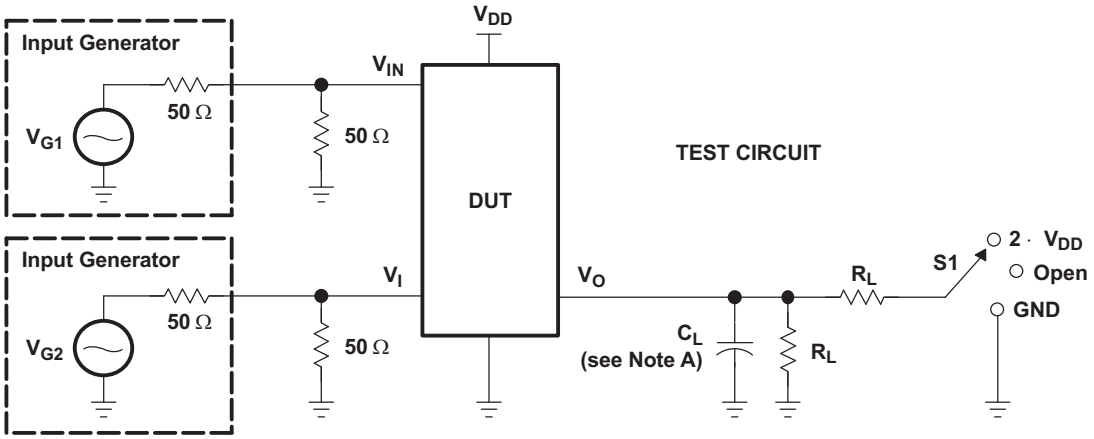


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

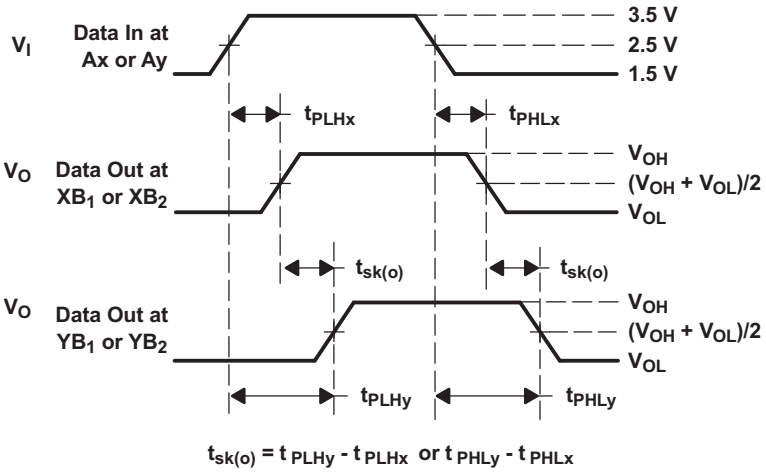
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis} or t_{OFF}.
F. t_{PZL} and t_{PZH} are the same as t_{en} or t_{ON}.

Figure 10. Test Circuit and Voltage Waveforms

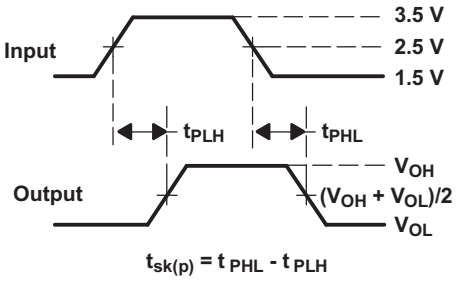
PARAMETER MEASUREMENT INFORMATION (Skew)



TEST	V_{AUDIO} (V_{DD})	S1	R_L	V_{in}	C_L
$t_{sk(o)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{DD} or GND	10 pF
$t_{sk(p)}$	3.3 V ± 0.3 V	Open	200 Ω	V_{DD} or GND	10 pF



VOLTAGE WAVEFORMS
OUTPUT SKEW ($t_{sk(o)}$)

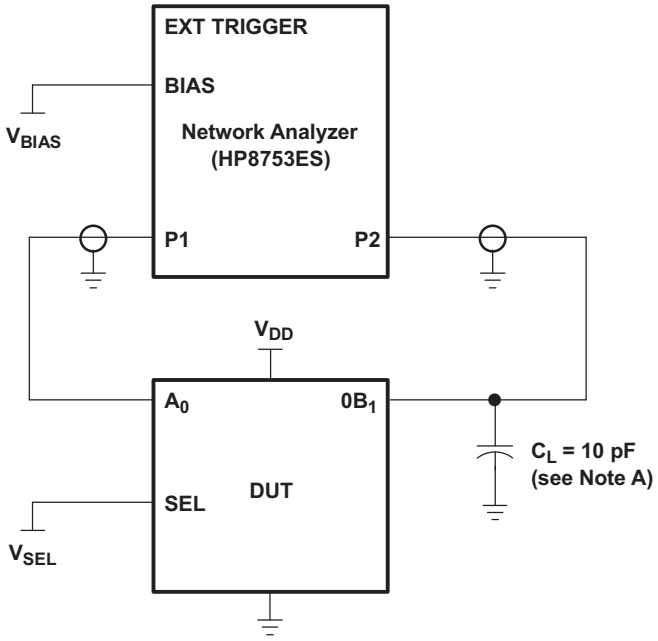


VOLTAGE WAVEFORMS
PULSE SKEW [$t_{sk(p)}$]

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

Figure 11. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



A. C_L includes probe and jig capacitance.

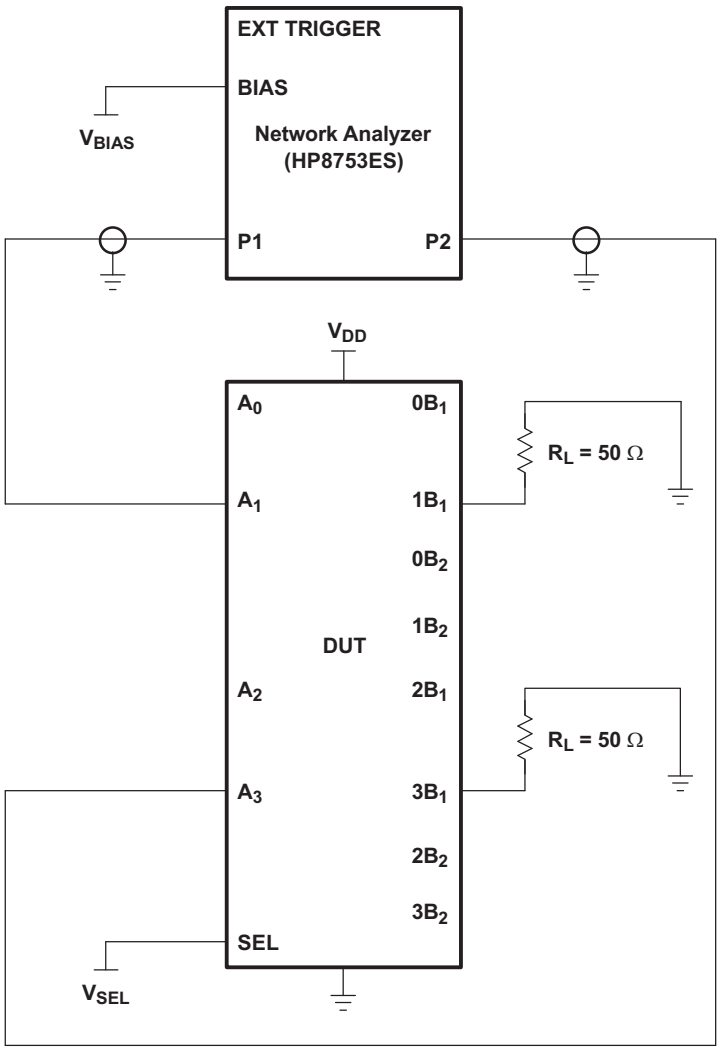
Figure 12. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_{SEL} = 0 and A_0 is the input, the output is measured at $0B_1$. All unused analog I/O ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

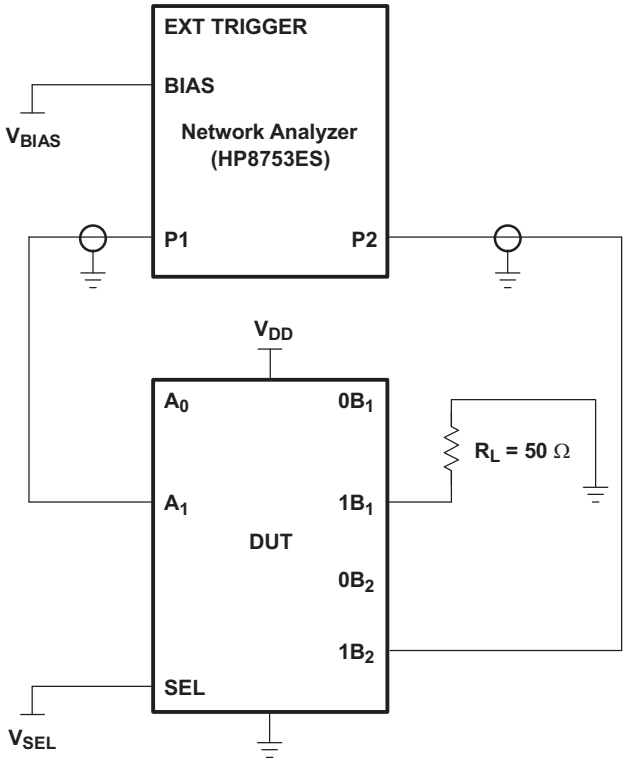
Figure 13. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_{SEL} = 0 and A_1 is the input, the output is measured at A_3. All unused analog input (A) ports are connected to GND, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L includes probe and jig capacitance.

B. A 50-Ω termination resistor is needed to match the loading of the network analyzer.

Figure 14. Test Circuit for OFF Isolation (O_{ISO})

OFF isolation is measured at the output of the OFF channel. For example, when V_{SEL} = GND and A_1 is the input, the output is measured at $1B_2$. All unused analog input (A) ports are connected to ground, and output (B) ports are left open.

HP8753ES Setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5USBA224RSWR	ACTIVE	UQFN	RSW	10	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(A5R, A5V)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

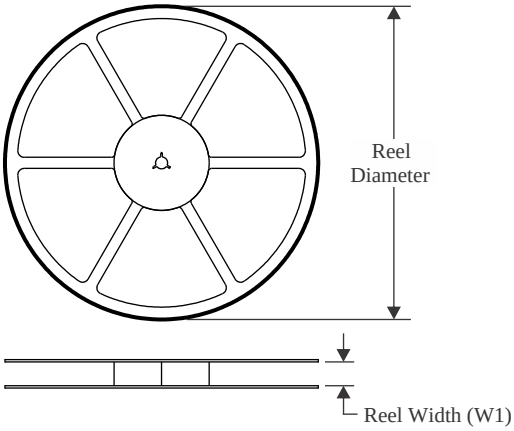
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

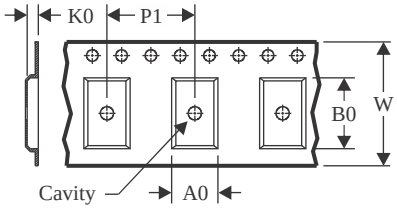
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

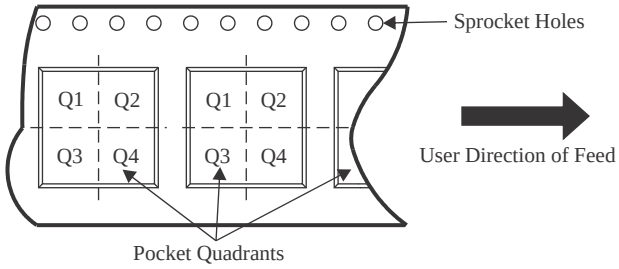


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

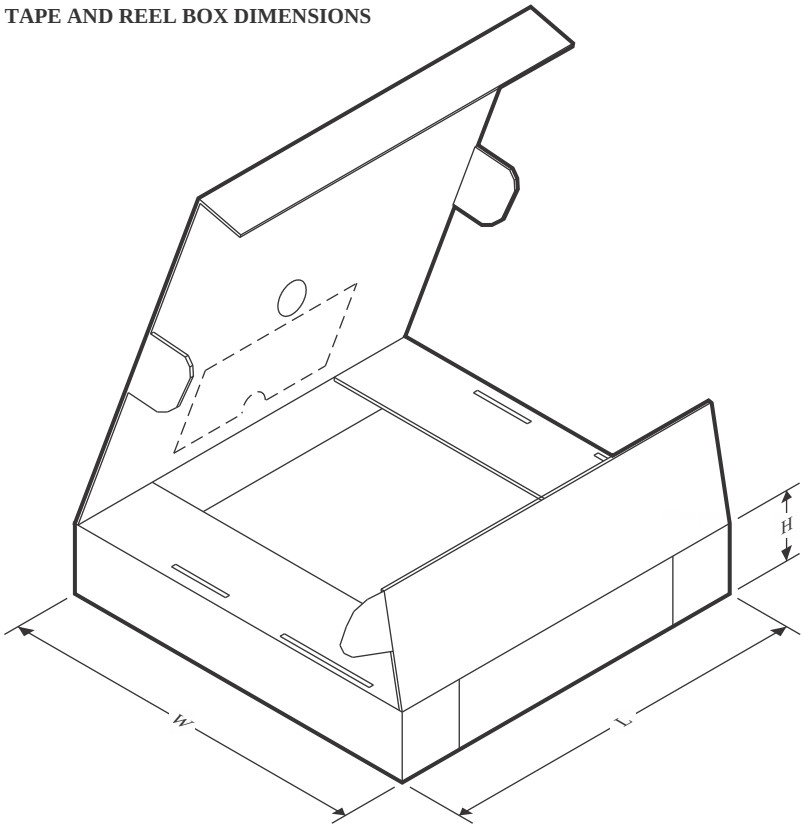
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5USBA224RSWR	UQFN	RSW	10	3000	180.0	9.5	1.6	2.0	0.8	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

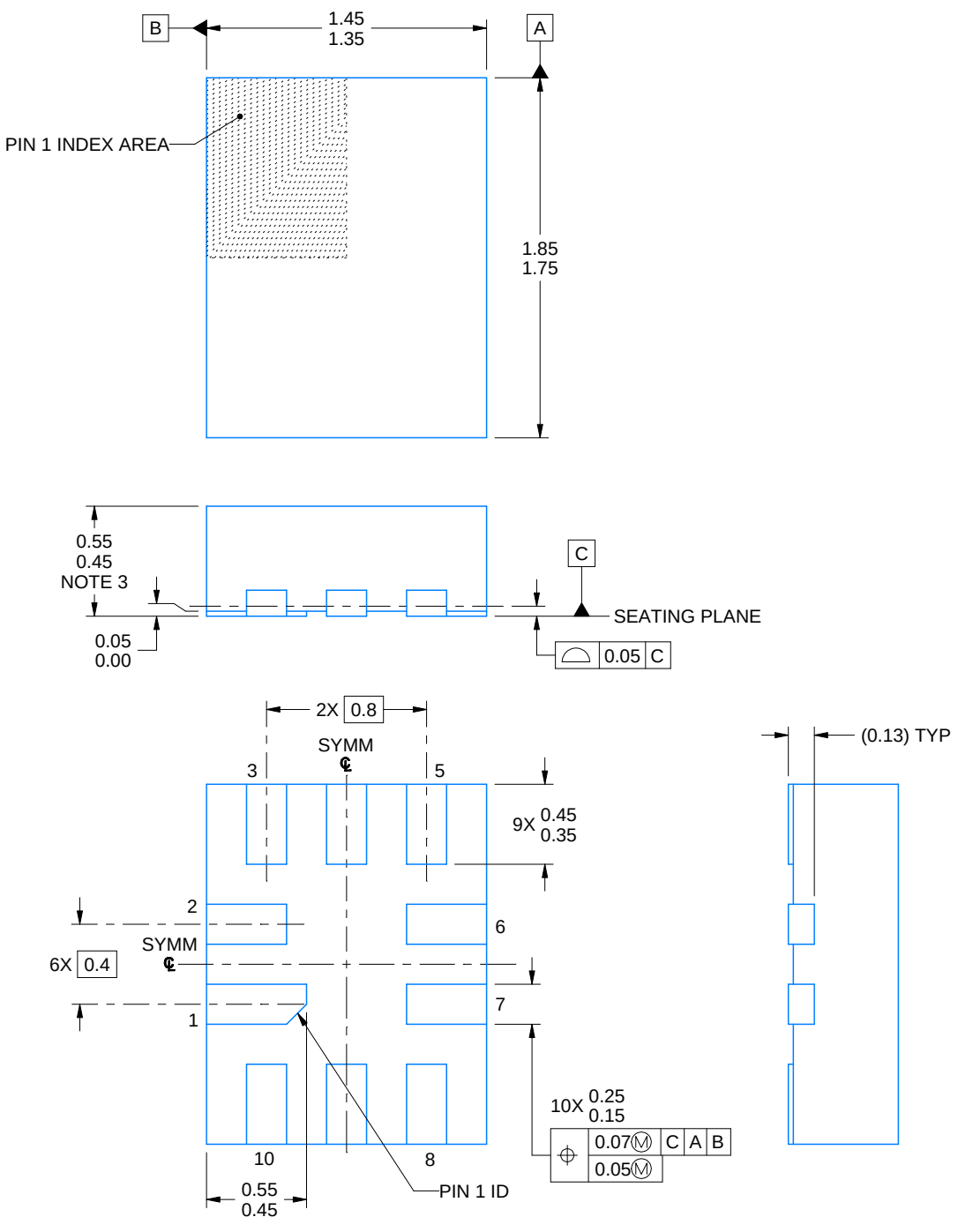
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5USBA224RSWR	UQFN	RSW	10	3000	189.0	185.0	36.0

PACKAGE OUTLINE

RSW0010A

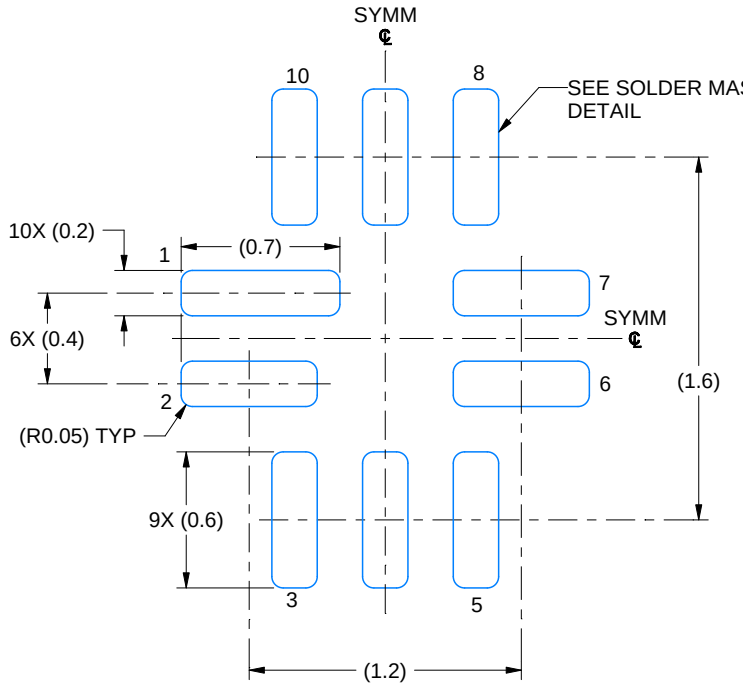
UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

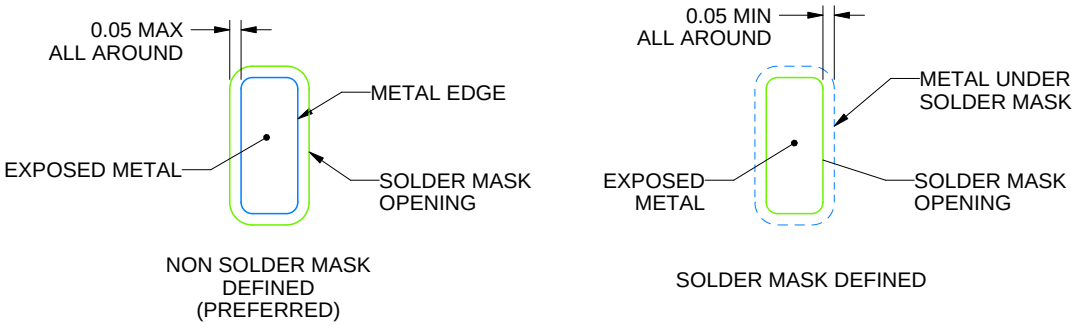


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package complies to JEDEC MO-288 variation UDEE, except minimum package height.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

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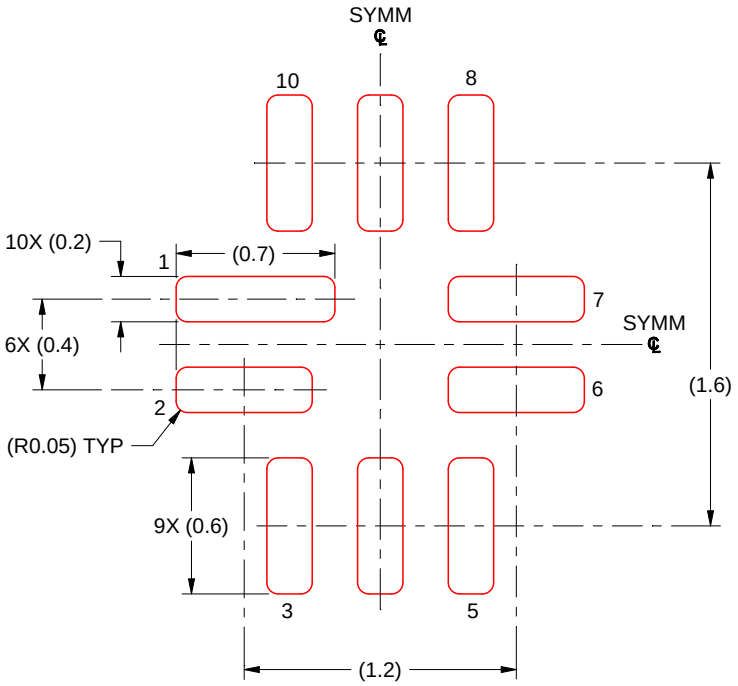
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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