Application Report

Voltage Level Translation for SPI, UART, and JTAG Interfaces With Focus On 2N7001T

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ABSTRACT

This application report discusses the SPI, UART, and JTAG interface standards. Voltage level translation using the 2N7001T and AXC family of translators along with the usage examples in video doorbell and wireless speaker end equipments are discussed.

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Trademarks

1 Introduction

The 2N7001T is a single bit unidirectional level shifter device. This voltage signal converter uses two separate configurable power supply rails to translate an unidirectional signal up or down. The device helps system designers implement unidirectional level shifting solutions while reducing component count and board space compared to discrete level shifting implementations. The key features for this device are listed in Table 1-1:

Table 1-1. 2N7001T Features

PARAMETER	2N7001T
Voltage Support	1.65 V – 3.6 V
Data Rate	100 Mbps
Drive Strength	12 mA
Icc (AXC1T at 125°C)	14 µA
ESD Ratings	2 kV HBM, 1 kV CDM
Operating Temperature	-40°C to 125°C
Power Sequencing	Not Required
Ioff Partial Power Down	Supported
Packages	SC-70 (DCK) and X2SON (DPW)

Signal level shifting is necessary to enable communication between two devices which are operating at different voltage levels. A common level shifting example would be the communication of a processor I/O at 1.8 V and a peripheral device I/O that operates at 3.3 V. The 2N7001T is able to provide a great solution to level shifting due to the buffered architecture of the device. Watch *2N7001T Introduction* and refer to the application report *Common Risks of Discrete FET Voltage Translation and Advantages of TI's Ontegrated 2N7001T Level Shifter*.

This device can be utilized for common communication interface standards such as Serial Peripheral Interface (SPI), Universal asynchronous receive transmit (UART), Joint Test Access Group (JTAG), or the General purpose Input output (GPIO) pins such as enable or restart. The basics of these interfaces as well as the operation of the 2N7001T level shifter with these standard interfaces are discussed in the following sections. Examples of level translation used in building automation like video doorbell and personal electronics applications such as wireless speakers are discussed as well. Figure 1-1 and Figure 1-2 shows the leaded SC-70 DCK package and the non-leaded X2SON DPW package that the 2N7001T device is available in.

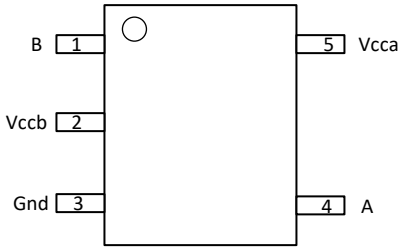

Figure 1-1. 2N7001T DCK (SC-70) Package

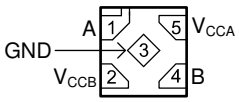

Figure 1-2. 2N7001T DPW (X2SON) Package

2 Common Interfaces and 2N7001T Implementation

2.1 General Purpose Input Output (GPIO)

Communication between any two devices occur when a signal is sent from the output of one device to the input of the interfacing device; the core device and the peripheral devices, however, might be operating at different voltage levels, which is why a level shifter is needed in between them to facilitate the communication. If the required signals are not shifted to the voltage at which the core device is operating, then the reliability of communication is impacted. The 2N7001T provides a good solution for voltage translating common control I/O signals such as enable or restart. Figure 2-1 shows how the clock buffering, power good, error flag, reset, memory error, processor overheat, LED, and display driving are other common signal types that often need level shifting.

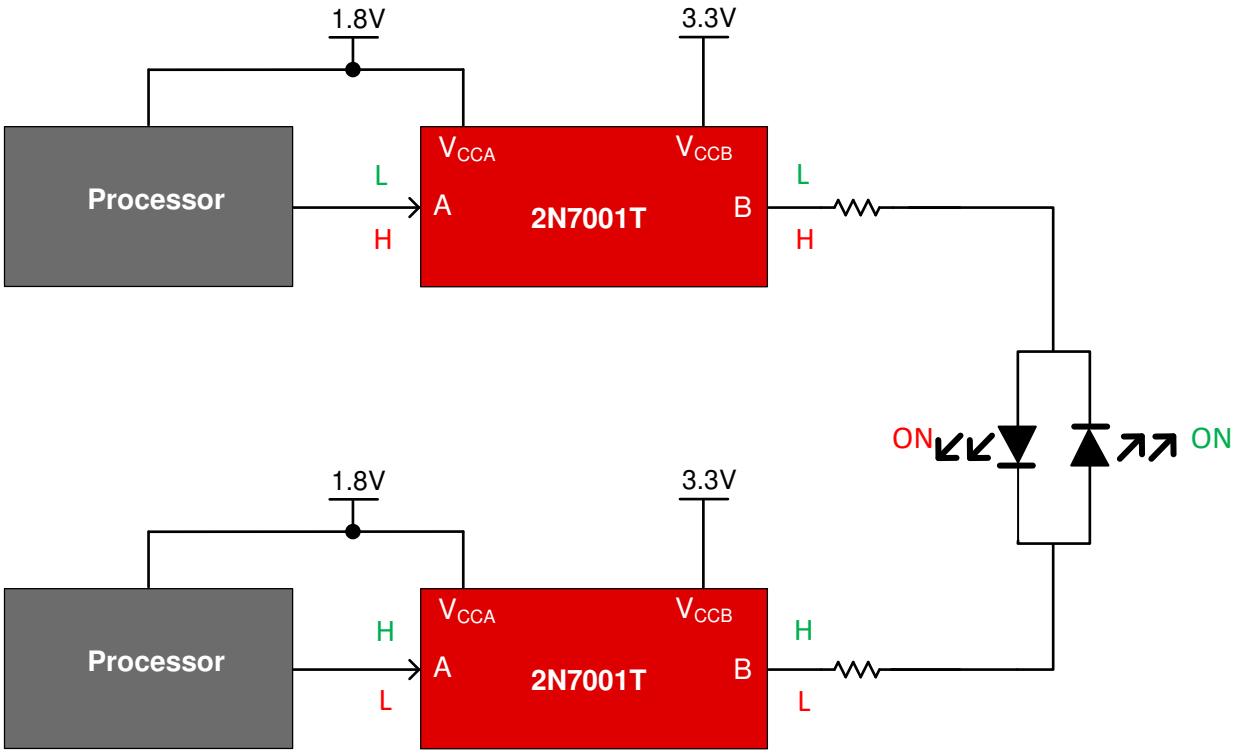

Figure 2-1. Driving LED with Translation Using 2N7001T

3 Serial Peripheral Interface (SPI)

SPI provides synchronous communication between a processor and a peripheral device. Table 3-1 shows how the SPI interface has a total of four signal lines.

Table 3-1. SPI Interface

SIGNAL	DESCRIPTION	DIRECTION
CLK	Clock Signal	Controller to Peripheral
CIPO	Controller Input/Peripheral Output	Peripheral to Controller
COPI	Controller Output/Peripheral Input	Controller to Peripheral
CS	Peripheral Select	Controller to Peripheral

The first is the clock (CLK), which only the controller can control. The controller can transmit one bit of data or receive one bit of data from the peripheral on each pulse of the CLK. Since SPI is full duplex, it requires one line for transmission (COPI) and one line for receiving data (CIPO), meaning it can receive and transmit at the same time. Finally, there is a line for peripheral select (CS) which activates the peripheral.

Communication occurs when the peripheral select line is held low to initiate communication, and then one bit of data is transmitted or received on each clock pulse. This communication is only possible if the peripheral device and the processor are operating at the same voltage levels. Since this is usually not the case, the 2N7001T can be used to provide a unidirectional level shift for the CIPO line. *SN74AXC4T245 Four-bit Bus Transceiver with Configurable Voltage Translation and Tri-State Outputs* data sheet shows how the three other lines that are operating in the opposite direction can be level shifted using the SN74AXC4T245, which is a 4-bit direction controlled level shifter. The 2N7001T can easily operate with data rates of up to 100 Mbps, which is usually within the recommended communication speeds for SPI interface. Alternatively, the SN74AXC4T774 or TXB0104 devices can work as a single chip solution.

3.1 Application – SPI

SPI has the ability to support high data rates and full duplex data communication while having a simple hardware interface and complete protocol flexibility for the bits transferred. Due to these advantages, SPI is implemented in many application use cases. *Video Doorbell* is one example of the use of SPI protocol. It is the preferred communication method for sensors, control devices, camera lenses, memory, LCD, and SD cards.

Another notable use case involves the control devices in the two way audio communication block. The SPI communication protocol is commonly used in ADC, DAC, CODEC, and DSP processors. Another critical advantage of using SPI instead of I^2C for these devices is that SPI allows for a faster data rate. This results in a higher sample rate, which produces better sound quality.

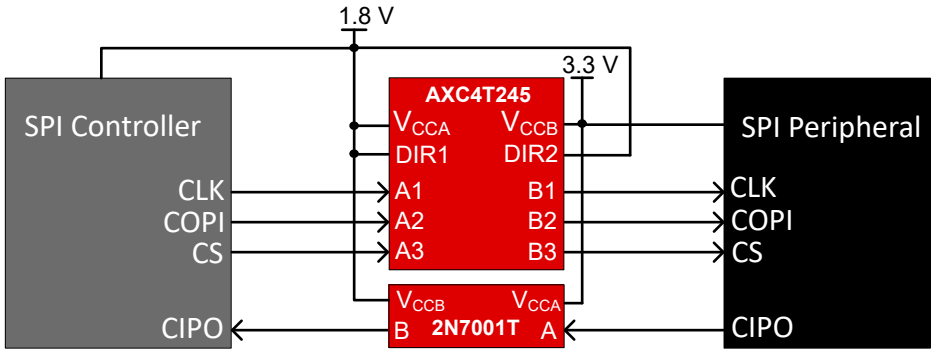

Figure 3-1. SPI Interface Using SN74AXC4T245 and 2N7001T Devices

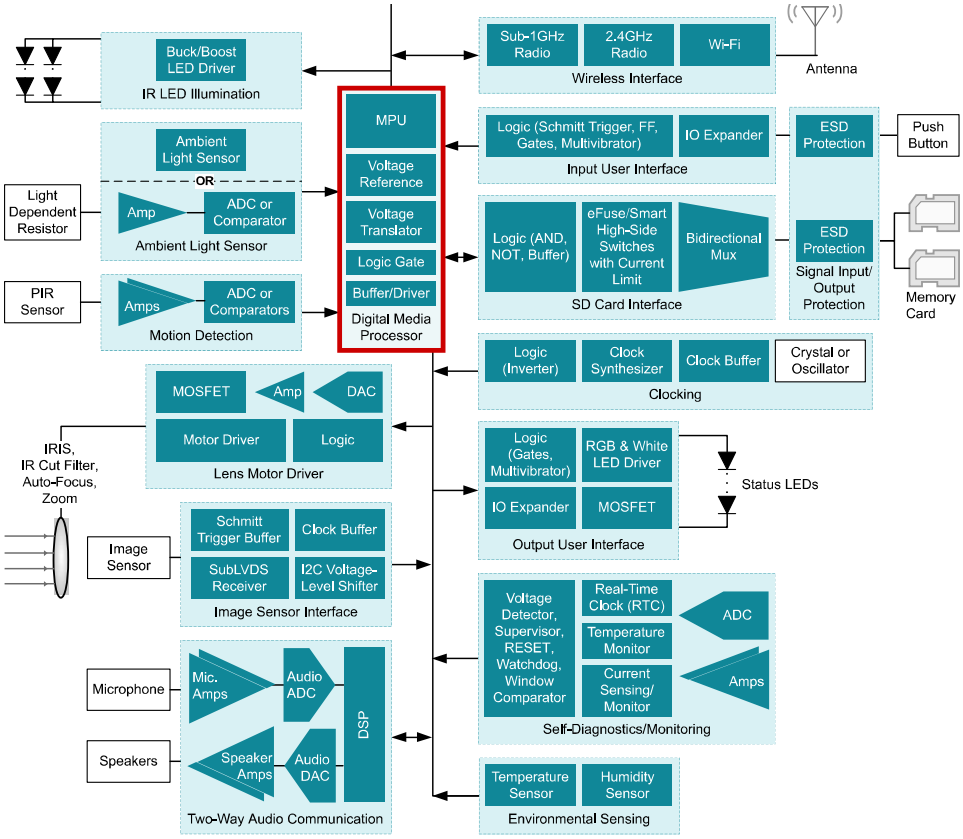

Figure 3-2. SPI Interface in Video Doorbell

4 Universal Asynchronous Receive Transmit (UART)

UART is an asynchronous, moderate speeds, full duplex communication interface with either two or four channels; TX (transmit), RX (receive), or RX ,RTS, CTS, and TX.

Communication occurs with a start bit being sent, the data line being pulled from high to low in the middle of a bit period. The start bit is followed by 8 bits of information and a stop bit, the data line going from a logic low to a logic high in the middle of a bit period. Certain communication protocols sometimes have a parity bit which confirms that the correct information was transferred. UART does not depend on a clock line because the receiver and transmitter will have internal clocks that can be set to a selected baud rate or bits per second (usually from 300 bps to 115 kbps) for transmission.

For the UART interfaces to operate appropriately between two devices that are at different voltages, for example 1.8 V to 3.3 V, two of the 2N7001T unidirectional level shifters can be used at each of the signal lines. Since the device can up translate or down translate, it can be used for the receive and transmit lines.

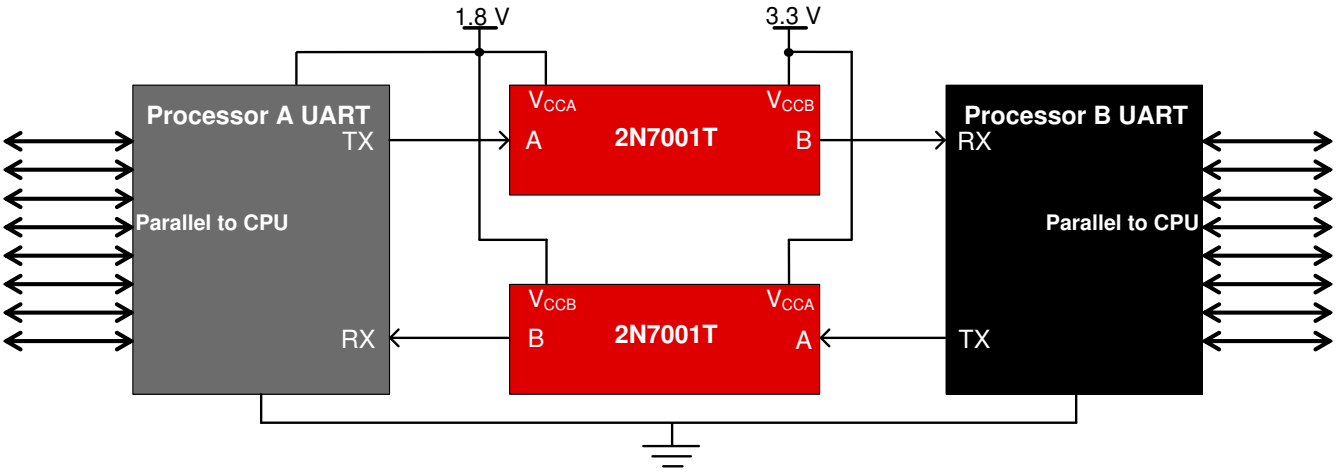

Figure 4-1. Two-Wire UART Interface Using 2N7001T Device

4.1 Application – UART

A common use case for UART interfaces is as a communication link between devices.

An example is the communication between the circuits of a *wireless speaker*. The 2N7001T provides a simple solution for voltage level shifting between the processor and MCU. Figure 4-2 shows how an UART interface could be used for enabling the communication between the processor and the Wi-Fi block.

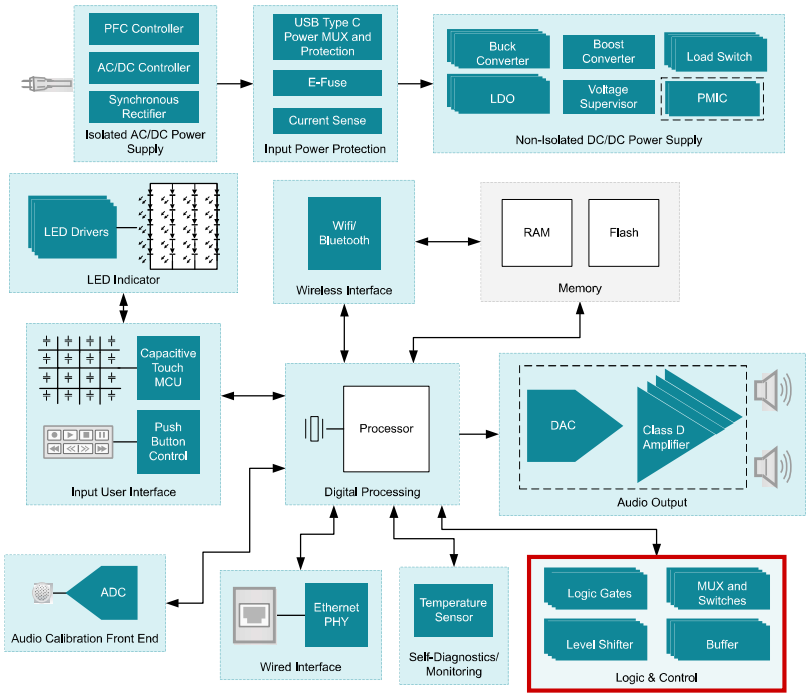

Figure 4-2. UART Interface in Wireless Speakers

5 Joint Test Access Group (JTAG)

The Joint Test Access Group developed a hardware interface to allow for the debugging, programming, and testing of embedded devices. JTAG, similar to SPI, operates using a set of five JTAG interface signals as shown in Table 5-1.

Table 5-1. JTAG Interface

SIGNAL	DESCRIPTION	DIRECTION
TCK	Test Clock Signal	Controller to Debugger
TDI	Test Data In	Controller to Debugger
TDO	Test Data Out	Debugger to Controller
TMS	Test Mode Select	Controller to Debugger
TRST (Optional)	Test Reset	Controller to Debugger

The test clock is used to provide a steady timing signal at which the test data will arrive. The test mode select allows the user to select what section or circuit is going to be tested. The JTAG protocol depends on the device being tested. TDI is the pin that is used to perform the test and the results are returned through the TDO pin. The optional test reset pin allows the ability to reset JTAG to a known good state.

Usually, there are multiple devices on a board that need to be tested via the JTAG interface. Using JTAG, these devices can be daisy chained to each other with the TDO pin, which extends out of the last device in the chain. If this last device in the daisy chain is on a different voltage level, the 2N7001T can be used for a voltage translation. The signal flow of TDO is opposite to the direction of the other pins allowing for the use of the 2N7001T in combination with SN74AXC4T245, for the remaining three channels.

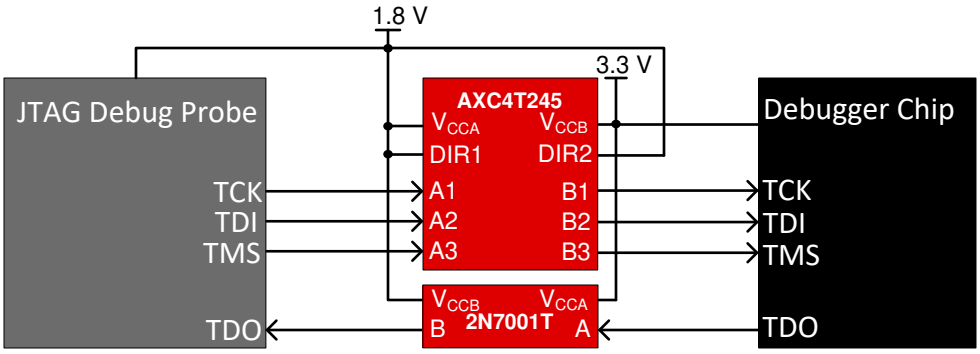

Figure 5-1. JTAG Interface Using 2N7001T Device

5.1 Application – JTAG

A voltage level translator is necessary while interfacing numerous sub-systems that operate at different voltage levels. In enterprise computing applications, JTAG interface can be found in *Campus and Branch Switches* as shown in Figure 5-2. The JTAG port enables easier debugging during periodic maintenance of the server.

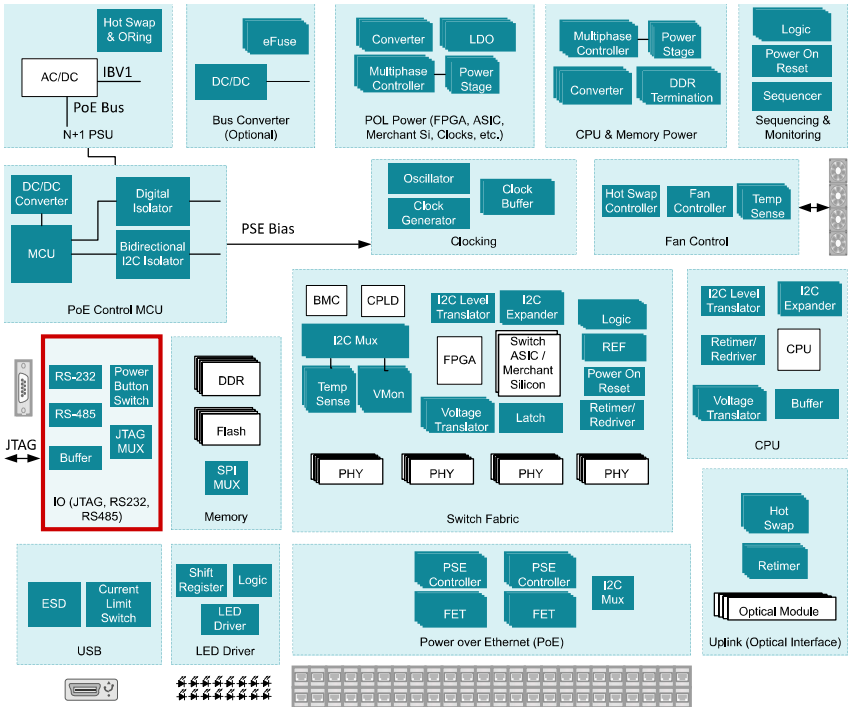

Figure 5-2. JTAG Translation in Campus Branch Switches

6 Additional Resources

- Texas Instruments, *2N7001T Evaluation Module* user's guide
- Texas Instruments, *Common Risks of Discrete FET Voltage Translation and Advantages of TI's Ontegrated 2N7001T Level Shifter* application report
- Texas Instruments, *Glitch Free Power Sequencing With AXC Level Translators* application report
- Texas Instruments, *Optomizing Video Doorbell Designs with Common Logic Use Cases* application report
- Texas Instruments, *SN74AXC4T245 Four-bit Bus Transceiver with Configurable Voltage Translation and Tri-State Outputs* data sheet

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2019) to Revision A (March 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2
• Updated the SPI terms throughout the document	2

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