Functional Safety Information

TPS62871-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPS62871-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

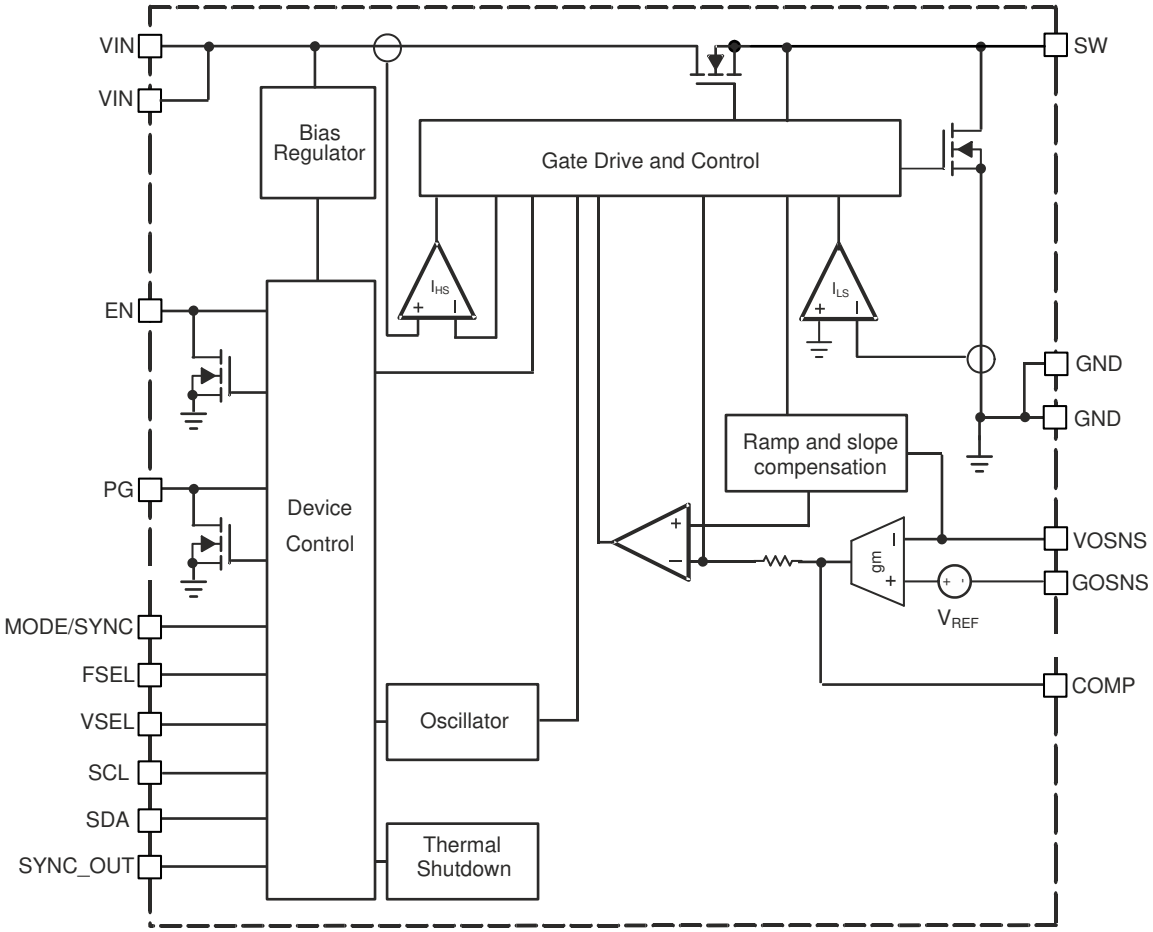

Figure 1-1. Functional Block Diagram

The TPS62871-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPS62871-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	4
Package FIT Rate	6

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 750 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS62871-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
SW no output	20%
SW output not in specification – voltage or timing	15%
SW power HS or LS FET stuck on	35%
EN or PG false trip or fails to trip	10%
Switching frequency or output voltage range not in spec	10%
no device communication	10%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS62871-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS62871-Q1 pin diagram. For a detailed description of the device pins, please refer to the *Pin Configuration and Functions* section in the TPS62871-Q1 data sheet.

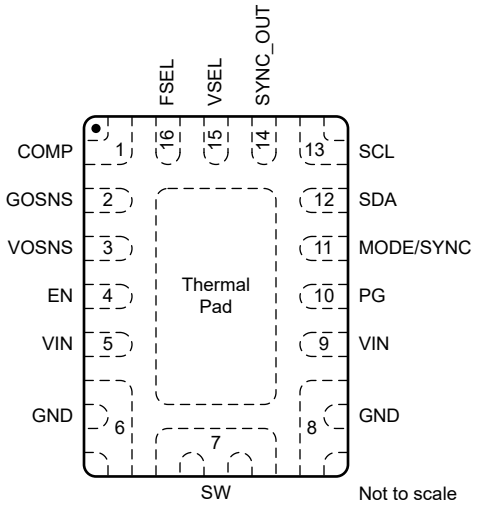

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- The device is running in the typical application. Please refer to the 'Simplified Schematics' on the first page in the *TPS6287x-Q 12.7-V to 6-V Input, 6-A/9-A/12-A/15-A, Automotive, Stackable,Synchronous Step-Down Converters with Fast Transient Response* data sheet.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	The device does not power up and there is no output voltage.	B
GOSNS	2	Normal operation, but output voltage accuracy gets worse	C
VOSNS	3	Maximum duty cycle operation and no regulated output voltage. Output voltage follows the input voltage.	B
EN	4	The device is disabled. Normal operation	C
VIN	5	The device does not power up and there is no output voltage.	B
GND	6	Normal operation	D
SW	7	Potential device damage	A
GND	8	Normal operation	D
VIN	9	The device does not power up and there is no output voltage.	B
PG	10	Normal operation and loss of PG indication	B
MODE/SYNC	11	Normal operation. Power save mode is enabled.	C
SDA	12	Normal operation and no I^2C communication	B
SCL	13	Normal operation and no I^2C communication	B
SYNC_OUT	14	Potential device damage	A
VSEL	15	Normal operation. Defines start-up voltage	C
FSEL	16	Normal operation. Defines switching frequency	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	No loop compensation and can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B
GOSNS	2	No output voltage regulation and can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B
VOSNS	3	No output voltage regulation and can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B
EN	4	Undetermined device operation. The device can power up and operate normal. Stays turned off	B
VIN	5	Normal operation. Pin 9 is still connected.	C
GND	6	Normal operation. Pin 8 and the exposed thermal pad are still connected.	C
SW	7	No output voltage	B
GND	8	Normal operation. Pin 6 and the exposed thermal pad are still connected.	C
VIN	9	Normal operation. Pin 5 is still connected.	C
PG	10	Normal operation and loss of PG indication	B
MODE/SYNC	11	Normal operation. Operation mode is undefined.	B
SDA	12	Normal operation and no I^2C communication	B
SCL	13	Normal operation and no I^2C communication	B
SYNC_OUT	14	Normal operation	D
VSEL	15	Normal operation. Start-up voltage is undefined.	B
FSEL	16	Normal operation. Switching frequency is undefined.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	2	The device does not power up and there is no output voltage.	B
GOSNS	2	3	Maximum duty cycle operation and no regulated output voltage. Output voltage follows the input voltage.	B
VOSNS	3	4	The device does not power up or there is potential device damage.	A
EN	4	5	Potential device damage	A
VIN	5	6	The device does not power up and there is no output voltage.	B
GND	6	7	Potential device damage	A
SW	7	8	Potential device damage	A
GND	8	9	The device does not power up and there is no output voltage.	B
VIN	9	10	Potential device damage	A
PG	10	11	Potential device damage if MODE/SYNC is tied high. Loss of PG indication	A
MODE/SYNC	11	12	Potential device damage if MODE/SYNC is tied high. No I^2C communication	A
SDA	12	13	Normal operation and no I^2C communication	B
SCL	13	14	Potential device damage	A
SYNC_OUT	14	15	Potential device damage if VSEL is tied high or low	A
VSEL	15	16	Normal operation. Defines start-up voltage and switching frequency	B
FSEL	16	1	No output voltage regulation and can cause the output voltage to oscillate. Oscillation frequency cannot be predicted.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
COMP	1	Potential device damage	A
GOSNS	2	Potential device damage	A
VOSNS	3	The device will not start up. Output voltage stays low or there is potential device damage.	A
EN	4	Potential device damage	A
VIN	5	Normal operation	D
GND	6	The device does not power up and there is no output voltage.	B
SW	7	Potential device damage	A
GND	8	The device does not power up and there is no output voltage.	B
VIN	9	Normal operation	D
PG	10	Potential device damage	A
MODE/SYNC	11	Normal operation and forced PWM operation	C
SDA	12	Potential device damage	A
SCL	13	Potential device damage	A
SYNC_OUT	14	Potential device damage	A
VSEL	15	Normal operation. Defines start-up voltage	C
FSEL	16	Normal operation. Defines switching frequency	C

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