Functional Safety Information

AMC1306M25-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the AMC1306M25-Q1 (SOIC package) to aid in a functional safety system design. Information provided are:

- Functional safety failure in time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

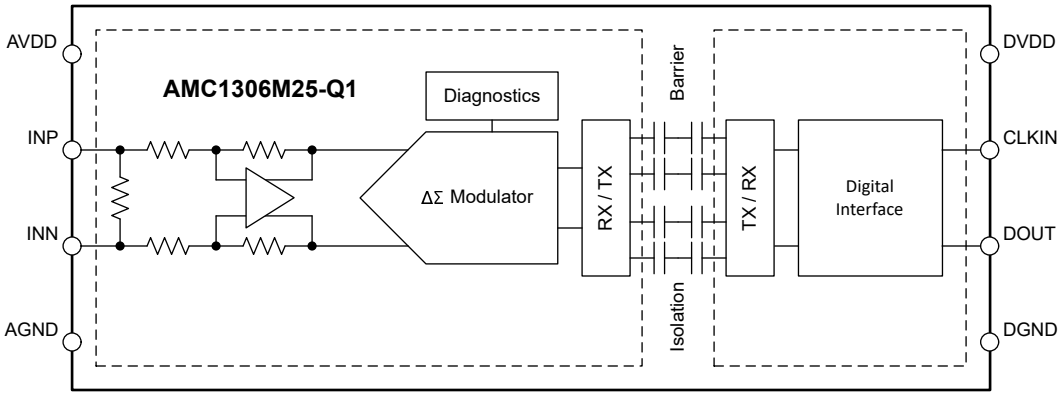

Figure 1-1. Functional Block Diagram

The AMC1306M25-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides functional safety failure in time (FIT) rates for the AMC1306M25-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	18
Die FIT rate	3
Package FIT rate	15

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 87 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	25 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the AMC1306M25-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity, and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures resulting from misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
DOUT stuck high or low	45%
Bitstream output out of specification (equivalent to gain error)	15%
Device behavior undetermined	15%
Reduced CMTI performance	10%
Bitstream output out of specification (equivalent to offset error)	10%
Bitstream output out of specification (increased noise)	5%

The FMD in Table 3-1 excludes short-circuit faults across the isolation barrier. Faults for short circuits across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a safety-separated extra low voltage (SELV) or protective extra low voltage (PELV) power supply is used, pollution degree 2 / OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the AMC1306M25-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality.
B	No device damage, but loss of functionality.
C	No device damage, but performance degradation.
D	No device damage, no impact to functionality or performance.

Figure 4-1 shows the AMC1306M25-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the AMC1306M25-Q1 data sheet.

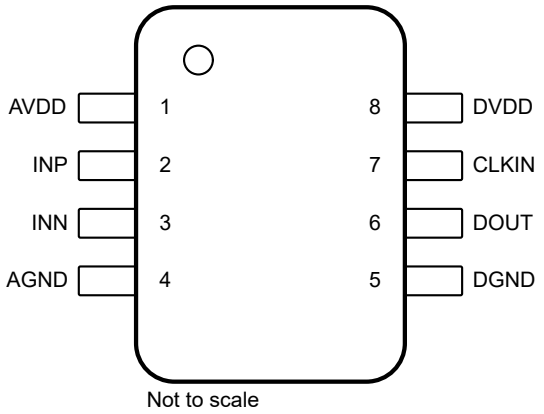

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Analog inputs are connected to a resistive signal source.
- Differential RC filter on INP or INN.
  Series resistors are sized to limit the input currents into INP or INN to <10 mA in all circumstances (for example, if the device is unpowered and the input signal is applied).
- CLKIN is driven with CMOS-compliant signal levels.
- DOUT load is only capacitive (no DC connection to DGND or DVDD).
- For pins on the primary side:
  Short-circuited to ground means short to AGND.
  Short-circuited to supply means short to AVDD.
- For pins on the secondary side:
  Short-circuited to ground means short to DGND.
  Short-circuited to supply means short to DVDD.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	Device primary side unpowered. Device outputs fail-safe state (see data sheet for details). Observe that the absolute maximum ratings for INP and INN of the device are met, otherwise device damage may be plausible.	A
INP	2	INP stuck low (AGND). Value of DOUT output bitstream proportional to voltage difference ($V_{AGND} – V_{INN}$).	B
INN	3	INN stuck low (AGND). Value of DOUT output bitstream proportional to voltage difference ($V_{INP} – V_{AGND}$).	B
AGND	4	No effect. Normal operation.	D
DGND	5	No effect. Normal operation.	D
DOUT	6	DOUT stuck low (DGND). No valid DOUT output bitstream. DOUT output bitstream looks like fail-safe output response (see data sheet for details). Excess current consumption from DVDD source when DOUT tries to drive high. Long-term damage plausible.	A
CLKIN	7	CLKIN stuck low (DGND). Device not functional because of missing clock input. DOUT stuck in same state (high or low) as when CLKIN stopped. No valid DOUT output bitstream.	B
DVDD	8	Device secondary side unpowered. DOUT pin is driven to DGND. No valid DOUT output bitstream. Observe that the absolute maximum ratings for CLKIN of the device are met, otherwise device damage may be plausible.	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	Device primary side unpowered. Device outputs fail-safe state (see data sheet for details). INP and INN have special ESD cells with blocking diodes and no direct connection to internal AVDD. The device does not power up if INP or INN is biased high. However, some input clamp damage can occur if the INP or INN input current exceeds the absolute maximum input current rating.	B
INP	2	INP undetermined. Value of DOUT output bitstream undetermined.	B
INN	3	INN undetermined. Value of DOUT output bitstream undetermined.	B
AGND	4	Device primary side unpowered. Device outputs fail-safe state (see data sheet for details).	B
DGND	5	Device secondary side periodically powered through ESD diode of the CLKIN pin when CLKIN is driven low. If the CLK driver can supply 8 mA of current then the device may function and produce a DOUT output bitstream. However, the logic high and low levels of DOUT are not met. Otherwise, the DOUT output bitstream is undetermined.	B
DOUT	6	DOUT undetermined. No valid DOUT output bitstream.	B
CLKIN	7	CLKIN floating. Device not functional because of missing clock input. DOUT stuck in same state (high or low) as when CLKIN stopped. No valid DOUT output bitstream.	B
DVDD	8	Device secondary side periodically powered through ESD diode of the CLKIN pin when CLKIN is driven high. If the CLK driver can supply 8 mA of current then the device may function and produce a valid DOUT output bitstream. However, the logic high and low levels of DOUT are not met. Otherwise, the DOUT output bitstream is undetermined.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	INP	INP stuck high (AVDD). Value of DOUT output bitstream proportional to voltage difference ($V_{AVDD} – V_{INN}$). Overrange or common-mode overvoltage detection is likely to trigger (see data sheet for more details).	B
INP	2	INN	INP shorted to INN, resulting in zero differential input voltage. Value of DOUT output bitstream at mid-scale (50% zeros, 50% ones).	B
INN	3	AGND	INN stuck low (AGND). Value of DOUT output bitstream proportional to voltage difference ($V_{INP} – V_{AGND}$).	B
AGND	4	DGND	Not considered. Corner pin.	D
DGND	5	DOUT	DOUT stuck low (DGND). No valid DOUT output bitstream. DOUT output bitstream looks like fail-safe output response (see data sheet for details). Excess current consumption from DVDD source when DOUT tries to drive high. Long-term damage plausible.	A
DOUT	6	CLKIN	DOUT output bit stream corrupted. Excess current consumption from DVDD source when DOUT tries to drive high, while CLKIN drives low and vice versa. Long-term damage plausible.	A
CLKIN	7	DVDD	CLKIN stuck high (DVDD). Device not functional because of missing clock input. DOUT stuck in same state (high or low) as when CLKIN stopped. No valid DOUT output bitstream.	B
DVDD	8	AVDD	Not considered. Corner pin.	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
AVDD	1	No effect. Normal operation.	D
INP	2	INP stuck high (AVDD). Value of DOUT output bitstream proportional to voltage difference ($V_{AVDD} – V_{INN}$). Overrange or common-mode overvoltage detection is likely to trigger (see data sheet for more details).	B
INN	3	INN stuck high (AVDD). Value of DOUT output bitstream proportional to voltage difference ($V_{INP} – V_{AVDD}$). Overrange or common-mode overvoltage detection is likely to trigger (see data sheet for more details).	B
AGND	4	Device primary side unpowered. Device outputs fail-safe state (see data sheet for details).	B
DGND	5	Device secondary side unpowered. DOUT pin is driven to DGND. No valid DOUT output bitstream. Observe that the absolute maximum ratings for CLKIN of the device are met, otherwise device damage may be plausible.	A
DOUT	6	DOUT stuck high (DVDD). No valid DOUT output bitstream. Excess current consumption from DVDD source when DOUT tries to drive low. Long-term damage plausible.	A
CLKIN	7	CLKIN stuck high (DVDD). Device not functional because of missing clock input. DOUT stuck in same state (high or low) as when CLKIN stopped. No valid DOUT output bitstream.	B
DVDD	8	No effect. Normal operation.	D

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