Functional Safety Information

TPS3760

Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for TPS3760 (DYY package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

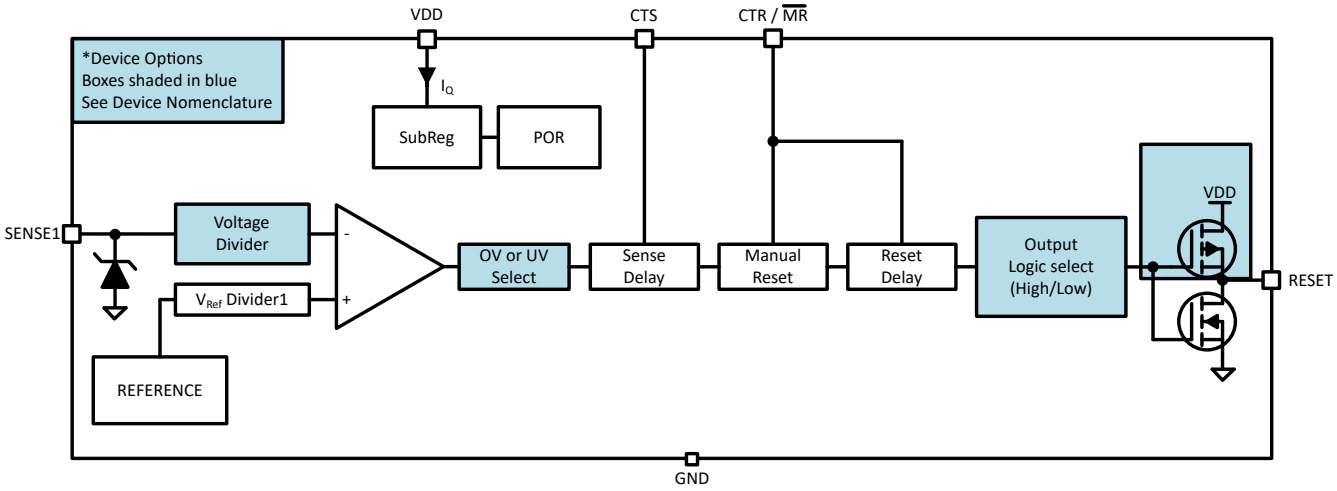

Figure 1-1. Functional Block Diagram

TPS3760 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS3760 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	7
Die FIT Rate	3
Package FIT Rate	4

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 364 µW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS3760 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
RESET / fails to trip	16%
RESET / false trip	16%
RESET / trip outside specification (voltage or time)	62%
RESET / delay outside specification	6%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS3760. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS3760 pin diagram. For a detailed description of the device pins please refer to *TPS3760* in the *Pin Configuration and Functions* section of the data sheet.

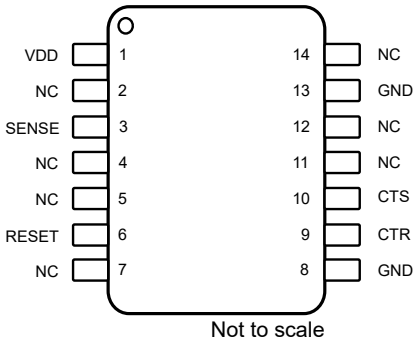

Figure 4-1. Pin Diagram DYY Package 14-Pin SOT-23

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- RESET are pictured as active low, some configurations ($\overline{\text{RESET}}$) will be active low. RESET in Figure 4-1 is shown as open-drain, some configurations will be push-pull. Refer to TPS3760 Pin Configuration and Functions section of the data sheet.
- At $V_{DD\ (MIN)} \leq VDD \leq V_{DD\ (MAX)}$, CTR = CTS = Open
- Output reset Pullup Resistor (R_{PULLUP}) = 10 kΩ, Output reset pullup voltage (V_{PULLUP} = 5.5 V, output reset load (C_{LOAD}) = 10 pF.
- Tables valid over the operating free-air temperature range of – 40°C to 125°C, unless otherwise noted.
- Typical values are at T_A = 25°C, VDD = 16 V, and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}) unless stated otherwise.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
VDD	1	VDD short to GND, Device has no power for normal operation	B
NC	2	Normal operation, Pin is not connected during normal operation	D
SENSE	3	Functionality affected, Voltage threshold will not be intended threshold	B
NC	4	Normal operation, Pin is not connected during normal operation	D
NC	5	Normal operation, Pin is not connected during normal operation	D
RESET	6	Functionality affected, Unreliable device output	A
NC	7	Normal operation, Pin is not connected during normal operation	D
GND	8	Normal operation	D
CTR	9	RESET will be asserted.	B
CTS	10	Normal operation, RESET will be asserted	B
NC	11	Normal operation, Pin is not connected during normal operation	D
NC	12	Normal operation, Pin is not connected during normal operation	D
GND	13	Normal operation	D
NC	14	Normal operation, Pin is not connected during normal operation	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
VDD	1	Device Unpowered	B
NC	2	Normal operation, Pin is not connected during normal operation	D
SENSE	3	Functionality affected, Voltage threshold will not be intended threshold	B
NC	4	Normal operation, Pin is not connected during normal operation	D
NC	5	Normal operation, Pin is not connected during normal operation	D
RESET	6	Functionality affected, Unreliable device output	A
NC	7	Normal operation, Pin is not connected during normal operation	D
GND	8	Device Unpowered	B
CTR	9	Normal operation	D
CTS	10	Normal operation	D
NC	11	Normal operation, Pin is not connected during normal operation	D
NC	12	Normal operation, Pin is not connected during normal operation	D
GND	13	Device Unpowered	B
NC	14	Normal operation, Pin is not connected during normal operation	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

PIN NAME	PIN NO.	SHORTED TO	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
VDD	1	NC	Normal operation	D
NC	2	SENSE	Normal operation	D
SENSE	3	NC	Normal operation	D
NC	4	NC	Normal operation	D
NC	5	RESET	Normal operation	D
RESET	6	NC	Functionality affected, Unreliable device output. NC is not connected during normal operation.	B
NC	7	GND	Normal operation	D
GND	8	CTR	Functionality affected, RESET is asserted	B
CTR	9	CTS	Functionality affected, Iq can increase	B
CTS	10	NC	Functionality affected, Iq can increase	B
NC	11	NC	Functionality affected, Iq can increase	C
NC	12	GND	Functionality affected, Iq can increase	C
GND	13	NC	Normal operation	D
NC	14	VDD	Normal operation	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

PIN NAME	PIN NO.	DESCRIPTION OF POTENTIAL FAILURE EFFECT(S)	FAILURE EFFECT CLASS
VDD	1	Normal operation	D
NC	2	Normal operation	D
SENSE	3	Functionality affected, Voltage threshold will not be intended threshold	B
NC	4	Normal operation	D
NC	5	Normal operation	D
RESET	6	Functionality affected, Can cause short from VDD to GND	A
NC	7	Functionality affected, Can cause short from VDD to GND	A
GND	8	VDD short to GND Fault	B
CTR	9	May damage device if VDD is greater than the pin's recommended operating condition	A
CTS	10	May damage device if VDD is greater than the pin's recommended operating condition	A
NC	11	May damage device if VDD is greater than the pin's recommended operating condition	A
NC	12	May damage device if VDD is greater than the pin's recommended operating condition	A
GND	13	VDD short to GND Fault	B
NC	14	Normal operation	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2022	*	Initial Release

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