Functional Safety Information

SN74HCS14-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for SN74HCS14-Q1 (BQA, D, DYY, and PW packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

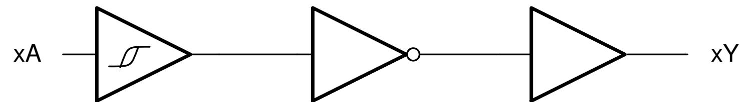

Figure 1-1. Functional Block Diagram

SN74HCS14-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

2.1 BQA, D, DYY, and PW Packages

This section provides Functional Safety Failure In Time (FIT) rates for BQA, D, DYY, and PW packages of SN74HCS14-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) - WQFN (BQA)	FIT (Failures Per 10^9 Hours) - SOIC (D)	FIT (Failures Per 10^9 Hours) - SOT (DYY)	FIT (Failures Per 10^9 Hours) - TSSOP (PW)
Total Component FIT Rate	8	18	8	11
Die FIT Rate	3	3	4	3
Package FIT Rate	5	15	4	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 100 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS Logic FCT, HC, LV, LVC, ALVC, VHC, and so forth	5 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74HCS14-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck-at fault	30%
Output open (HIZ)	25%
Output functional – out of specification timing or voltage	45%

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN74HCS14-Q1 (BQA, D, DYY, and PW packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V_{CC} (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 BQA, D, DYY, and PW Packages

Figure 4-2 shows the SN74HCS14-Q1 pin diagram for the BQA, D, DYY, and PW packages. For a detailed description of the device pins and their corresponding pin type, please refer to the *Pin Configuration and Functions* section in the SN74HCS14-Q1 data sheet. **Thermal Thermal Pad should be tied directly to GND plane to avoid potential failures that can cause excessive current.**

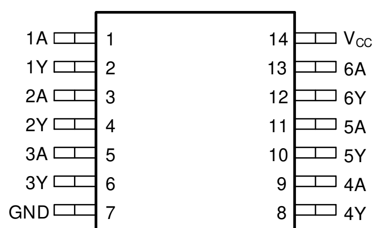

Figure 4-1. Pin Diagram (D, DYY, and PW) Packages

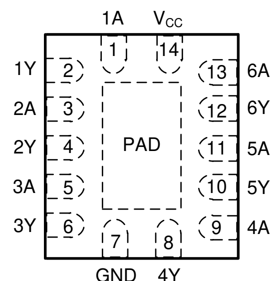

Figure 4-2. Pin Diagram (BQA) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A	1, 3, 5, 9, 11, 13	Input pin is forced to the low logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
GND	7	Normal operation.	D
Y	2, 4, 6, 8, 10, 12	Can cause excessive output current; output remains in the low output state independent of input states.	A
V_{CC}	14	Device is not powered. System level damage can occur in this scenario.	B
Thermal Pad(1)	—	Normal operation.	D

(1) BQA package only

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A	1, 3, 5, 9, 11, 13	Pin is floating, can change output state and cause excessive current from V_{CC} to GND. See Implications of Slow or Floating CMOS Inputs.	A

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Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
GND	7	Device is not powered.	B
Y	2, 4, 6, 8, 10, 12	Normal operation.	D
V_{CC}	14	Device is not powered.	B
Thermal Pad(1)	—	Normal operation.	D

(1) BQA package only

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
A	1, 3, 5, 9, 11, 13	A	Two inputs shorted together can cause a loss of functionality or damage to the device. Damage to the device can occur when the input voltage (V_I) is driven such that $V_{IL} < V_I < V_{IH}$.	A
A	1, 3, 5, 9, 11, 13	Y	Can cause loss of functionality or damage to the device. Damage to the device can occur due to feedback oscillation causing excessive current consumption.	A
A	1, 3, 5, 9, 11, 13	GND	Input pin is forced to the low logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
A	1, 3, 5, 9, 11, 13	Thermal Pad	Input pin is forced to the low logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
A	1, 3, 5, 9, 11, 13	V_{CC}	Input pin is forced to the high logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
Y	2, 4, 6, 8, 10, 12	GND	Can cause excessive output current; output remains in the low output state independent of input states.	A
Y	2, 4, 6, 8, 10, 12	Thermal Pad	Can cause excessive output current; output remains in the low output state independent of input states.	A
Y	2, 4, 6, 8, 10, 12	V_{CC}	Can cause excessive output current; output remains in the high output state independent of input states.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
A	1, 3, 5, 9, 11, 13	Input pin is forced to the high logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
GND	7	Device can not be powered because short is external to device. System level damage can occur in this scenario.	B
Y	2, 4, 6, 8, 10, 12	Can cause excessive output current; output remains in the high output state independent of input states.	A
V_{CC}	14	Normal operation.	D
Thermal Pad(1)	—	Device is not powered. System level damage can occur in this scenario.	B

(1) BQA package only

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2023	*	Initial Release

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