Functional Safety Information

SN74HCS20-Q1
Functional Safety FIT Rate, FMD and Pin FMA

Table of Contents

Trademarks

1 Overview

This document contains information for SN74HCS20-Q1 (D and PW packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

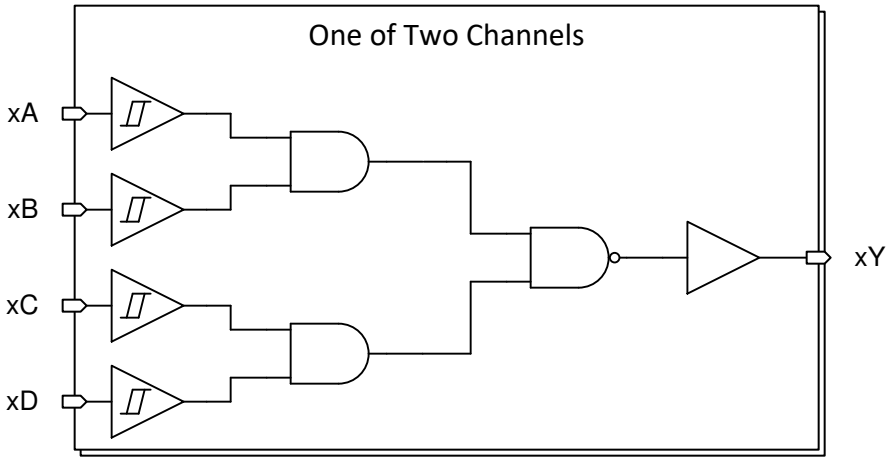

Figure 1-1. Functional Block Diagram

SN74HCS20-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 D and PW Packages

This section provides Functional Safety Failure In Time (FIT) rates for D and PW packages of SN74HCS20-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours) - TSSOP (PW)	FIT (Failures Per 10^9 Hours) - SOIC (D)
Total Component FIT Rate	10	17
Die FIT Rate	2	2
Package FIT Rate	8	15

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 25 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
3	CMOS Logic FCT, HC, LV, LVC, ALVC, VHC, and so forth	5 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74HCS20-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output stuck-at fault	30%
Output open (HIZ)	25%
Output functional – out of specification timing or voltage	45%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the SN74HCS20-Q1 (D and PW packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to V_{CC} (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

4.1 D and PW Packages

Pin Diagram (D and PW) Packages shows the SN74HCS20-Q1 pin diagram for the D and PW packages. For a detailed description of the device pins and their corresponding pin type, please refer to the *Pin Configuration and Functions* section in the SN74HCS20-Q1 data sheet.

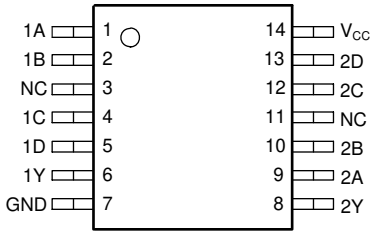

Figure 4-1. Pin Diagram (D and PW) Packages

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	3, 11	Normal operation.	D
A, B, C, D	1, 2, 4, 5, 9, 10, 12, 13	Input pin is forced to the low logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
GND	7	Normal operation.	D
Y	6, 8	Can cause excessive output current; output remains in the low output state independent of input states.	A
V_{CC}	14	Device is not powered. System level damage can occur in this scenario.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	3, 11	Normal operation.	D
A, B, C, D	1, 2, 4, 5, 9, 10, 12, 13	Pin is floating, can change output state and cause excessive current from V_{CC} to GND. See Implications of Slow or Floating CMOS Inputs.	A
GND	7	Device is not powered.	B
Y	6, 8	Normal operation.	D

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
V_{CC}	14	Device is not powered.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
NC	3, 11	A, B, C, D, Y, V_{CC}, GND, Thermal Pad	Normal operation.	D
A, B, C, D	1, 2, 4, 5, 9, 10, 12, 13	A, B, C, D	Two inputs shorted together can cause a loss of functionality or damage to the device. Damage to the device can occur when the input voltage (V_I) is driven such that $V_{IL} < V_I < V_{IH}$.	A
A, B, C, D	1, 2, 4, 5, 9, 10, 12, 13	Y	Can cause loss of functionality or damage to the device. Damage to the device can occur due to feedback oscillation causing excessive current consumption.	A
A, B, C, D	1, 2, 4, 5, 9, 10, 12, 13	GND	Input pin is forced to the low logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
A, B, C, D	1, 2, 4, 5, 9, 10, 12, 13	Thermal Pad	Input pin is forced to the low logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
A, B, C, D	1, 2, 4, 5, 9, 10, 12, 13	V_{CC}	Input pin is forced to the high logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
Y	6, 8	GND	Can cause excessive output current; output remains in the low output state independent of input states.	A
Y	6, 8	Thermal Pad	Can cause excessive output current; output remains in the low output state independent of input states.	A
Y	6, 8	V_{CC}	Can cause excessive output current; output remains in the high output state independent of input states.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_{CC}

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	3, 11	Normal operation.	D
A, B, C, D	1, 2, 4, 5, 9, 10, 12, 13	Input pin is forced to the high logic state. See *Device Function Table* in the device data sheet for details of how the failure affects functionality.	B
GND	7	Device is not powered. System level damage can occur in this scenario.	B
Y	6, 8	Can cause excessive output current; output remains in the high output state independent of input states.	A
V_{CC}	14	Normal operation.	D

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2023	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265