Functional Safety Information

SN74AXC1T45-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the SN74AXC1T45-Q1 (SC70 and SON packages) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

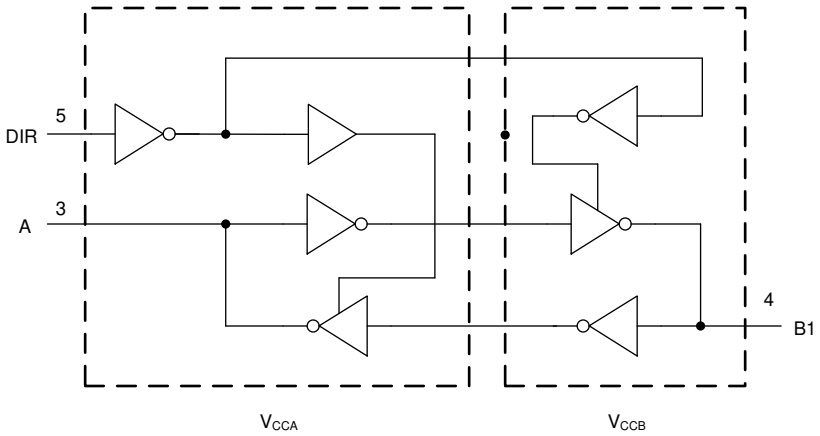

Figure 1-1. Functional Block Diagram

SN74AXC1T45-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SC70 Package

This section provides functional safety failure in time (FIT) rates for the SC70 package of the SN74AXC1T45-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	5
Die FIT rate	3
Package FIT rate	2

The failure rate and mission profile information in Table 2-1 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 60 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog, or mixed	8 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 SON Package

This section provides functional safety failure in time (FIT) rates for the SON package of the SN74AXC1T45-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	3
Package FIT rate	1

The failure rate and mission profile information in Table 2-3 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: motor control from table 11
- Power dissipation: 60 mW
- Climate type: world-wide table 8
- Package factor (lambda 3): table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS Logic	8 FIT	55°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for SN74AXC1T45-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Driver HIZ no output	22%
Output functional – out of specification timing or voltage	23%
Driver stuck at fault high	22%
Driver stuck at fault low	25%
Driver stuck at undetermined state	8%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a failure mode analysis (FMA) for the pins of the SN74AXC1T45-Q1 (SC70 and SON packages). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5 and Table 4-6)

Table 4-2 through Table 4-6 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Pin Diagram shows the SN74AXC1T45-Q1 pin diagram. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the SN74AXC1T45-Q1 data sheet.

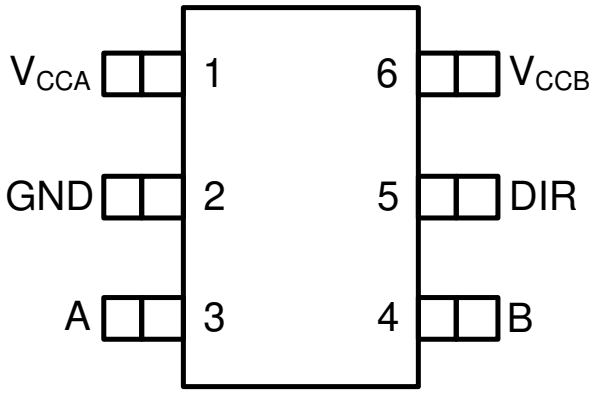

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VCCA (see Table 4-5)
- Pin short-circuited to VCCB (see Table 4-6)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	GND short to VCC, device will be bypassed; may cause system damage, but not device damage	B
GND	2	Normal Operation	D
A	3	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
B	4	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
DIR	5	Direction control will fix B --> A direction	B
VCCB	6	GND short to VCC, device will be bypassed - may cause system damage, but not device damage	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Device will not be powered	B
GND	2	Device will not be powered	B
A	3	If configured as output, normal operation. If configured as input, no damage, but output will not switch	B
B	4	If configured as output, normal operation. If configured as input, no damage, but output will not switch	B
DIR	5	Direction control will fix B --> A direction	B
VCCB	6	Device will not be powered	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	GND	GND short to VCC, device will be bypassed; may cause system damage, but not device damage	B
GND	2	A	If A is configured as an output then damage is possible. If configured as input, output will be fixed LOW	A
A	3	B	Both bits will have the same value always, but could have bus contention during transitions that may cause high current	A
B	4	DIR	If DIR is LOW, B will be an input and drive the output LOW. If DIR is HIGH, B will be an output and damage is possible based on state of A.	A
DIR	5	VCCB	If VCCB>VCCA, DIR will fix B --> A direction OR if VCCB<VCCA, input could be inappropriate logic level potentially causing damage	A
VCCB	6	VCCA	VCCB short to VCCA, device will be bypassed; may cause system damage, but not device damage	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VCCA

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	Normal Operation	D
GND	2	GND short to VCC, device will be bypassed; may cause system damage, but not device damage	B
A	3	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
B	4	If configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL not met	A
DIR	5	Direction control will fix A --> B direction	B
VCCB	6	VCCA short to VCCB, device will be bypassed; may cause system damage, but not device damage	B

Table 4-6. Pin FMA for Device Pins Short-Circuited to VCCB

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VCCA	1	VCCB short to VCCA, device will be bypassed; may cause system damage, but not device damage	B
GND	2	GND short to VCC, device will be bypassed; may cause system damage, but not device damage	B
A	3	If configured as an output then damage is possible. If configured as input, damage is possible if VIH/VIL not met	A
B	4	If configured as an output then damage is possible. If configured as input, no damage, but output will not switch	A
DIR	5	If VCCB>VCCA, DIR will fix B --> A direction OR if VCCB is less than VCCA, input could be inappropriate logic level potentially causing damage	A
VCCB	6	Normal Operation	D

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265