Application Report
SLLA343 – October 2013

SN65DSI86 and SN65DSI96 Hardware Implementation Guide

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ABSTRACT

This document includes guidelines and recommendations for implementing SN65DSI86 or SN65DSI96 in system hardware. These recommendations are only guidelines and it is the designer's responsibility to consider all system characteristics and requirements. Refer to the datasheet (SLLSEH2) for technical details such as device operation, terminal description, and so forth.

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1 Overview

1.1 What are SN65DSI86 and SN65DSI96?

The SN65DSI86 and SN65DSI96 devices will be referred to as SN65DSIX6 in this document. SN65DSIX6 is an MIPI DSI-to-eDP bridge device that supports video modes in forward direction. The SN65DSIX6 is primarily targeted for portable applications such as tablets and smart phones that utilize the MIPI DSI video format. The SN65DSIX6 can be used between a GPU with DSI output and a video panel with DisplayPort inputs.

Both devices share the same pin out and package.

Table 1 presents a summary of the feature sets on these devices

Table 1. SN65DSIX6 Features Summary

Part Name	Description
SN65DSI86	Dual Channel DSI to 4 eDP lanes
SN65DSI96	Dual Channel DSI to 4 eDP lane with Assertive Display Technology

Note: Each DSI channel has 4 DSI data lanes and 1 CLK lane.

2 HW Implementation Guidelines

2.1 Power Supplies (V_{CC}, V_{CCA}, V_{CCIO}, V_{PLL})

2.1.1 V_{CC} Supply

The 1.2-V V_{CC} supply feeds the digital core for the SN65DSIX6. These supply pins should be connected to a power plane and each pin should have a 100-nF decoupling capacitor.

2.1.2 V_{CCA} supply

The 1.2-V V_{CCA} supply feeds the analog circuits for the DSI and DisplayPort interface. These supply pins should be connected to a power plane and each pin should have a 100-nF or 10-nF decoupling capacitor.

2.1.3 V_{PLL} Supply

The 1.8-V V_{PLL} supply provides power to the DisplayPort PLL. For optimal performance, it is critical this pin is well filtered. A 1-µF, 100-nF, and 10-nF decoupling capacitor is recommended.

2.1.4 V_{CCIO} Supply

The 1.8-V V_{CCIO} supply provides power to the LVCOM 1.8-V I/Os (GPIO[4:1], ADDR, and so forth). Using a 100-nF capacitor on each V_{CCIO} pin is recommended.

2.2 MIPI DSI Interface

2.2.1 DSI Critical Route Rules

1. DA*P/N and DB*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
2. Keep away from other high-speed signals.
3. Keep lengths to within 5 mils of each other.
4. Length matching should be near the location of mismatch. Refer to Figure 4 for an example.
5. Each pair should be separated at least by 3 times the signal trace width.
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135º. This will minimize any length mismatch caused by the bends and therefore minimize the impact bends have on EMI.
7. Route all differential pairs on the same layer.
8. The number of VIAS should be kept to a minimum. Keeping the VIAS count to 2 or less is recommended.
9. Keep traces on layers adjacent to the ground plane.
10. Do not route differential pairs over any plane split.
11. Adding test points will cause impedance discontinuity, therefore, negatively impacting signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.
12. The maximum trace length over FR4 between SN65DSIX6 and the GPU is 25 – 30 cm.

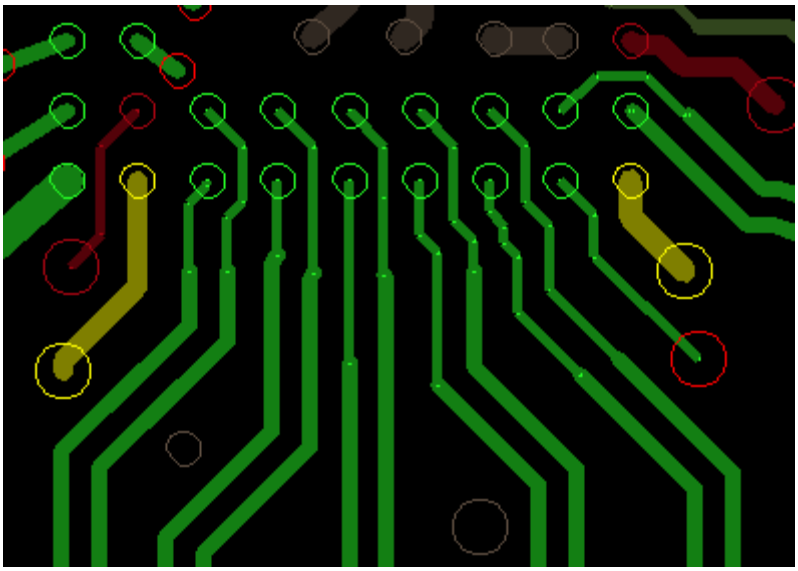


Figure 1. DSI Channel Routing Example

2.2.2 Unused DSI Channels or lanes

Leave unused DSI input terminals (DA*N/P, DB*N/P) unconnected or driven to LP11 state.

2.3 DisplayPort Interface

The SN65DSIX6 is compliant to DisplayPort 1.2a and eDP 1.4 and supports up to four lanes at data rates up to 5.4 Gbps (HBR2).

2.3.1 Main Link

2.3.1.1 AC Coupling Capacitors

All physical DisplayPort pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort Sink as depicted in Figure 2. It is recommended these capacitors are placed close to the eDP receptacle. The AC coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.

2.3.1.2 Lane Assignment Feature

The SN65DSIX6 has four physical DisplayPort lanes and each physical lane can be assigned to one specific logical lane. By default, physical lanes 0 thru 3 are mapped to logical lanes 0 thru 3, as depicted in Figure 2. When routing between the SN65DSIX6 and a non-standard eDP receptacle, this Lane Assign feature, along with polarity inversion, can greatly ease routing. By reprogramming the lane assignments, trace crossing on PCB can be eliminated and layer count may be reduced. Figure 3 shows an example of the logical lane to physical lane assignments to interface to a non-standard eDP receptacle.

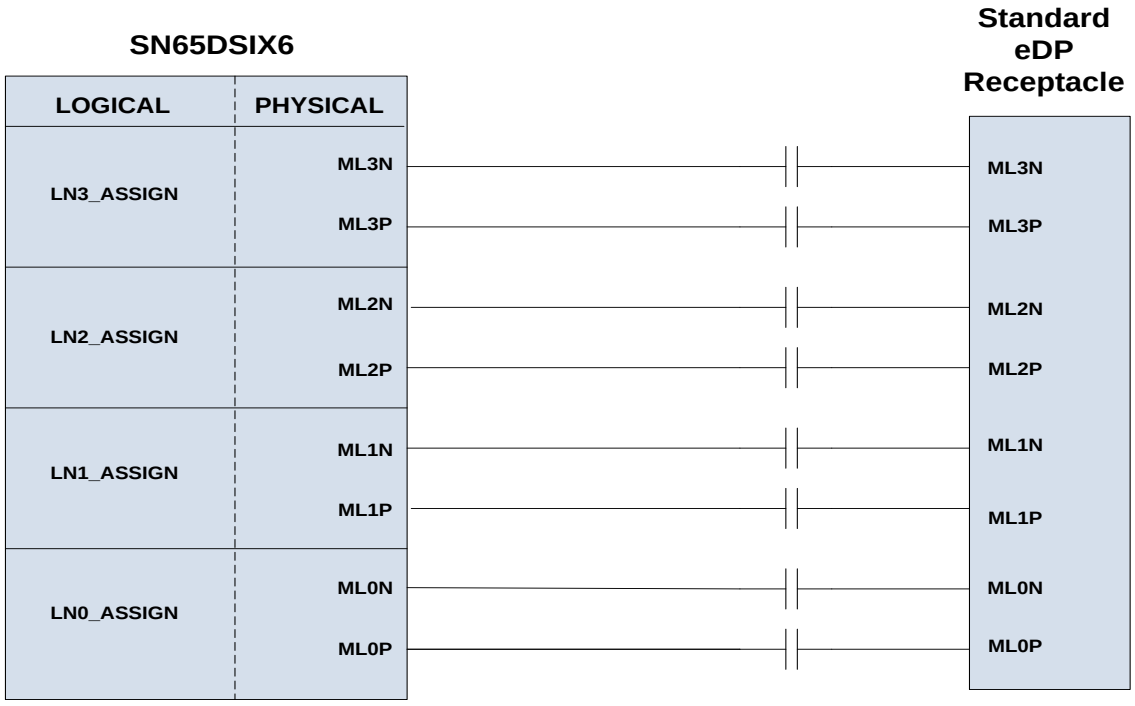


Figure 2. Default Configuration Lane Assignment Example

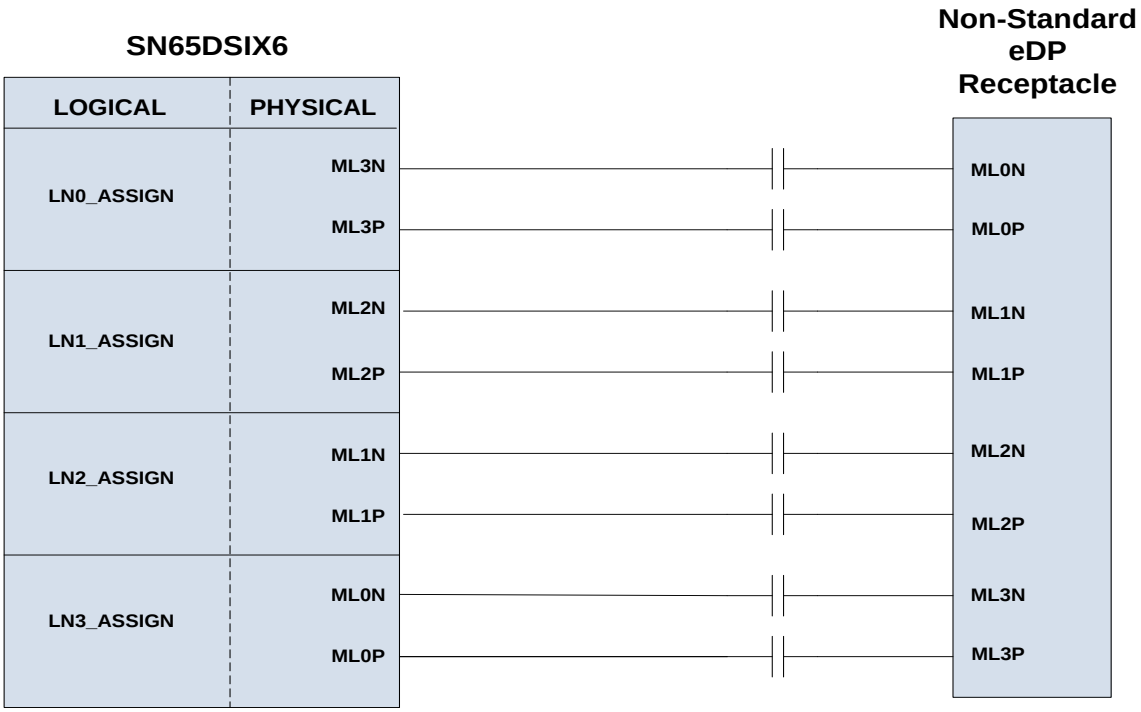


Figure 3. Custom Lane Assignment Example

2.3.1.3 Polarity Inversion Feature

The SN65DSIX6 provides the ability to swap the polarity of any DisplayPort lane. By default, the polarity of each lane is not inverted but by setting the appropriate MLx_POLR bit, the polarity of that specific physical lane will be inverted. This feature is very useful in eliminating crossing within a pair when routing traces across a PCB.

2.3.1.4 Main Link Critical Routes Rules

1. ML*P/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).
2. Keep away from other high-speed signals.
3. Intra-pair skew should be kept as small as possible. It is recommended to keep lengths to within 5 mils of each other.
4. Length matching should be near the location of mismatch. Refer to Figure 4 for an example.
5. Each pair should be separated by at least 3 times the signal trace width.
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135º. This will minimize any length mismatch caused by the bends, therefore, minimizing the impact bends have on EMI.
7. Route all differential pairs on the same layer.
8. The number of VIAS should be kept to a minimum. Keeping the VIAS count to 2 or less is recommended.
9. Keep traces on layers adjacent to the ground plane.
10. Do not route differential pairs over any plane split.
11. Adding test points will cause impedance discontinuity, therefore, negatively impacting signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.
12. The maximum trace length over FR4 between SN65DSIX6 and the eDP receptacle is 4 inches for data rates ≤ HBR (2.7 Gbps) and 2 inches for HBR2 (5.4 Gbps).

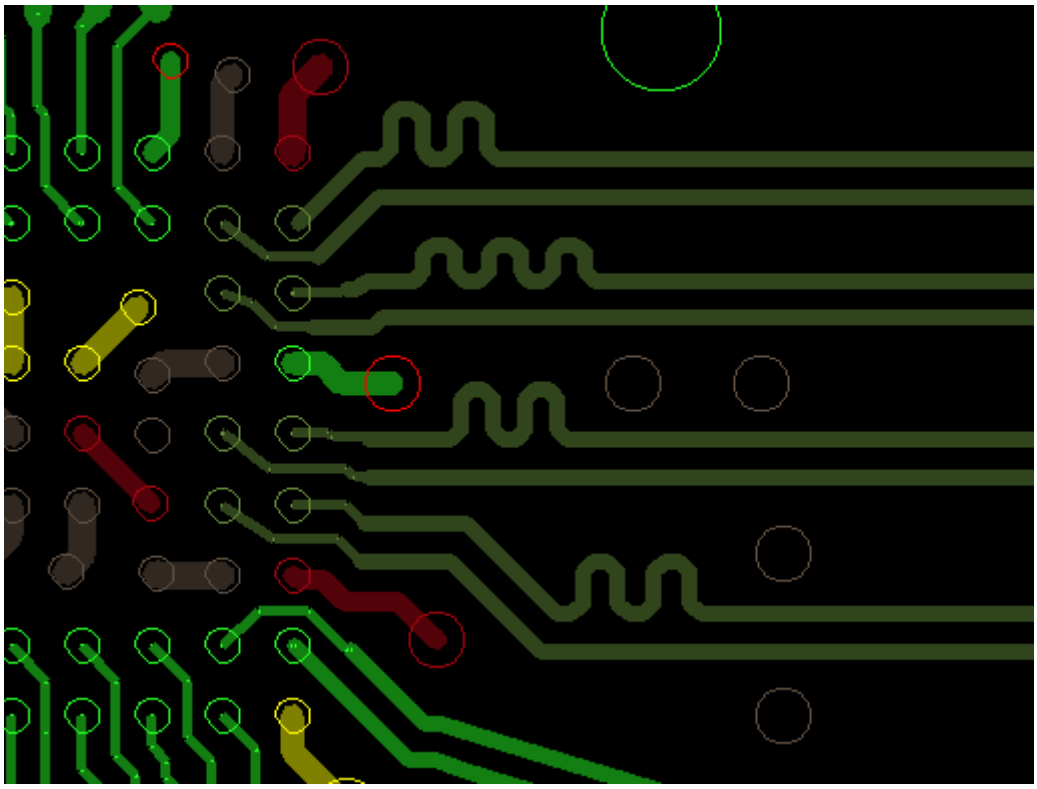


Figure 4. DisplayPort Main Link Routing Example

2.3.1.5 Unused DisplayPort Lanes

Leave unused DisplayPort terminals unconnected.

2.3.2 AUX

The SN65DSIX6 supports a Manchester-II encoded 1-Mbps AUX interface. FAUX (Fast AUX) is not supported.

2.3.2.1 AUX Implementation

AUXP/N pins require AC coupling capacitors between the SN65DSIX6 and the DisplayPort sink. Place these capacitors close to the eDP receptacle. The AC-coupling capacitor must be in the range of 75 nF to 200 nF. A value of 100 nF is recommended. A package size of 0201 is recommended but a 0402 is acceptable.

Source detection pull-up and pull-down resistors are optional. Some DisplayPort sinks will require source detection resistors while others will not.

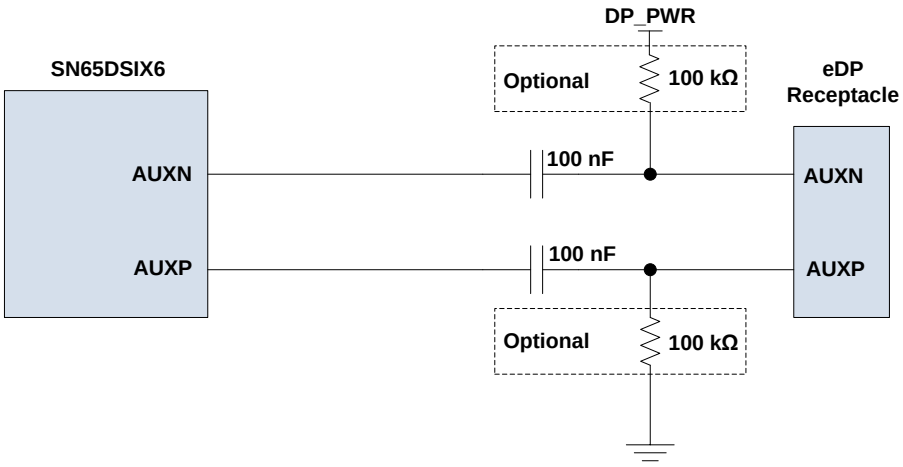


Figure 5. AUX Implementation

2.3.2.2 AUX Routing Rules

AUXP/N pairs should be routed with controlled 100-Ω differential impedance (±20%) or 50-Ω single-ended impedance (±15%).

2.3.3 HPD

The HPD I/O cell has an internal 60-kΩ pull-down resistor. The HPD pin requires a series external 51-kΩ 1% resistor as depicted in Figure 6. According to the VESA Embedded DisplayPort standard, use of HPD is optional for a DisplayPort transmitter. If the system designer chooses to not use HPD, then software must disable HPD by setting the HPD_DISABLE bit.

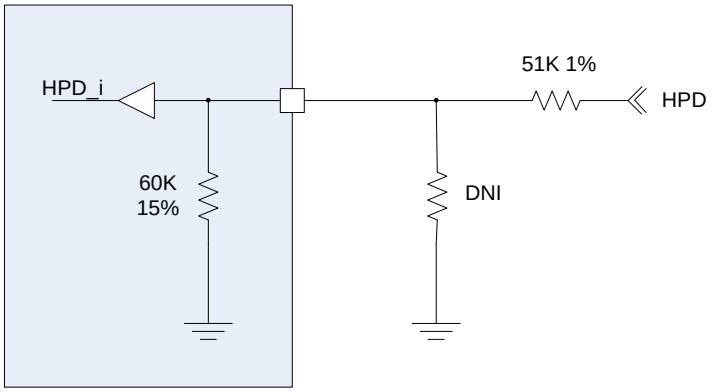


Figure 6. HPD Implementation

2.4 REFCLK

The SN65DSIX6 supports the following frequencies: 12 MHz, 19.2 Mhz, 26 MHz, 27 MHz, and 38.4 MHz. The REFCLK frequency must be specified by either configuration of GPIO[3:1] pins at rising edge of EN or through setting the appropriate value of the REFCLK_FREQ field in the configuration registers.

A series resistor is recommended near the RECLK source to reduce EMI. If possible, bury the REFCLK trace in the inner layer or minimize the trace length from the REFCLK terminal to CLK source by placing the source near the SN65DSIX6 REFCLK terminal.

When DSI_CLKA is used instead of REFCLK for the DisplayPort PLL, then the REFCLK pin must be tied or pulled down to GND.

2.5 RESET Implementation

The SN65DSIX6 is reset by controlling the EN terminal. The reset implementation defined in the datasheet should be followed for correct operation of the device after the reset.

2.6 I^2C

The I^2C interface (SDA and SCL pins) requires external pull-up resistors to V_{CCIO} for proper operation. If the I^2C interface is not used, then it should be pulled-down or tied directly to GND.

2.7 ADDR

The ADDR determines the least significant bit of the I^2C ADDR for the SN65DSIX6. This bit should be pulled high or low through a resistor depending on the I^2C address the system chooses to use for the SN65DSIX6. When this pin is pulled low, the device address is 0x2C. When this pin is pulled high, the device address is 0x2D.

IMPORTANT:

When it is pulled high, ADDR must be tied to the device V_{CCIO} such that this pin does not remain high when the device power is removed.

2.8 GPIOS

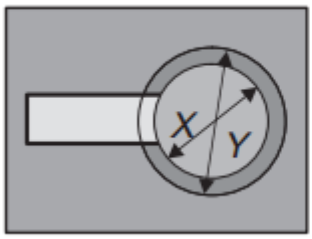
The GPIO[4:1] are used for various purposes. Please refer to the SN65DSIX6 datasheet for functional details of each GPIO. The GPIO[4:1] do not have any internal pull-up or pull-down resistors. When a GPIO is pulled-up, it should be pulled-up to the V_{CCIO} supply. Unused GPIOs should be pulled-down or tied to GND.

2.9 TEST Pins

TEST1, TEST2 and TEST3 are reserved pins and are intended for Texas Instruments use only. TEST1 should be left unconnected or tied to GND. TEST2 should be left unconnected or tied to GND. TEST2 must be pulled up to V_{CCIO} when performing DisplayPort compliance testing. TEST3 should be left unconnected or tied to GND through a 0.1-µF capacitor.

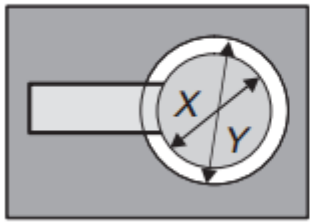
2.10 Land Pattern Configuration

The SN65DSIX6 package has a ball pitch of 0.5 mm. Follow the solder-mask defined land and non-solder mask defined land for a 0.5-mm ball pitch detailed in Figure 7.



Solder-Mask-Defined Land

Ball Pitch	X DIA.	Y DIA.	Stencil Th	Stencil DIA.
0.5 mm	0.28 mm	0.38 mm	120 µm	0.25–0.30 mm
0.8 mm	0.38 mm	0.48 mm	150 µm	0.35–0.40 mm
1.0 mm	0.45 mm	0.55 mm	150 µm	0.45–0.50 mm



Non-Solder-Mask-Defined Land

Ball Pitch	X DIA.	Y DIA.	Stencil Th	Stencil DIA.
0.5 mm	0.25 mm	0.30 mm	120 µm	0.25–0.30 mm
0.8 mm	0.35 mm	0.50 mm	150 µm	0.35–0.40 mm
1.0 mm	0.40 mm	0.55 mm	150 µm	0.45–0.50 mm

Figure 7. Recommended Land Pattern Configurations

3 References

SN65DSIX6 Datasheet (SLLSEH2).

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