TRF7964A Silicon Errata

This document describes the known exceptions to the functional specifications for the device.

Contents

1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all devices. Each commercial family member has one of two prefixes: XTRF or TRF (for example, TRF7964A).

These prefixes represent evolutionary stages of product development from engineering prototypes (XTRF) through fully qualified production devices or tools (TRF).

Device development evolutionary flow of the TRF7964A:

XTRF — Experimental device that is not necessarily representative of the final device's electrical specifications.

TRF — Fully qualified production device.

XTRF devices are shipped against the following disclaimer:

"Developmental products are intended for internal evaluation purposes.

TRF devices have been fully characterized, and the quality and reliability of the device have been fully demonstrated. TI's standard warranty applies.

Predictions show that prototype devices (XTRF) have a greater failure rate than the standard production devices. Texas Instruments recommends not to use these devices in any production system."

2 Revision Identification

Figure 1 provides an example of the device marking. The device revision can be determined by the symbols marked on the top of the device.

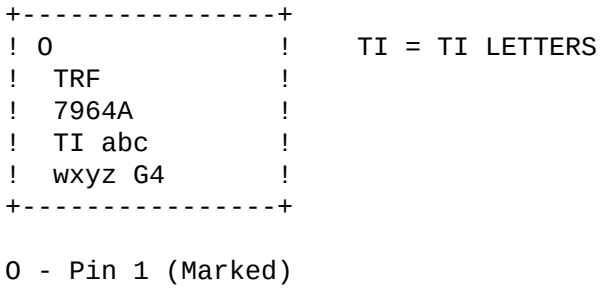

Figure 1. Package Markings

3 Known Design Exceptions to Functional Specifications

Device#B01 *In Reader/Writer communication mode at 106 kbps, 1-etu duration outside ISO 14443 specification.*

Expected Behavior The bit duration (1 etu) as defined by ISO14443A/NFC-A air interface is 9.44 µs (±0.5%).

Issue The device fails this criterion. Measuring this value (for example, for EMVCO compliance testing), the 1 etu is approximately ≥9.587 µs and, hence, outside the specification limits.

Condition The device operates as ISO14443A/NFC-A reader/writer and as NFC-A Peer to Peer (P2P) Initiator.

Implications The device fully supports ISO14443A communication. The device fail the EMVCO compliance testing as the 1-etu value is outside given range.

Workaround There is no workaround identified

Device#B02 *FIFO not accessible in SPI without SS mode.*

Expected Behavior FIFO is accessible in all SPI modes

Issue The TRF7964A was supposed to have three methods of communication with a microcontroller (MCU): Parallel Mode, Serial Peripheral Interface (SPI) with Slave Select (SS), and SPI without SS.

In the SPI operation mode without SS, the TRF7964A registers can be read from and written to; however, the FIFO is not accessible.

Condition SPI operation mode without SS

Implications FIFO is not accessible.

Workaround The following workarounds exist:

1. Use SPI with SS.
2. Use Direct Mode 1.
   This requires using I/O_5, MOD pin, and dedicated MCU firmware for data encode and decode.
3. Use Direct Mode 0.
   This requires using MOD pin and dedicated MCU firmware.

Device#B04 *Parity error indication in IRQ status register (0x0C) Bit 3*

Expected Behavior	When parity error is sent back as part of an ISO14443A or NFC-A transponder response, Bit 3 in register 0x0Ch should be set.
Issue	The device is supposed to indicate a parity error by setting bit 3 of the IRQ status register when operating as a reader/writer or initiator. Instead, a parity error is indicated as a CRC error (bit 4 in the IRQ status register 0x0Ch).
Condition	The behavior is not dependent on any particular device condition.
Implications	No parity error indication during EMVCoL1 Digital or NFC Wave1 compliance testing.
Workaround	Use the device in Direct Mode 0. This requires using the MOD pin and dedicated MCU firmware.

Device#B05 *RX FIFO overflow error indication in FIFO Status register (0x1C) Bit 7*

Expected Behavior	When the FIFO has more than 127 bytes stored in it, Bit 7 in register 0x1C should be set.
Issue	The device is supposed to indicate a FIFO overflow error by setting bit 7 of the FIFO status register when the FIFO is filled with more than 127 bytes when receiving a message from another transceiver. If the FIFO is read out by from the MCU while the FIFO is being filled with another transceiver's command which is larger than 127 bytes, Bit 7 of the FIFO Status Register might be set.
Condition	The TRF7964A's FIFO is being written with a command with size larger than 127 bytes, from another transceiver. The behavior is not dependent on any particular physical condition.
Implications	Erroneous software behavior not receiving commands completely.
Workaround	The firmware must mask Bit 7, when reading the FIFO Status Register (0x1C) and validate the command size in firmware based on the specification used.

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