bq3060 Gas Gauge Circuit Design

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ABSTRACT

Components in the bq3060 reference design are explained in this application report. Design analysis and suggested tradeoffs are provided, where appropriate.

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1 Introduction

The bq3060 Advanced Gas Gauge has approximately 59 components in the reference design for a two-thermistor, four-cell application. An additional six components are required if external cell balancing is used. For clarity, the device is divided into the following classifications: High-Current Path, Gas Gauge Circuit, Secondary-Current Protection and Cell-Balancing Circuit, and Secondary-Voltage Protection.

The discussion is based on the four-cell reference design for the bq3060. The complete schematic appears on the last page of this document.

2 High-Current Path

The high-current path begins at the PACK+ terminal of the battery pack. As charge current travels through the pack, it finds its way through protection FETs, a chemical fuse, the lithium-ion cells and cell connections, the sense resistor, and then returns to the PACK– terminal (see the reference design schematic at the end of this document). In addition, some components are placed across the PACK+ and PACK– terminals to reduce effects from electrostatic discharge.

2.1 Protection FETs

The P-channel charge and discharge FETs must be selected for a given application. Most portable battery applications are a good match for the Si4435DY or equivalent. The P-channel precharge FET can usually be implemented with a smaller, less expensive device depending on the desired amount of precharge current.

The Fairchild Si4435DY is an –8.8-A, –30-V device with Rds(on) of 20 mΩ when the gate drive voltage is 10 V.

If a precharge FET is used, R23 is calculated to limit the precharge current to the desired rate. Be sure to account for the power dissipation of the series resistor. The precharge current is limited to (Vcharger – Vbat)/R38 and maximum power dissipation is $(\text{Vcharger} - \text{Vbat})^2/\text{R23}$.

The gates of all protection FETs are pulled to the source with a high-value resistor between gate and source to ensure that they are turned off if the gate drive is open.

Capacitors C16 and C18 help to protect the FETs during an ESD event. The use of two devices ensures normal operation if one of them becomes shorted. In order to have good ESD protection, the copper trace inductance of the capacitor leads must be designed to be as short and wide as possible. Ensure that the voltage rating of both C16 and C18 are adequate to hold off the applied voltage if one of the capacitors becomes shorted.

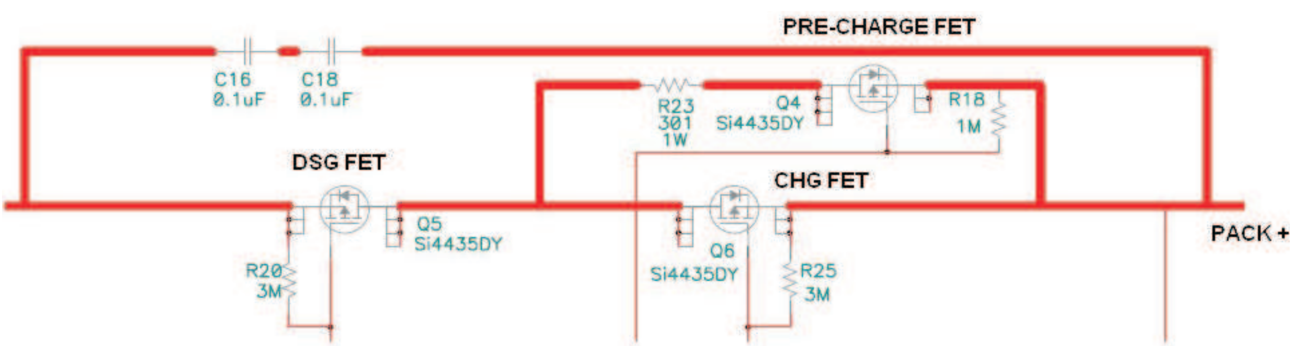


Figure 1. Protection FETs

2.2 Chemical Fuse

The chemical fuse (Sony Chemical, Uchihashi, etc.) is ignited under command from either the bq29412 secondary voltage protection IC or from the FUSE pin of the gas gauge. Either of these events applies a positive voltage to the gate of Q3 in Figure 2, which then sinks current from the third terminal of the fuse, causing it to ignite and open permanently.

It is important to carefully review the fuse specifications and match the required ignition current to that available from the N-channel FET. Ensure that the proper voltage, current, and Rds(on) ratings are used for this device. The fuse control circuit is discussed in detail in Section 3.5.

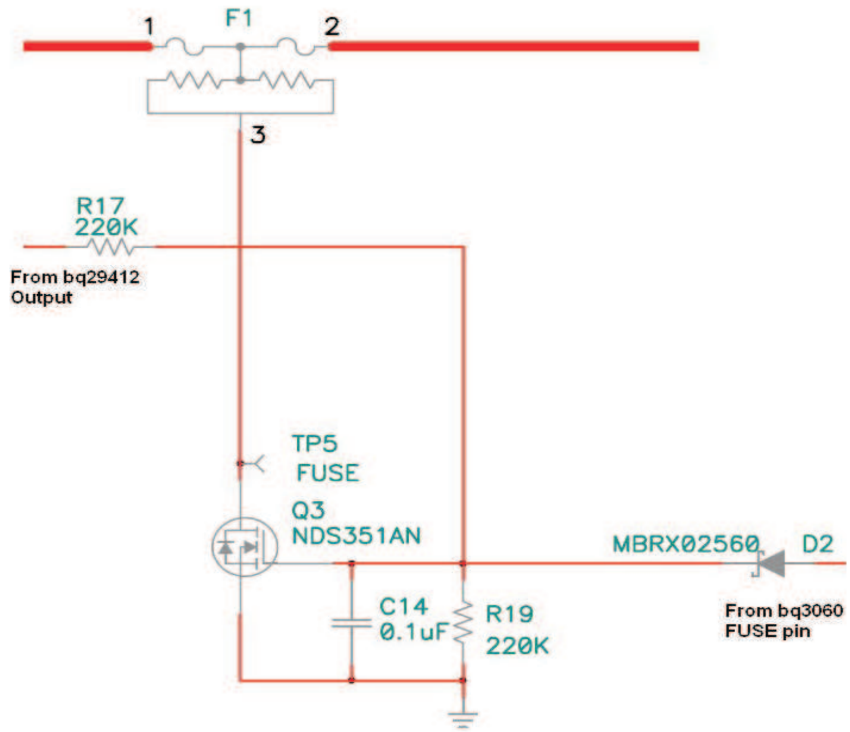


Figure 2. Chemical Fuse

2.3 Lithium-Ion Cell Connections

The important thing to remember about the cell connections is that high current flows through the top and bottom connections, and therefore the voltage sense leads at these points must be made with a Kelvin connection to avoid any errors due to a drop in the high-current copper trace. The location marked 4P in Figure 3 indicates the Kelvin connection of the most positive battery node. The connection marked 1N is equally important. Note that the VC5 pin (a ground reference for cell voltage measurement), which is presented in the older generation devices, has been removed in bq3060. Hence, the single-point connection at 1N to the low-current ground is needed in order to avoid undesired voltage drop through long traces while the gas gauge is measuring the bottom cell voltage.

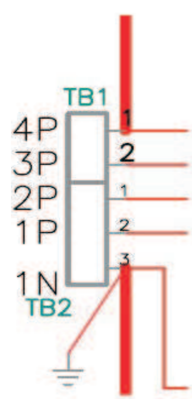


Figure 3. Lithium Ion Cell Connections

2.4 Sense Resistor

As with the cell connections, the quality of the Kelvin connections at the sense resistor is critical. The sense resistor must have a temperature coefficient no greater than 75 ppm in order to minimize current measurement drift with temperature. Choose the value of the sense resistor to correspond to the available overcurrent and short-circuit ranges of the bq3060. (See relevant tables in the data sheet.) Select the smallest value possible in order to minimize the negative voltage generated on the bq3060 pin 19 (VSS) node during a short circuit. This pin has an absolute minimum of –0.3 V. For a pack with two parallel cylindrical cells, 10 mΩ is generally ideal . Parallel resistors can be used as long as good Kelvin sensing is ensured.

Note that the ground scheme of bq3060 is different than the older generation devices. In previous devices, the device ground (or low current ground) is connected to the SRN side of the Rsense resistor pad. The bq3060, however, connects the low-current ground on the SRP side of the Rsense resistor pad, close to the battery 1N terminal (see Section 2.3). This is because the bq3060 has one less VC pin (a ground reference pin VC5) compared to the previous devices. The pin was removed and was internally combined to SRP.

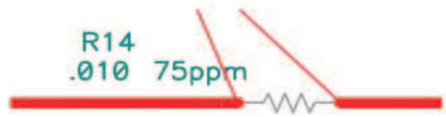


Figure 4. Sense Resistor

2.5 ESD Mitigation

A pair of series 0.1-µF ceramic capacitors is placed across the PACK+ and PACK– terminals to help in the mitigation of external electrostatic discharges. The two devices in series ensure continued operation of the pack if one of the capacitors becomes shorted.

Optionally, a tranzorb such as the SMBJ2A can be placed across the terminals to further improve ESD immunity.

3 Gas Gauge Circuit

The Gas Gauge Circuit includes the bq3060 and its peripheral components. These components are divided into the following groups: Differential Low-Pass Filter, Power Supply Decoupling/RBI/, System Present, SMBus Communication, and FUSE circuit.

3.1 Differential Low-Pass Filter

As shown in Figure 5, a differential filter must precede the current sense inputs of the gas gauge. This filter eliminates the effect of unwanted digital noise, which can cause offset in the measured current. Even the best differential amplifier has less common-mode rejection at high frequencies. Without a filter, the amplifier input stage may rectify a strong RF signal, which then may appear as a dc offset error.

Five percent tolerance of the components is adequate because capacitor C15 shunts C12/C13 and reduces ac common mode arising from component mismatch. It is important to locate C15 as close as possible to the gas gauge pins. The other components also must be relatively close to the IC. The ground connection of C12 and C13 must be close to the IC. It is also proven to reduce offset and noise error by maintaining a symmetrical placement pattern and adding ground shielding for the differential filter network.

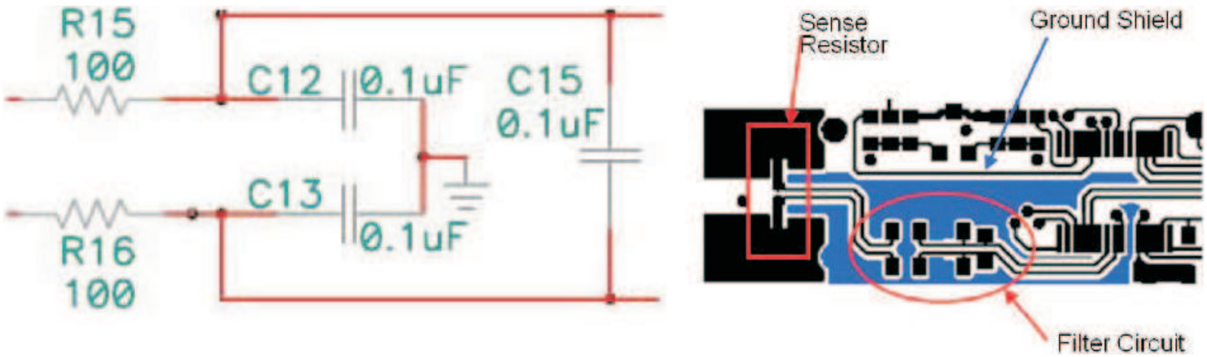


Figure 5. Differential Filter

3.2 *Power Supply Decoupling and RBI*

Power supply decoupling is important for optimal operation of the bq3060 advanced gas gauges. The low-dropout regulator within bq3060 is also the main power source for most of its internal circuits. As shown in Figure 6, a single 0.1-µF ceramic decoupling capacitor from REG27 to V_{SS} must be placed adjacent to the IC pins.

The RBI pin is used to supply backup RAM voltage during brief transient power outages. The partial reset mechanism makes use of the RAM to restore the critical CPU registers following a temporary loss of power. A standard 0.1-µF ceramic capacitor is connected from the RBI pin to ground as shown in Figure 6.

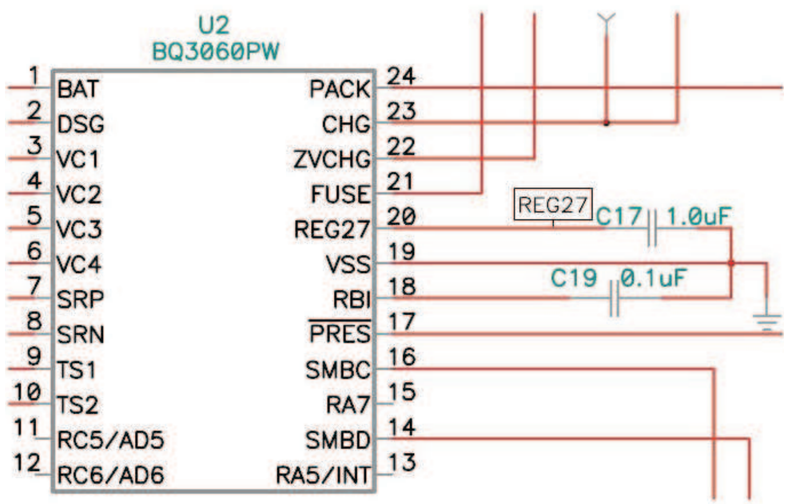


Figure 6. Power Supply Decoupling

3.3 *System Present*

The System Present signal is used to inform the gas gauge whether the pack is installed into or removed from the system. In the host system, this pin is grounded. The PRES pin of the bq3060 is occasionally sampled to test for system present. To save power, an internal pullup is provided by the gas gauge during a brief 4-µs sampling pulse once per second.

Because the System Present signal is part of the pack connector interface to the outside world, it must be protected from external electrostatic discharge events. An integrated ESD protection on the PRES device pin reduces the external protection requirement to just R30 for 8-kV ESD contact rating. However, if it is possible that the System Present signal may short to PACK+, then R32 and D4 must be included for high-voltage protection.

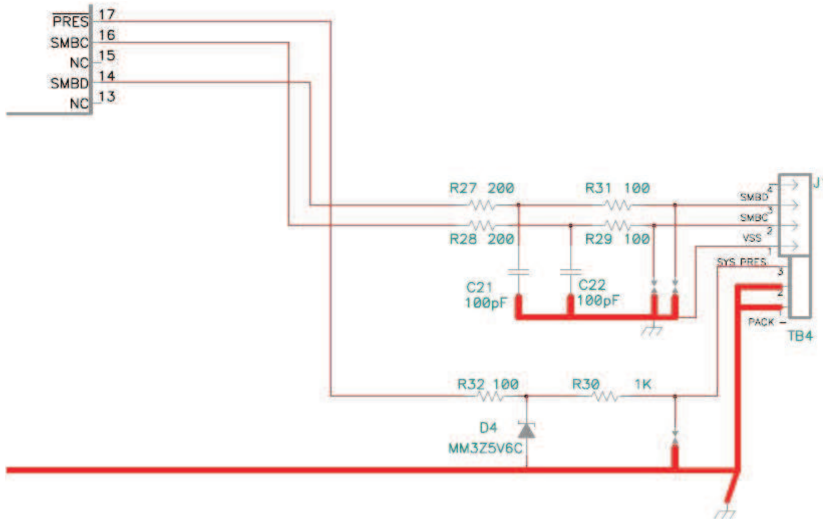


Figure 7. System Present ESD and Short Protection

3.4 SMBus Communication

Similar to the System Present pin, the SMBus clock and data pins have integrated high-voltage ESD protection circuit that reduce the need for external Zener diode protection. When using the circuit shown in Figure 8, the communication lines can withstand an 8-kV (contact) ESD strike. Note that C21 and C22 are selected with a 100-pF value in order to meet the SMBus specifications. If it is desirable to provide increased protection with a larger input resistor and/or Zener diode, carefully investigate the signal quality of the SMBus signals under worst-case communication conditions.

Both the SMbus clock and data lines have internal pulldown. When the gas gauge senses that both lines are low (such as during removal of the pack), the device performs auto offset calibration and then goes into sleep mode to conserve power.

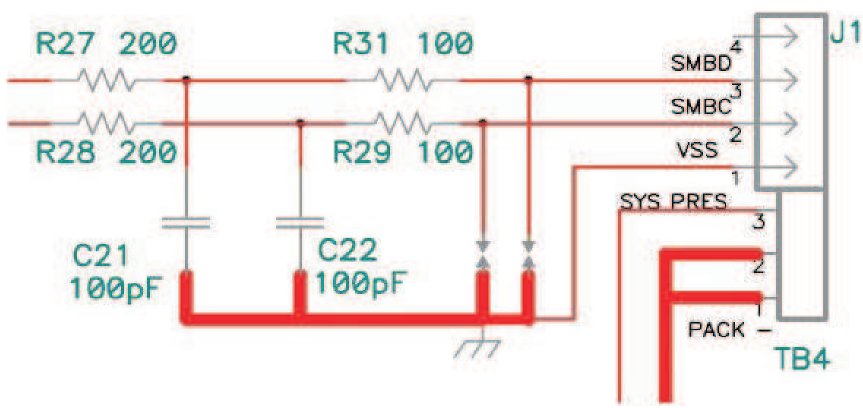


Figure 8. ESD Protection for SMB Communication

3.5 FUSE Circuitry

The FUSE pin of the bq3060 is designed to ignite the chemical fuse if one of the various safety criteria is violated. The FUSE pin is also used to monitor the state of the secondary-voltage protection IC. Q3 ignites the chemical fuse when its gate is high. R17, R19, and D2 form a logical OR gate, which enables the Q3 gate if either the FUSE signal or the output of the bq29412 device go to the high state. The 7-V output of the bq29412 is divided in half by R17 and R19, which provides adequate gate drive for Q3 while guarding against excessive back current into the bq29412 from D2 if the FUSE signal is high.

The use of C14 is generally good practice, especially for RFI immunity, but may be removed if desired because the chemical fuse is a comparatively slow device and is not affected by any sub-microsecond glitches that may come from the SAFE output during the cell connection process.

The combination of D2 and C14, and the gate capacitance form a peak detector with R17 and R19 as a discharge path. It is important to note that this network rectifies strong RF signals and produces a positive dc level on the gate of the FET. This potential issue can be avoided by ensuring that the trace on the anode side of D2 is kept short or is shielded by ground on both sides.

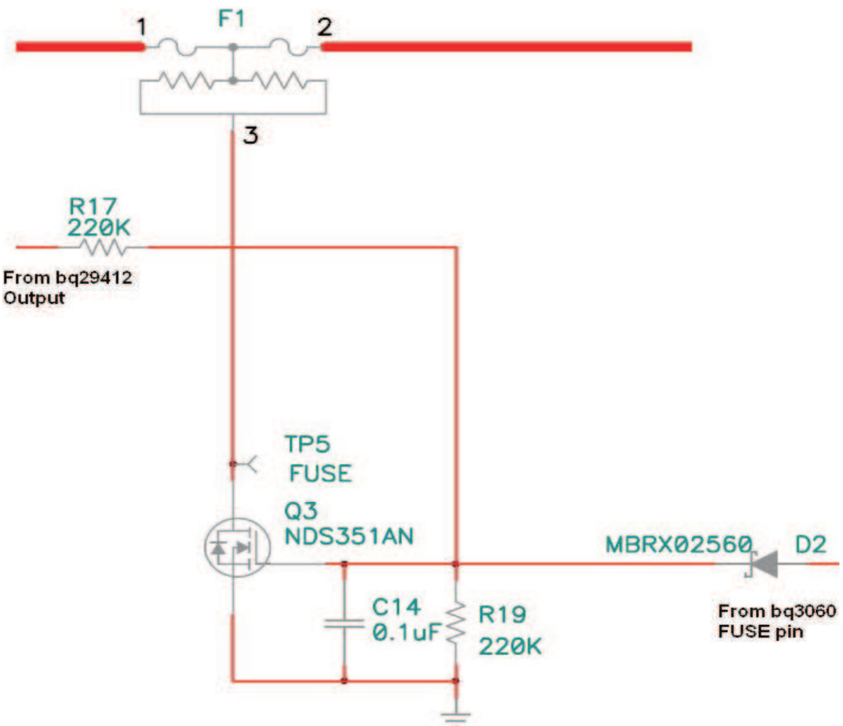


Figure 9. FUSE Circuit

When the bq3060 is commanded to ignite the chemical fuse, the FUSE pin activates to give a typical 8-V output. The new design makes it possible to use a higher Vgs FET for Q3. This improves the robustness of the system, as well as widens the choices for Q3.

3.6 PFIN Detection

As previously mentioned, the FUSE pin has a dual role on this device. When bq3060 is not commanded to ignite the chemical fuse, the FUSE pin defaults to sense the OUT pin status of the secondary voltage protector. When the secondary voltage protector ignites the chemical fuse, the high voltage is sensed by the FUSE pin, and the bq3060 sets the PFIN flag accordingly. It is highly recommended to place D2 as close to the device as possible. This arrangement helps to reduce EMI noise, and avoid the PFIN flag being set inadvertently. Changing the resistors (R17 and R19) to 110 kΩ can also reduce the EMI noise effect on the FUSE pin.

4 Secondary-Current Protection

The bq3060 provides secondary overcurrent and short-circuit protection, cell balancing, cell voltage multiplexing, and voltage translation. The following discussion examines Cell and Battery Inputs, Pack, and FET Control, Regulator Output, Temperature Output, and Cell Balancing.

4.1 Cell and Battery Inputs

Each cell input is conditioned with a simple RC filter. This filter provides ESD protection during cell connect and acts to filter unwanted voltage transients. The series resistors (R1, R2, R3, and R4) that connect the cell tabs to VC1 – VC4 pins of the bq3060 are required to be 1 kΩ for cell balancing and safety protection.

These filter resistors are used as part of a voltage divider to turn on external cell-balancing FETs. Further discussion occurs in the immediately following section. In addition to the external cell-balancing purpose, the 1-kΩ resistor value is also preferred to minimize voltage error. With the maximum filter resistor value being 1 kΩ, the resulting voltage error is approximately 2 mV to 4 mV.

The BAT input uses a diode (D1) and 1-µF ceramic capacitor (C13) to isolate and decouple it from the cells in the event of a transient dip in voltage caused by a short-circuit event.

Also, as described previously in Section 2, the top and bottom nodes of the cells must be sensed at the battery connections with a Kelvin connection to prevent voltage sensing errors caused by a drop in the high-current PCB copper.

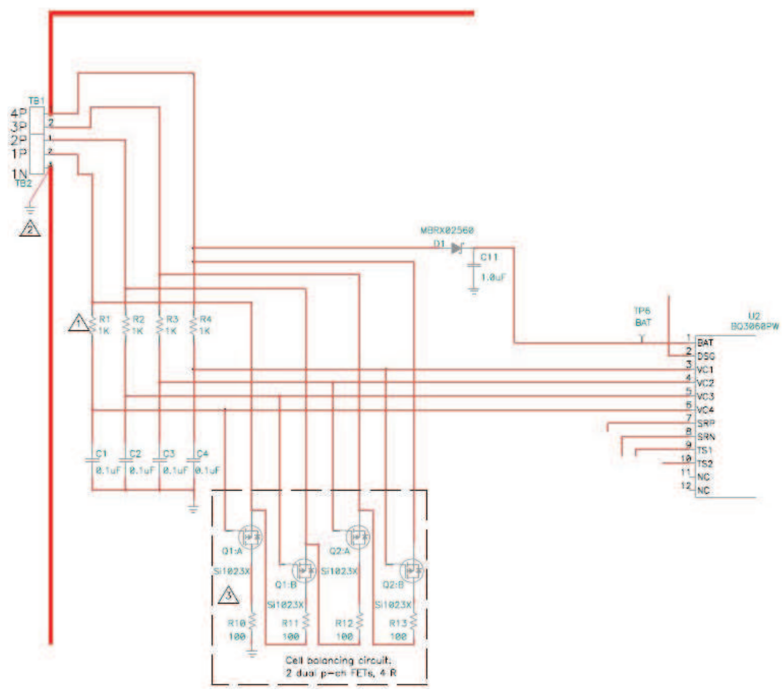


Figure 10. Cell and BAT Inputs

4.2 External Cell Balancing

Designed to provide a low-cost solution, the cell-balancing circuit is not included in the bq3060 data sheet reference schematic. However, the device does support this feature. The bq3060 can use an external P-ch FETs for cell balancing. This is accomplished by connecting an external parallel bypass load to each cell and enabling the bypass load, depending on each individual cell's charge state. When the cell-balancing control is enabled, the bq3060 is connected to an internal pulldown resistor. Designed to work with a 1-kΩ filtering resistor, the internal pulldown resistor and the filtering resistor create a voltage difference, which turns on the P-ch MOSFET and allows cell balancing to occur.

A conceptional diagram is shown in Figure 11. When cell balancing is activated to enable an internal pulldown path, 2 mA to 3 mA of current is pulled through the 1-kΩ filter resistor and the internal pulldown resistor. This creates an IR drop of 2 V to 3 V to turn on the external cell balance FET. Ensure that the cell balance FET is selected with proper Vgs. Resistors R10, R11, R12, and R13 are added in series of the P-ch FET to limit the cell-balancing current. Using a 100-Ω resistor as shown in this application report, the cell-balancing current is about 43 mA at 4 V and 32 mA at 3 V. Use different resistors values of R10-R13 if a different cell-balancing current is preferred.

Note that because R10-R13 are used for current limiting, the user must select higher-power-rated resistors and the cell-balancing trace must also widen up to withhold the target cell-balancing current.

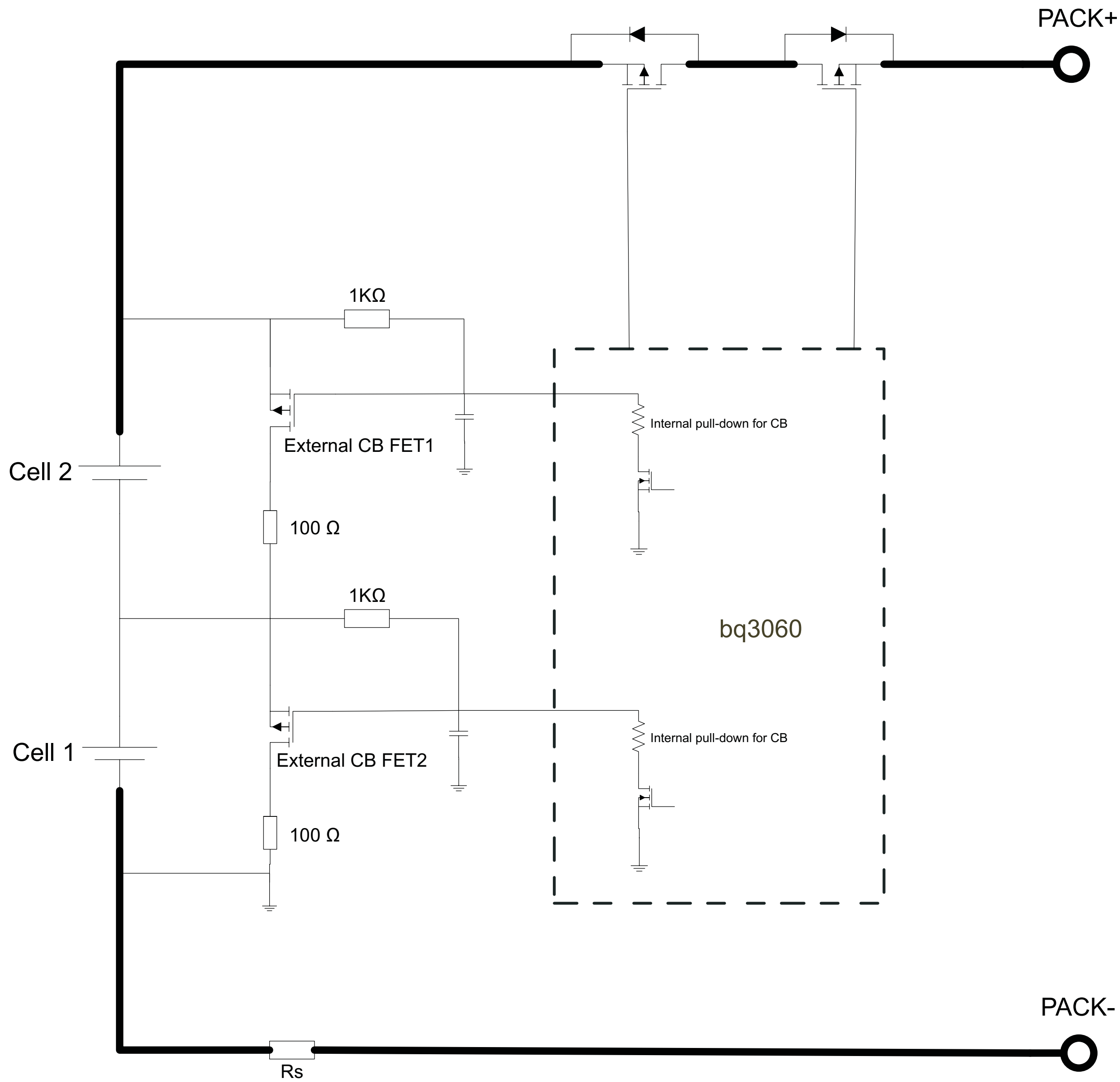


Figure 11. Conceptual External Cell-Balancing Circuit

4.3 PACK and FET Control

The PACK input provides power to the bq3060 from the charger. It also provides a method to measure and detect the presence of a charger. D3 is used to guard against input transients and prevents misoperation of the gate driver during short-circuit events. Ensure that the voltage rating of C20 is adequate to withstand the full-system voltage.

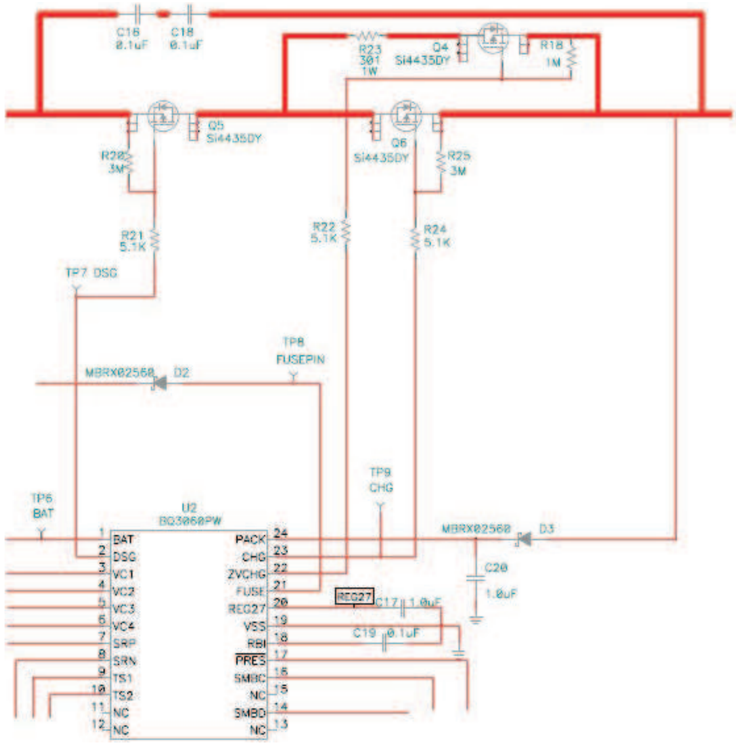


Figure 12. PACK and FET Control

The P-channel charge and discharge FETS are controlled with 5-kΩ series gate resistors, which provide a switching time constant of a few microseconds. The 3-MΩ resistors ensure that the FETs are off in the event of an open connection to the FET drivers. The precharge FET is a P-channel device.

4.4 Regulator Output

As mentioned in Section 3.2, the low-dropout regulator in the bq3060 requires capacitive compensation on the output. The REG27 output must have a 1-µF ceramic capacitor placed close to the IC terminal pin.

4.5 Temperature Output

TS1 (pin 9) and TS2 (pin 10) provide thermistor drive under program control. Each pin can be enabled with an integrated 18-kΩ (typical) linearization pullup resistor to support the use of a 10-kΩ at 25°C (103) NTC external thermistor such as a Mitsubishi BN35-3H103. The reference design includes two 10-kΩ thermistors, RT1 and RT2.

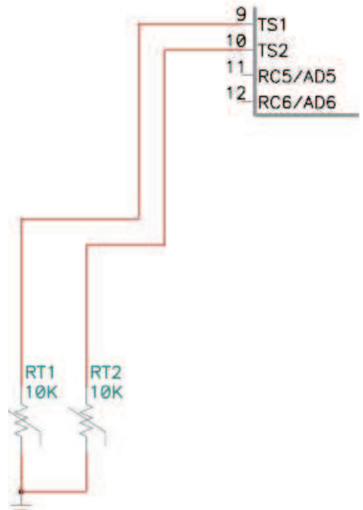


Figure 13. Thermistor Drive

5 Secondary-Voltage Protection

The bq29412 provides secondary-overvoltage protection and commands the chemical fuse to ignite if any cell exceeds the internally referenced threshold. The peripheral components are Cell Inputs and Time Delay Capacitor.

5.1 *Cell Inputs*

An input filter is provided for each cell input. This is comprised of resistors R5, R6, R7, and R9 along with capacitors C2, C4, C8, and C9. Note that this input network is completely independent of the filter network used as input to the bq3060. To ensure independent safety functionality, the two devices must have separate input filters.

Note that because the filter capacitors are implemented differentially, a low-voltage device can be used in each case.

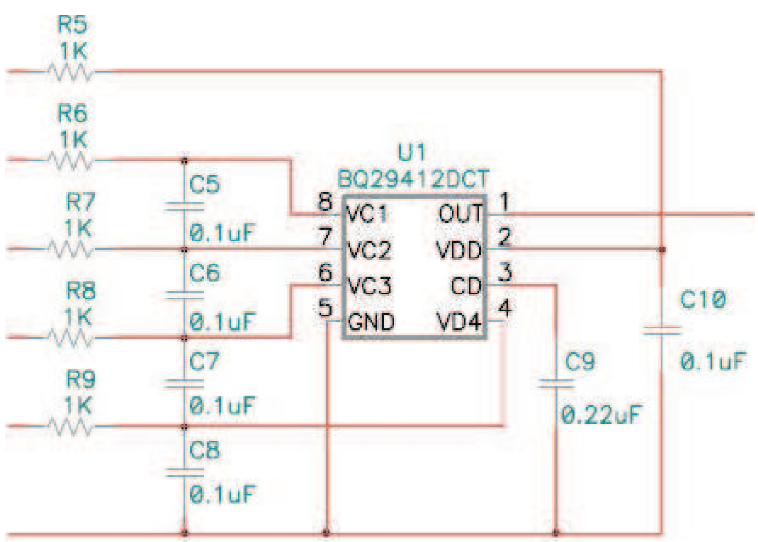


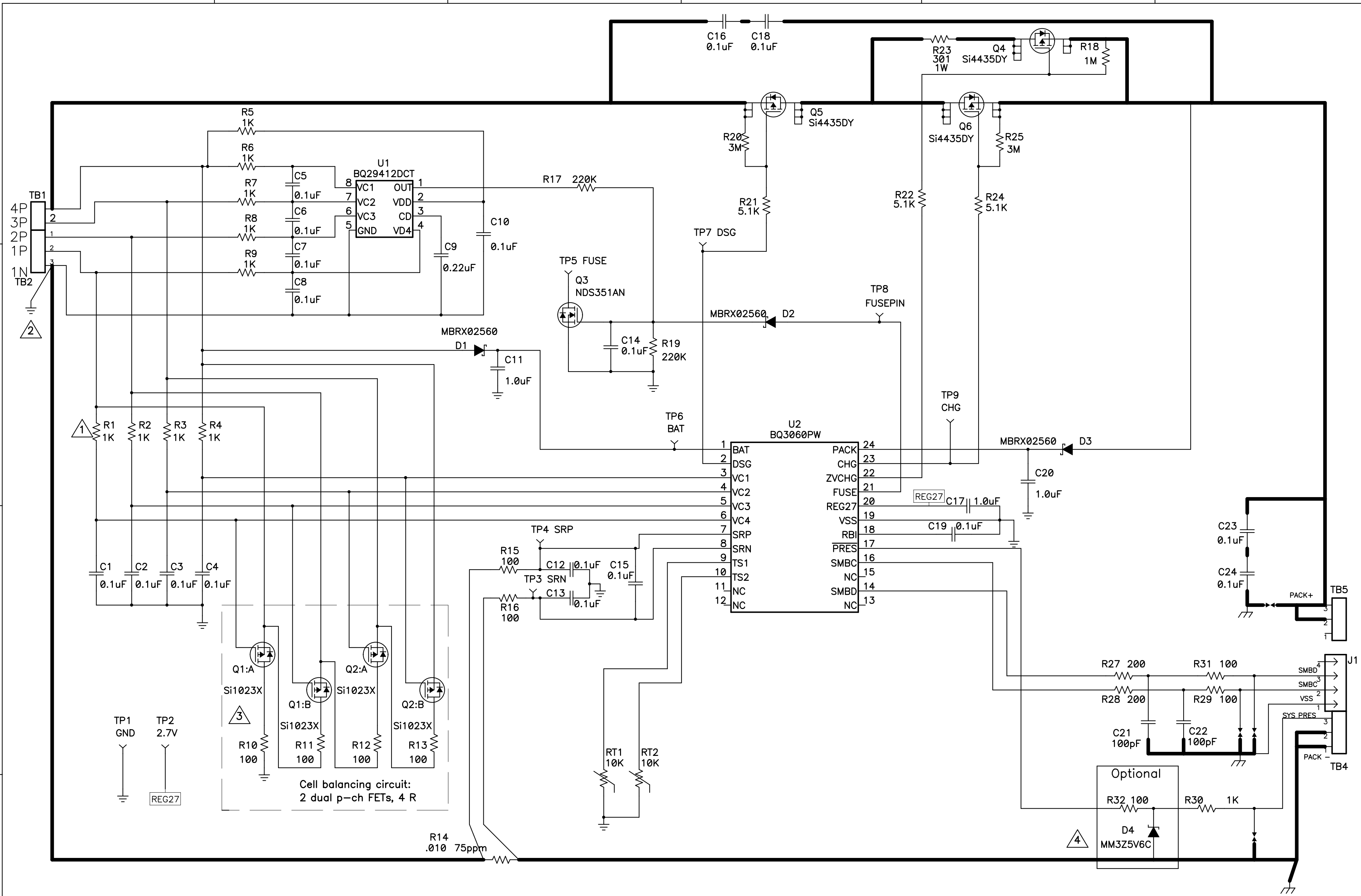
Figure 14. bq29412 Cell Inputs and Time-Delay Capacitor

5.2 Time-Delay Capacitor

C9 sets the time delay for activation of the output after any cell exceeds the threshold voltage. The time delay is calculated as td = 1.2 V × DelayCap (μF)/0.18 μA.

6 Reference Design Schematic

The reference schematic appears on the following page.



1. R1–R4: Required to be 1k.
2. IC ground should be connected to the 1N cell tab.
3. R10 – R13: If smaller resistors are used, user should make sure the power rating of the resistor can handle the desired cell balance current
4. Optional – Only required if PRES has a chance to short PACK+ (NOT AVALIABLE IN REV.A EVM)

Texas Instruments

Title	bq3060 EVM	
Size C	Number HPA328	Rev B
Date Thu Mar 26, 2009	Drawn by S. Wen	
Filename HPA328B.sch	Sheet 1 of 1	