Implementing a Bipolar Gate Drive for Low-Side IGBTs and SiC FETs in Motor Drives Applications

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BLDC Motor Drives applications such as pumps and compressors use three-phase inverters in their power modules to convert the rectified DC power to AC power necessary to control the speed, torque, and direction of the AC motors. IGBTs are the basic building blocks of the inverter stage which, in some cases, require a bipolar or unipolar gate drive supply to drive the low-side IGBT. When implementing a bipolar power supply to turn off the IGBTs, a level shifter is required to interface between the controller, referenced to GND, while the driver IC is referenced to negative power supply. This tech note discusses how to implement a level-shifter network to allow a bipolar gate drive, which is critical to safely turn off the low-side IGBT.

Low-Side Gate Driver Selection

The control architecture in Figure 1 is common practice in BLDC motor drives applications (< 5 kW) where the controller shares the same ground with the IGBTs in the inverter stage. This architecture allows the reinforced isolation to be implemented on the communication channels, as shown in Figure 1, and reduces the number of reinforced isolation gate drivers. This enables driving the low-side IGBTs without isolation while driving the high-side IGBTs with a functional isolated driver. This ensures a cost-optimized, compact solution where non-isolated, low-side gate drivers can effectively drive each of the three legs of the low-side IGBTs. The UCC27531 and family are available in SOT23 6-pin packages and have a wide V_{DD} voltage range (10 to 35 V), suitable for IGBTs that require a unipolar (+15 V / 0 V) or bipolar gate drive voltage (+15 V / -8 V).

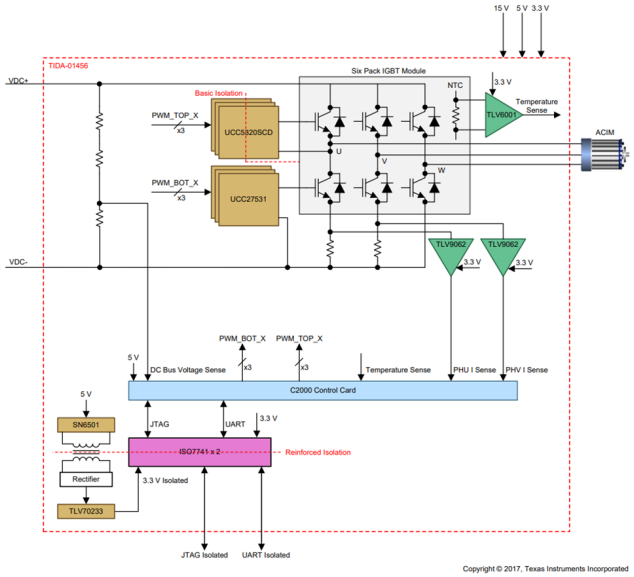

Figure 1. System Block Diagram

Unipolar Supply Operation

Some applications (low to medium power) use a unipolar gate drive with V_{DD}=15–18 V and VDC- = 0V to drive the IGBTs, in which case both the emitter of the IGBT, the MCU, as well as the gate driver and the decoupling capacitor of the gate driver CV_{DD} are referenced to the same 0-V ground.

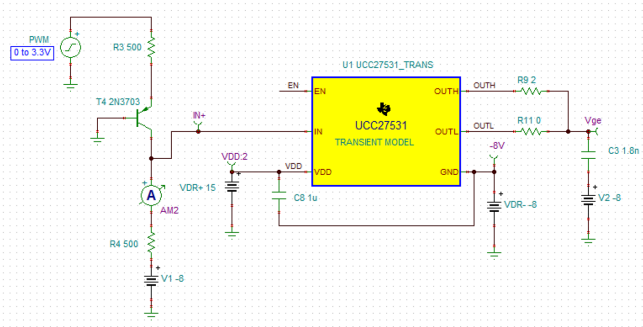

Figure 2. Simulations Schematic

Bipolar Supply Operation

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For medium to high power applications where the gate driver does not have the Miller clamp feature, there is a risk of Miller-induced turn-on when a high dv/dt is seen across the collector-to-emitter junctions of the IGBT. Leakage current in the form of $I_{CG} = C_{CG}*dV_{CE}/dt$ can couple at the gate, which can charge the gate voltage beyond the threshold of the IGBT. To overcome this issue, designers can use a bipolar gate drive operation where the negative voltage (V_{GE} = -5 to -8V) ensures that the collector-to-gate charge is lower than the gate to-emitter's to keep the IGBT fully off. To implement this, there are couples of key considerations to drive the low-side IGBT with a negative voltage.

Because both the low-side gate driver and low-side IGBT are referenced to the negative voltage supply, a level-shifter network is therefore required to interface the MCU signal, referenced to 0 V, and the gate driver IC, referenced to -8 V.

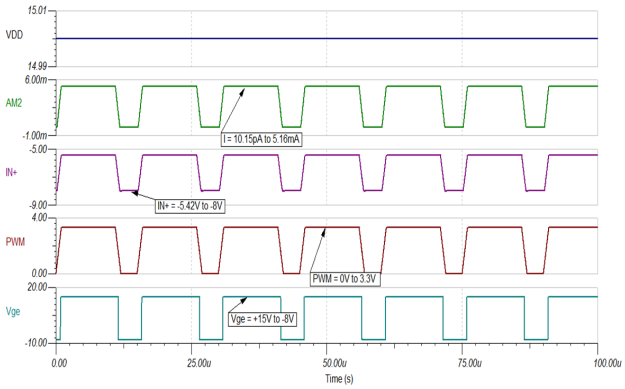

Figure 3. Simulation Results

The schematic in Figure 2 shows the PWM signal (0 to 3.3 V) referenced to 0 V while the driver GND pin is referenced to the -8-V negative supply necessary to fully turn off the IGBT. A low-cost PNP transistor in an emitter base configuration allows the control signal to interface with the input stage of the driver. In this configuration, the emitter is connected to the PWM signal with a resistor R_3 setting the current through the transistor. The base voltage is negatively biased with respect to the emitter, while the collector resistor R_4 (optional) helps dissipate power away from the transistor. C_8 is used to provide the peak current necessary to turn on the IGBT while also filtering noise on the supply pin of the driver. This capacitor, referenced to the negative supply -8 V, in practice must be placed directly across the V_{DD} pin of the driver. The EN pin of the driver left floating in this application ensures that this pin is internally pulled high through a 500-kΩ resistor. This EN pin is convenient for battery-powered applications to disable the driver and set it in a low current standby mode.

Figure 3 shows the PWM signal referenced to the 0-V controller ground while the driver input signal sees a PWM signal from -5.42 V to -8 V. AM2 captures the current through the level-shifter; this current is based on the power dissipation capability of the transistor, bandwidth, and desired prop delay. The V_{GE} at the output of the driver provides the positive gate voltage to turn on the IGBT/SiC and the negative voltage to keep the FET off during high dv/dt transitions.

Table 1. Alternate Devices

	UCC27531	UCC27533	UCC27536	UCC27537	UCC27538	UCC27532
Current Source/Sink	2.5 A / 5 A	2.5 A / 5 A	2.5 A / 5 A	2.5 A / 5 A	2.5 A / 5 A	2.5 A / 5 A
IN	Single	Dual	Single	Single	Dual	Single
EN	Yes	No	Yes	Yes	No	Yes
Output	Split	Single	Single	Single	Split	Split
Inverting	No	Yes	Yes	No	No	No

1 References

Texas Instruments, Gate Driver Overview Page

Texas Instruments, *UCC27531* Product Page

Texas Instruments, *UCC27531 EVM* Page

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