Application Note

Using Half-Bridge Gate Driver to Achieve 100% Duty Cycle for High Side FET

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ABSTRACT

In solar optimizer applications, Buck topology is frequently used in power stage of the whole system. Consequently, to drive the FETs inside Buck circuit, half-bridge gate driver is an easy way. But in solar optimizer or some other applications, the high side FET is often required to operate with 100% duty cycle. The common half-bridge gate driver with bootstrap diode and capacitor is unable to achieve 100% duty cycle for high side FET. Initially, this application note covers the background of why high side FET can operate with 100% duty cycle in optimizer. A design to achieve 100% duty-cycle using half-bridge gate driver is introduced subsequently. Also, risks that can arise in the design are analyzed by theory and simulation. Based on the theory and simulation, comparative experiments are also completed for verification. Design consideration and suggestions to avoid these risks are introduced in the end of the publication.

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1 Introduction

Solar optimizer is frequently used in string inverter system to maximize the output power of the solar panel. To achieve this goal, MPPT (Maximum Power Point Tracking) algorithm is widely used in the control of optimizer. MPPT's basic logic is to adjust the output voltage of optimizer which means adjust duty cycle of FETs to match output impendence. Buck topology is often used in optimizer. Once the output voltage of solar panel is equal or lower than the output voltage of buck converter when it operates in maximum power point, optimizer can go into pass through mode.

In pass through mode, the output power of solar panel can directly pass to the output of optimizer, and it is required high side FET of buck converter to operate with 100% duty cycle and low side FET to turn off.

In practice, the PWM signal of FETS can work in complementary with dead time. And the duty cycle of both FET can not go straight into 100% for high side FET or from 50% to 0% for the low side FET. Assume both duty cycle of FETs is 50% to achieve MPPT. And if from this moment light intensity consistently drops down, so the input voltage of optimizer which is also the output voltage of solar panel can decrease correspondingly. Once the controller detects that output voltage is below the threshold, duty cycle of high side FET can gradually increase to 100%.

There are two steps to consider if we want half-bridge gate driver to be used successfully in previously mentioned scenario. The first step is how to achieve 100% duty cycle for high side FET and the other step is what risk we can meet during the design and how to solve it.

2 Design and Potential Risk in Certain Application Scenario

In common half-bridge gate driver, bootstrap circuit is frequently used to drive two FETs with one power supply. But half-bridge gate driver with bootstrap circuit configuration is unable to drive high side FET with 100% duty cycle. Because the low side FET must be on for a certain time to let power supply charges the bootstrap capacitor up through bootstrap diode. If not, bootstrap capacitor can be unable to provide power for driving high side FET.

For one design to achieve 100% duty-cycle using half-bridge gate driver is to add extra power supply between HB and HS pin of gate driver. Figure 2-1 shows specific schematic. Then the energy to drive high side FET can be provided by this extra power supply instead of bootstrap capacitor. Then the high side FET is able to operate with 100% duty cycle.

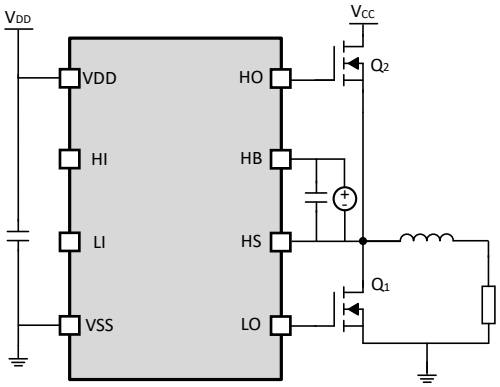

Figure 2-1. Overview of Proposed Design

The potential risk mainly appears from two reasons:

1. High duty cycle causes high current stress in bootstrap diode.
   For example, in the pass-through mode of optimizer, duty cycle of high side FET can gradually increase up to 100%. So, by end of transition process, a high duty cycle condition that persists for a period of time can let bootstrap diode withstand high current stress.
2. Influence by the extra power supply which is connected in HB, HS pin.
   Indeed, adding one extra power supply can let gate driver drive high side FET with 100% duty cycle. But the process still has some design consideration to make sure gate driver works properly. Improper design can increase bootstrap diode current stress during the transition process which is mentioned in reason 1.

These two reasons can be analyzed in the following details.

3 Analysis of Potential Problem

3.1 High Duty Cycle Causes High Current Stress in Bootstrap Diode

Let us analyze why high duty cycle can cause high current stress in bootstrap diode and assume power supply V_2 do not involve in first. Taking optimizer as the example, at the end of transition process from buck mode to pass through mode, high side FET duty cycle can nearly approach 100% and duty cycle of low side FET can nearly approach 0%, Figure 3-1 shows the time diagram of PWM signal. There are four operation modes during the transition period. Figure 3-2 shows the equivalent circuits of system.

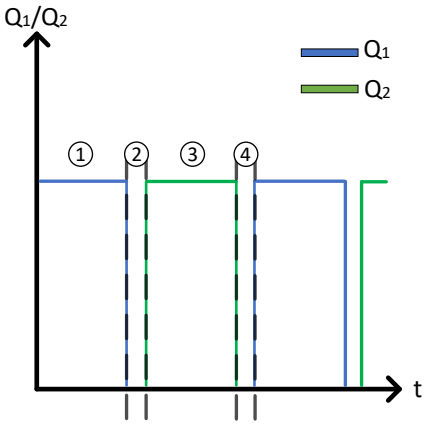

Figure 3-1. Time Diagram of PWM Signal

- Blue Line: low side MOSFET gate to source PWM signal
- Green Line: high side gate to source PWM signal

In practical applications, a common way to create these power supplies is to use fly-buck or fly-back topology with multiple windings. Assume two power supplies is produced by different windings, and connected to the VDD, GND, HB, HS separately. for better understanding, analysis for different modes are accomplished as follows.

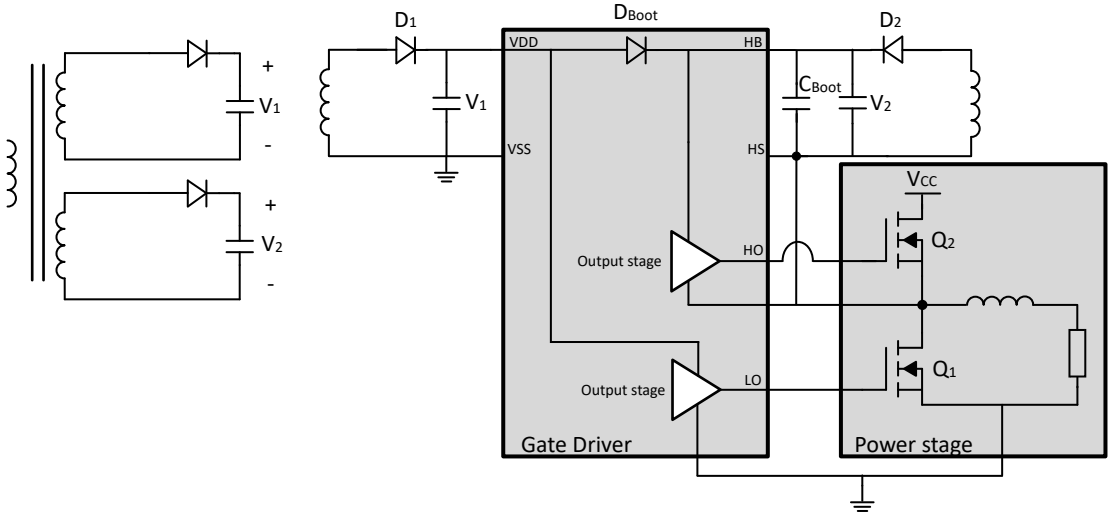

Figure 3-2. Schematic of System

3.1.1 Mode 1

In this mode, Q_1 is on and Q_2 is off. The equivalent circuit of this mode is shown in Figure 3-3.

Because when Q_1 turns on, FET can be modeled as a resistor, the value is equal to RDSON. V_1 can charge the bootstrap capacitor, so the voltage in bootstrap capacitor can increase gradually. One thing we can take into consideration is in this mode, inductor current can continue flowing from the ground to HS point. A voltage drop is created by the inductor current, furthermore, the HS voltage refer to the ground can be negative. This phenomenon can let bootstrap capacitor charge to a higher value. If we assume the voltage drop in bootstrap diode is V_{d1} and V_{d2} in body diode of FET, we can obtain the equation of voltage value in bootstrap capacitor, which is:

$$V_{CBOOT1} = V_1 - V_{d1} + V_{RDSON} \quad (1)$$

V_{CBOOT1}: voltage in bootstrap capacitor in mode 1

V_{d1}: forward voltage drop of bootstrap diode

V_{RDSON}: voltage drop in FET

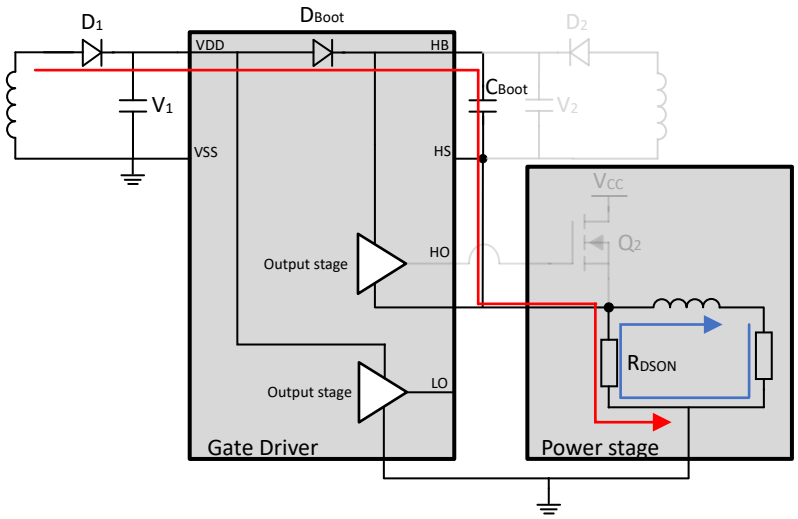

Figure 3-3. Equivalent Circuit in Mode 1

But in practice, a certain amount of time is needed to charge the bootstrap capacitor, if the time is limited, voltage in bootstrap diode can not reach the theoretic maximum value V_{CBOOT1}. Also, a bootstrap capacitor can not be charged if the capacitor has been charged to a value higher than V_{CBOOT1} in mode 2 or 4.

3.1.2 Mode 2

Mode 2 is a dead time period after Q_1 turns off and Q_2 still remains off. This mode is similar to mode 1. The only difference is that the inductor current can flow through body diode of Q_1. And in most cases, the voltage drop in body diode is higher than the V_{RDSON}. This means that voltage difference between bootstrap capacitor can higher than the difference in mode 1 and may overcharge the bootstrap capactitor. Using equation to express bootstrap voltage value is:

$$V_{CBOOT2} = V_1 - V_{d1} + V_{d2} \quad (2)$$

V_{CBOOT2}: voltage in bootstrap capacitor in mode 2

V_{d1}: forward voltage drop of bootstrap diode

V_{d2}: voltage drop of MOSFET body diode

Because V_{d2} is larger than V_{RDSON}, so V_{CBOOT2} can be larger than the V_{CBOOT1}. In facts, the voltage in bootstrap capacitor can be the maximum value in this mode if we do not count the potential oscillation in HS to ground voltage. Figure 3-4 shows equivalent circuits in mode 2.

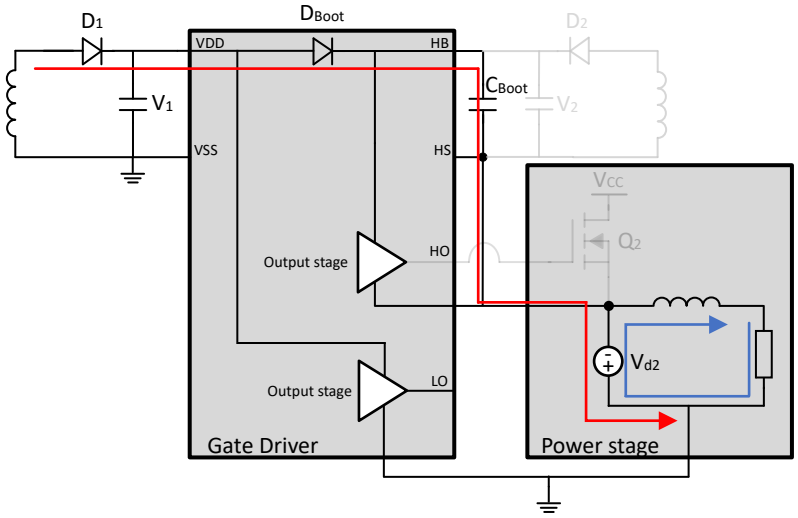

Figure 3-4. Equivalent Circuit in Mode 2

3.1.3 Mode 3

In this mode, Q_1 remains turn-off and Q_2 gradually turns on. Figure 3-5 shows equivalent circuits in mode 3.

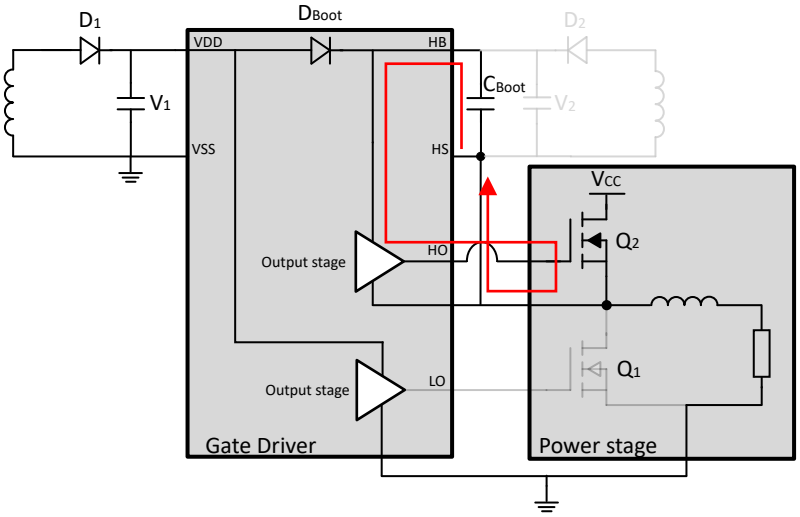

Figure 3-5. Equivalent Circuit in Mode 3

Assume the input voltage of power stage is V_{CC} . Due to the turn on process of Q_2, voltage in HS node can increase rapidly from V_{d2} to V_{CC}. So, HB to ground voltage can increase correspondingly. This can let bootstrap diode become reverse bias, a reverse recovery process can happen, reverse current can flow through bootstrap diode. This is the main risk to cause damage with gate driver.

3.1.4 Mode 4

This is another dead time period once Q_2 and Q_1 both turn off. Mode 4 is also similar to mode 2. A slight difference is that now the bootstrap capacitor has provided power to drive the high side FET. Voltage in bootstrap diode is decreased to the lowest value in steady state. Others remain the same as in mode 2.

In conclusion, influence to the gate driver caused by power stage is to change the voltage potential in HS node. Moreover, this influence can affect the working condition of bootstrap diode, forward conduction or reverse bias.

Previously mentioned is the working principle of bootstrap circuits, the influence of extra power supply in HB-HS can be discussed later. First, simulation can be used to explain why higher duty cycle can cause higher current stress in bootstrap diode.

In simulation using PSpice™, duty cycle of Q_2 is set to 50% and bootstrap diode without reverse recovery characteristic is used first. Value of bootstrap capacitor is 100nF.

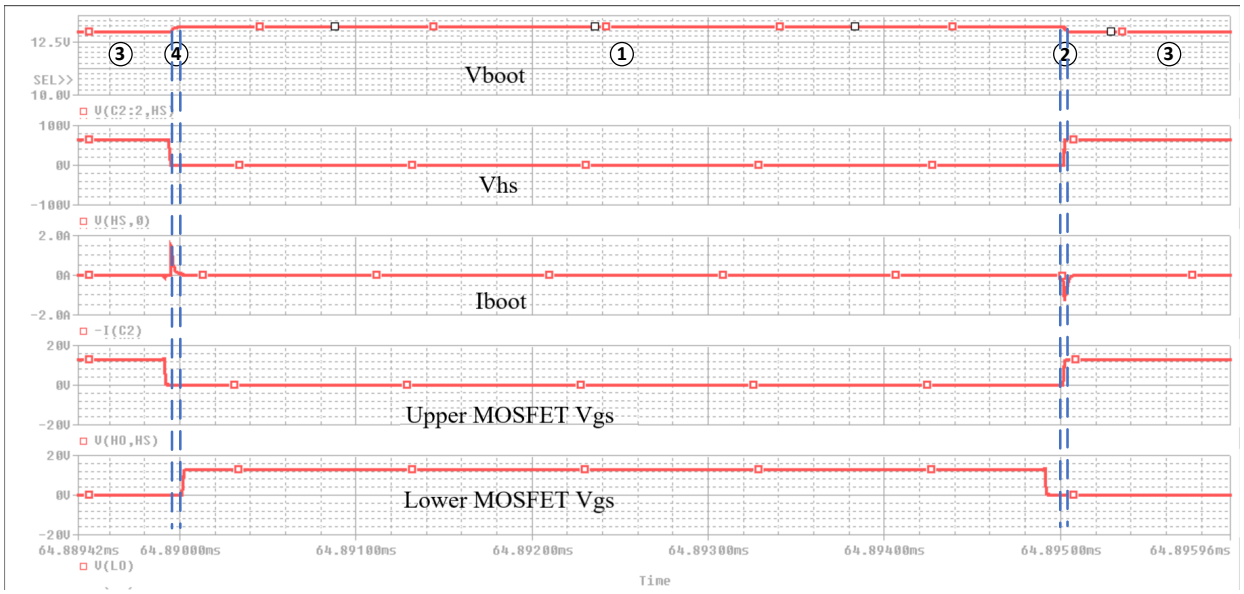

Figure 3-6. Simulation Results (D=50%, C_{boot}=100nF)

D: duty cycle of high side FET

V_{boot}: voltage in bootstrap capacitor

V_{hs}: HS to ground voltage

I_{boot}: current flows into bootstrap capacitor

As shown from Figure 3-7, the bootstrap capacitor can be charged in mode 4. And because V_{boot} have increased to a higher value than the possible maximum voltage in mode 1. Voltage of bootstrap capacitor can remain the same at mode 1. In the transition time from mode 2 to 3, bootstrap capacitor can provide power to turn-on the FET, so we can see the negative current in I_{boot} and the voltage drop in V_{boot}. The simulation results basically verified the theoretical analysis.

And what can happen if we increase duty cycle to a higher value. We increase the duty cycle to 99%.

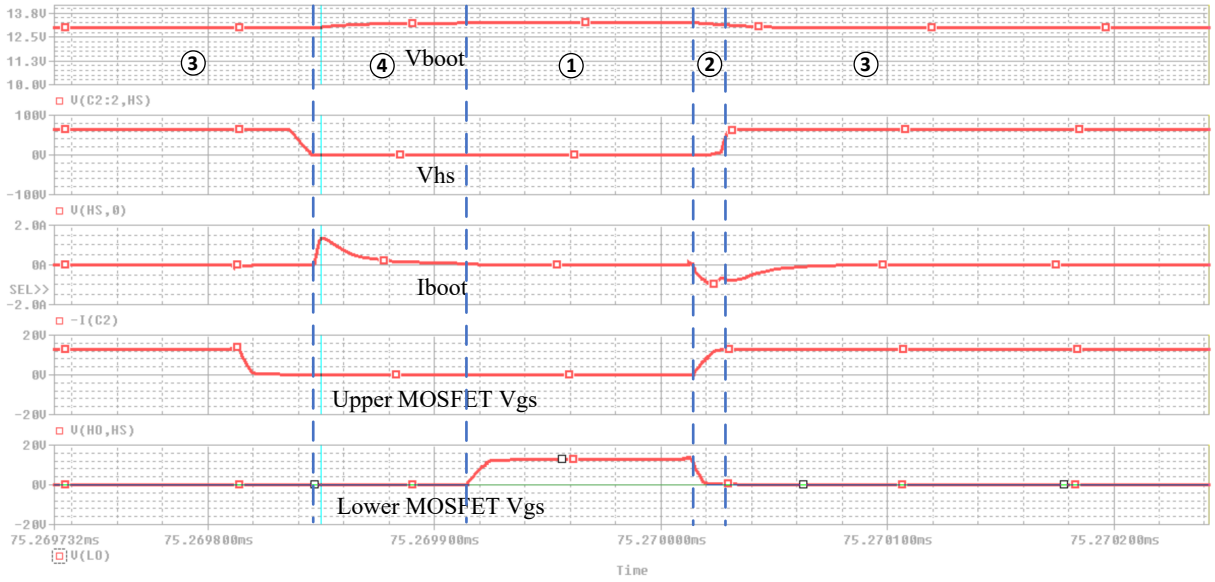

Figure 3-7. Simulation Results (D=99%, C_{boot}=100nF)

As shown, the transitions are tighter which means the bootstrap diode can withstand higher current stress in a short time.

Using same 100nf bootstrap capacitor, but adding reverse recovery characteristic in diode to do the simulation. As shown, large reverse current flows through body diode.

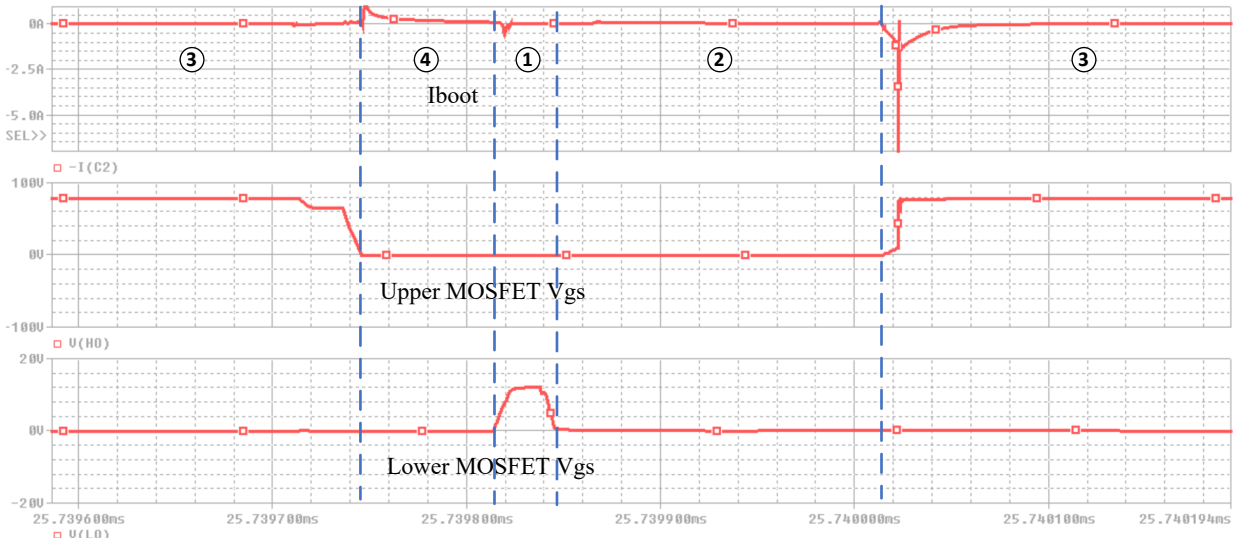

Figure 3-8. Simulation Results (D=99% With Reverse Recovery Characteristic)

And another key point is that if we consider the reverse recovery current of the bootstrap diode, the current stress can be more serious in high duty cycle than the normal duty cycle. Reverse recovery current is associated with reverse recovery time and forward current at the time that diode withstand reverse bias. Reverse recovery time is mainly decided by physical characteristic of diode. So, the forward current is what we can consider in that situation. Compared with small capacitance, lager bootstrap capacitance can have larger time constant. So, if

duty cycle of high side FET is approached to 100%, there is no enough time to charge the larger capacitor up, and current can maintain a higher value when working mode is changed to mode 3 (high side FET on, low side FET off). This causes a higher reverse recovery current than using small bootstrap capacitor because charging current of small capacitor can decrease to a low side value if the time keep the same. But in normal duty cycle, charge or discharge current all can decrease to a low value.

In facts, if we connect extra power supply in HB-HS and did not design properly, the influence is increased the equivalent capacitance and causes higher reverse recovery current.

3.2 Influence by the Extra Voltage Source

In this chapter, influence by the extra power supply connected in HB-HS pin is discussed.

The typical schematic when we consider the effect of extra power supply is shown in Figure 3-9. Based on the analysis, the influence of power stage to gate driver can be modeled as a power supply connected in HS pin and ground. The value of power supply will change from V_{d2} to V_{RDSON} to V_{CC}.

The proper operation process is all the power to drive Q_2 is provided by the V_2 in mode 3. And in mode 1, all the power to turn on low side FET is provided by V_1. So, no current flow through bootstrap diode now, bootstrap capacitor can be considered as a filter capacitor. So current stress in bootstrap diode will be zero since there is not current flow through it.

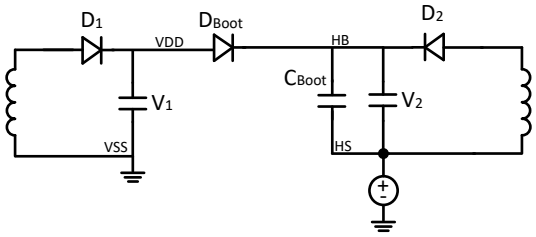

Figure 3-9. Schematic With V_2 Connected

In most of the design, we often just let V_1 vaguely equal to V_2, but this will cause some problems in certain application. The key point is the voltage difference between V_1 and V_2.

If we let $V_1 > V_2+V_{d1}$, So the bootstrap circuits will work normally like above analysis. Because output capacitor is in parallel with bootstrap capacitor, and in all of working mode, voltage between HB-HS will be larger than the V_2, So D_2 will withstand reverse bias all the time. It means that V_2 isn't involved in the system. The only difference in that situation compared to the normal bootstrap circuit operation is that the output capacitor is in parallel with the bootstrap capacitor which means the equivalent capacitance is increased. This will cause more serious current stress in bootstrap diode as we analyze above.

But with one exception, if FET consume too much power of capacitor, V_2 will charge bootstrap capacitor which means the voltage of bootstrap capacitor has been clamped. But this will have limited positive effect for the solution.

Based on the analysis above, simulation and experiments are made to verify the theory.

In Figure 3-10 and Figure 3-11, we compared the current flowing into the bootstrap capacitor in the transient period.

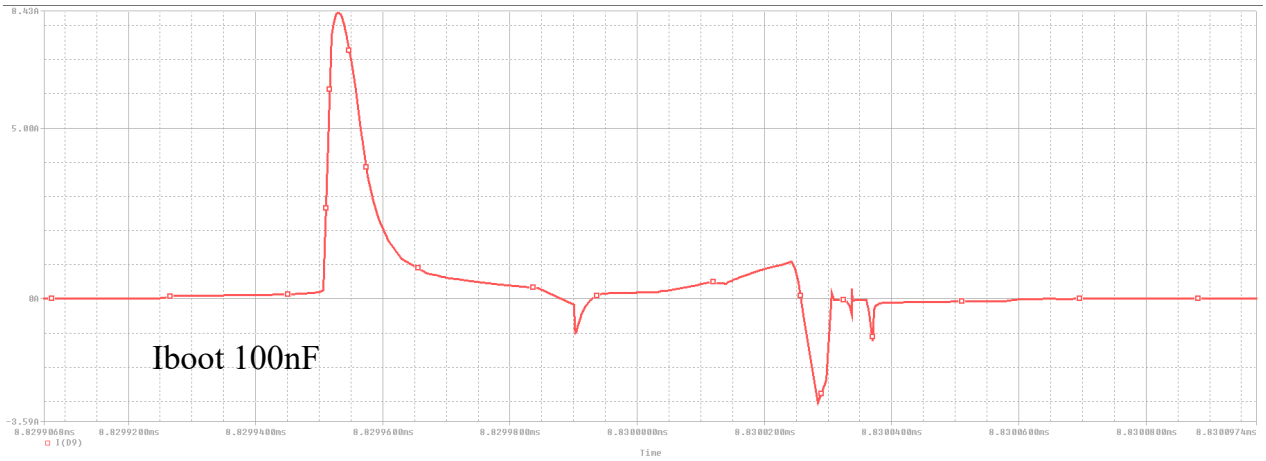

Figure 3-10. Simulation Results (D=99.5% With 100nF Bootstrap Capacitor)

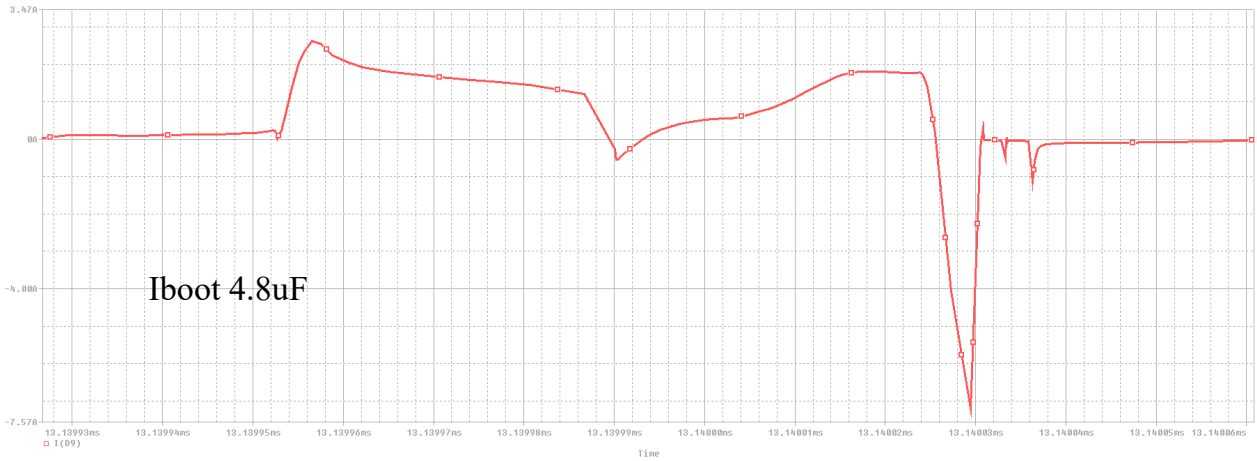

Figure 3-11. Simulation Results (D=99.5% With 4.7uF Bootstrap Capacitor)

As shown from the simulation results. If we increase bootstrap capacitor, reverse recovery current can increase dramatically. In product application, there is a high risk to cause failure to the gate driver.

Table 3-1. Specifications using LM76003

Input voltage	Output voltage	Output current	Capacitance	Duty cycle
5.5V	5.02V	1A	100nF/4.8uF	91.2%

Next, we use LM76003 to verify theory, specification of test is shown in Table 3-1. Current probe is used to test the current flowing from HB pin to bootstrap capacitor. As we can see from Figure 3-12 and Figure 3-13, as the bootstrap capacitance increases, reverse recovery current is also increases from -149mA (100nF) to -165mA (4.8uF). And if we use UCC27282 or some other gate driver ICs to build discrete high-power, reverse recovery current amplitude and slew rate when capacitor increase will be higher.

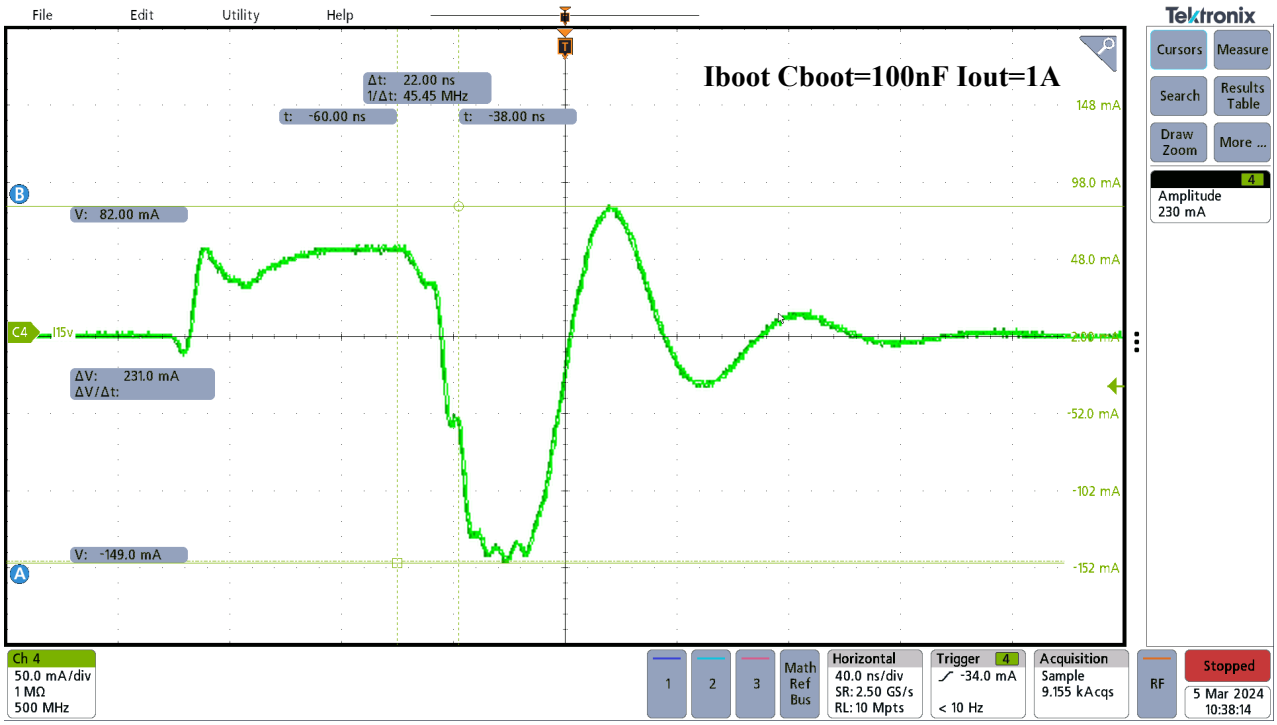

Figure 3-12. Experiment Results (100nF Bootstrap Capacitor)

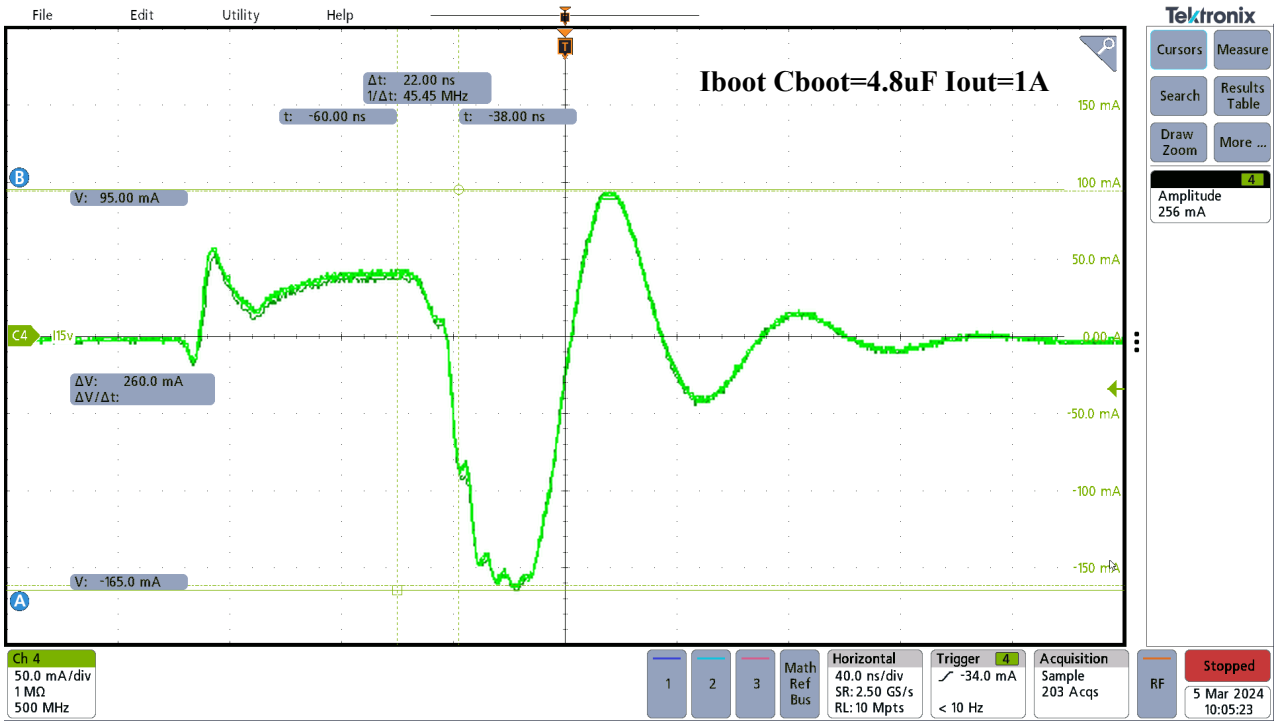

Figure 3-13. Experiment Results (4.8uF Bootstrap Capacitor)

As shown from the simulation and experiments results. If V_1>V_2-V_{d1}, current stress increases because equivalent capacitance is increased. In product application, this process can cause failure of gate driver.

4 Design Recommendation

To achieve this design properly, V_2 must be larger than V_1.

$$V_2 > V_1 \tag{3}$$

When V_2 is larger than V_1, bootstrap diode can keep reverse bias all the time which means V_1 can only provide power to internal circuits of gate driver and low side FET. Energy to drive high side FET can come from V_2.

Based on the previous analysis, we can also improve the current ability of gate driver to avoid the risk. The suggestion is to add external bootstrap diode such as Schottky or fast recovery diode.

Or we can just use half-bridge gate driver without built-in bootstrap diode. Because in this design, bootstrap diode can always work in reverse bias, so we can just simply remove this diode and the requirement of power supply's amplitude can not exist. For example, we can use UCC27888 to simplify the design process.

5 Summary

This application note provides an easy implemented design to drive high side FET with 100% duty cycle using half-bridge gate driver. This design only needs an extra power supply connected to a gate driver. The operation principle with or without extra power supply are analyzed. Furthermore, the potential risks that can occur in some certain application scenarios are also analyzed. A clear explanation and design consideration to this design are given and simulation and experiments are utilized to verify the theory.

6 References

- Texas Instruments, *Challenges and Solutions for Half-Bridge Gate Drivers in Bidirectional DC-DC Converters*, application note.
- Texas Instruments, *Bootstrap Circuitry Selection for Half Bridge Configurations*, application note.
- Texas Instruments, *UCC27282 3-A 120-V Half-Bridge Driver with Cross Conduction Protection and Low Switching Losses*, data sheet.
- Texas Instruments, *LM76002/LM76003 3.5-V to 60-V, 2.5-A/3.5-A Synchronous Step-Down Voltage Regulator*, data sheet.

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