Functional Safety Information

TPS57112C-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TPS57112C-Q1 (WQFN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

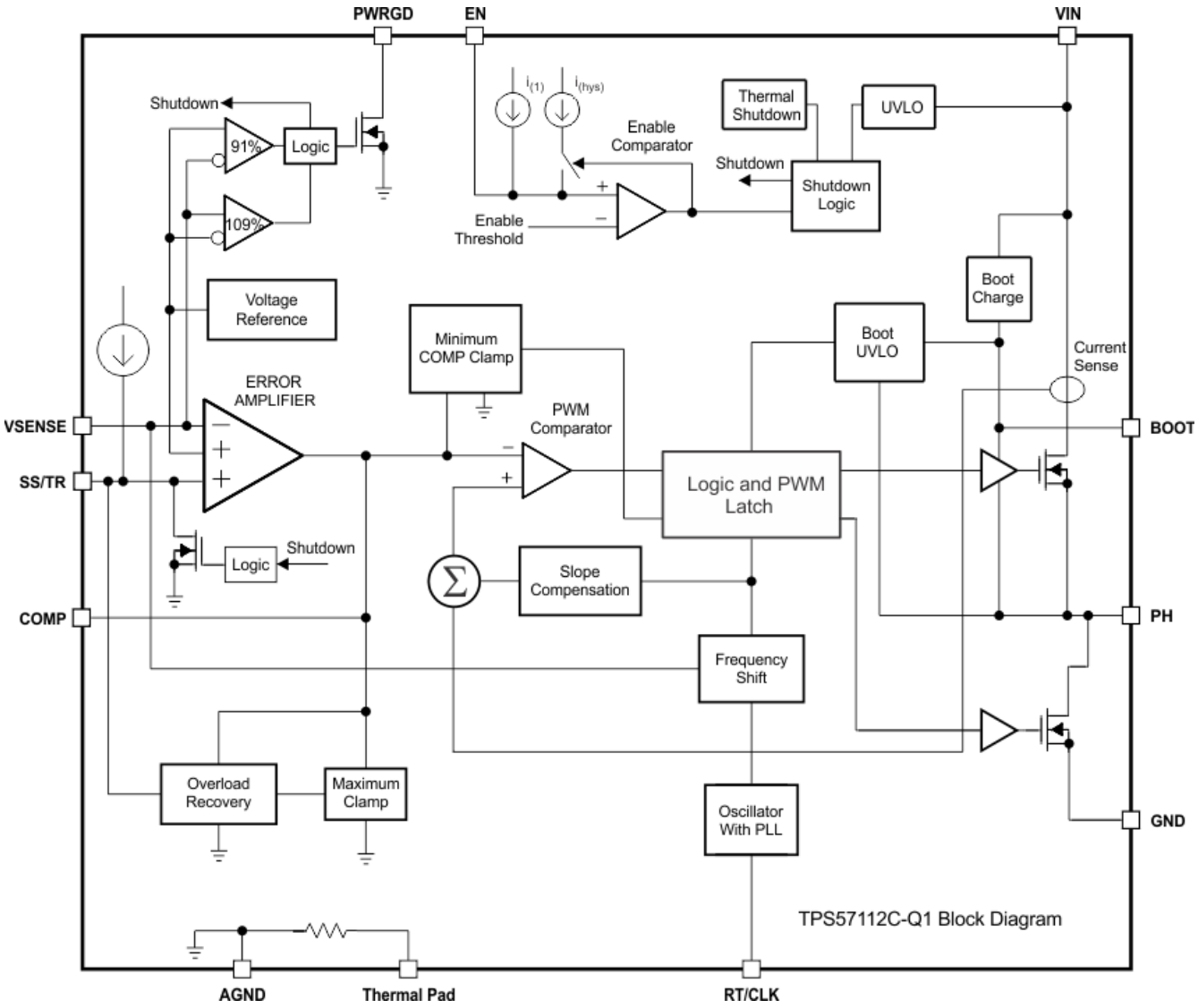

Figure 1-1. Functional Block Diagram

TPS57112C-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

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2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for TPS57112C-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	3
Package FIT Rate	7

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 450 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	20 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

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3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TPS57112C-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
No PH output	45%
PH output not in specification – voltage or timing	35%
PH Power FET stuck on	10%
PGOOD false trip, fails to trip	5%
Short circuit any two pins	5%

The FMD in Table 3-1 excludes short circuit faults across the isolation barrier. Faults for short circuit across the isolation barrier can be excluded according to ISO 61800-5-2:2016 if the following requirements are fulfilled:

1. The signal isolation component is OVC III according to IEC 61800-5-1. If a SELV/PELV power supply is used, pollution degree 2/OVC II applies. All requirements of IEC 61800-5-1:2007, 4.3.6 apply.
2. Measures are taken to ensure that an internal failure of the signal isolation component cannot result in excessive temperature of its insulating material.

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

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4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPS57112C-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VIN (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPS57112C-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TPS57112C-Q1 data sheet.

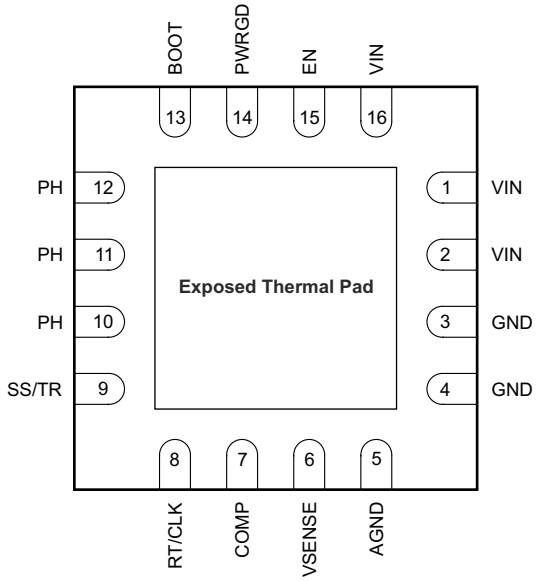

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Assumption the device is running in the typical application, please refer to the 'Simplified Schematics' on the first page in the TPS57112C-Q1 data sheet.

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Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	Device does not power up, no output voltage	B
VIN	2	Device does not power up, no output voltage	B
GND	3	Normal operation	D
GND	4	Normal operation	D
AGND	5	Normal operation	D
VSENSE	6	100% duty cycle operation, no regulated output voltage. Output voltage will follow the input voltage and go low periodically during refresh cycles of the bootstrap capacitor	B
COMP	7	0% duty cycle operation, no output voltage	B
RT/CLK	8	Device is not switching, no output voltage	B
SS/TR	9	Device does not turn on, no output voltage	B
PH	10	Potential device damage	A
PH	11	Potential device damage	A
PH	12	Potential device damage	A
BOOT	13	Damage the V_{IN} to BOOT path	A
PWRGD	14	PWRGD signal is always low, output voltage is regulated as programmed	B
EN	15	Device is disabled, no output voltage	B
VIN	16	Device does not power up, no output voltage	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	Normal operation, pins 2 and 16 are still connected	C
VIN	2	Normal operation, pins 1 and 16 are still connected	C
GND	3	Normal operation, pin 4 is still connected	C
GND	4	Normal operation, pin 3 is still connected	C
AGND	5	Normal operation, potential jitter issues	C
VSENSE	6	100% or 0% duty cycle operation, no regulated output voltage. Output voltage will either follow the input voltage and go low periodically during refresh cycles of the bootstrap capacitor or no output voltage	B
COMP	7	No loop compensation, output voltage can oscillate	B
RT/CLK	8	Very low switching frequency operation	B
SS/TR	9	No softstart function, output voltage is regulated as programmed	C
PH	10	Normal operation, pins 11 and 12 are still connected	C
PH	11	Normal operation, pins 10 and 12 are still connected	C
PH	12	Normal operation, pins 10 and 11 are still connected	C
BOOT	13	Boot capacitor is not charged, high side switch cannot be turned on, no output voltage	B
PWRGD	14	PWRGD signal is not available, output voltage is regulated as programmed	B
EN	15	EN pin is internally pulled up, device cannot be disabled, output voltage is regulated as programmed	B
VIN	16	Normal operation, pins 1 and 2 are still connected	C

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Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	2	Normal operation	D
VIN	2	3	Device does not power up, no output voltage	B
GND	3	4	Normal operation	D
GND	4	5	Normal operation	D
AGND	5	6	100% duty cycle operation, no regulated output voltage. Output voltage will follow the input voltage and go low periodically during refresh cycles of the bootstrap capacitor	B
VSENSE	6	7	No loop compensation, can cause output voltage oscillating. Oscillation frequency cannot be predicted.	B
COMP	7	8	Device will not start properly, no output voltage or too low output voltage	B
RT/CLK	8	9	tracking driven by RT/CLK voltage, low voltage at the output	B
SS/TR	9	10	Potential device damage, no output voltage	A
PH	10	11	Normal operation	D
PH	11	12	Normal operation	D
PH	12	13	Boot capacitor is not charged, high side switch cannot be turned on, no output voltage	B
BOOT	13	14	Potential device damage	A
PWRGD	14	15	Potential device damage	A
EN	15	16	Device cannot be disabled, output voltage is regulated as programmed	C
VIN	16	1	Normal operation	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VIN

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
VIN	1	Normal operation	D
VIN	2	Normal operation	D
GND	3	Device does not power up, no output voltage	B
GND	4	Device does not power up, no output voltage	B
AGND	5	Device does not power up, no output voltage	B
VSENSE	6	Potential device damage	A
COMP	7	Potential device damage	A
RT/CLK	8	Device is not switching, no output voltage	B
SS/TR	9	Potential device damage	A
PH	10	Potential device damage	A
PH	11	Potential device damage	A
PH	12	Potential device damage	A
BOOT	13	Boot capacitor is not charged, high side switch cannot be turned on, no output voltage	B
PWRGD	14	Potential device damage	A
EN	15	Device cannot be disabled, output voltage is regulated as programmed	C
VIN	16	Normal operation	D

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2020) to Revision A (November 2020)	Page
• Updated functional safety document to new template	2
• Added pin FMA	5

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